7. Signal Conditioning in Oscilloscopes and the Spirit of Invention

The Spirit of Invention

When I was a child my grandfather routinely asked me if I was going to be an engineer when I grew up. Since some of my great-uncles worked on the railroads, I sincerely thought he wanted me to follow in their footsteps. My grandfather died before I clarified exactly what kind of engineer he hoped I would become, but I think he would approve of my interpretation.

I still wasn't sure what an engineer was when I discovered I wanted to be an inventor. I truly pictured myself alone in my basement toiling on the important but neglected problems of humanity. Seeking help, I joined the Rocky Mountain Inventors' Congress. They held a conference on invention where I met men carrying whole suitcases filled with clever little mechanical devices. Many of these guys were disgruntled and cranky because the world didn't appreciate their contributions. One of the speakers, a very successful independent inventor, told of a bankrupt widow whose husband had worked twenty years in isolation and secrecy inventing a mechanical tomato peeler. The tomato peeler had consumed the family savings, and the widow had asked the speaker to salvage the device. With sadness the speaker related the necessity of informing her that tomatoes were peeled in industrial quantities with sulfuric acid. Apparently the inventor had been too narrowly focused to realize that in some cases molecules are more powerful than machines.

I didn't want to become disgruntled, cranky, or isolated and I didn't even own a basement. So I went to engineering school and adopted a much easier approach to inventing. I now design products for companies with such basic comforts as R&D budgets, support staff, and manufacturing operations. Along the way I have discovered many ways of nurturing inventiveness. Here are some techniques that seem to work:

Give yourself time to invent. If necessary, steal this time from the unending rote tasks that your employer so readily recognizes and rewards. I try to work on things that have nothing to do with a particular product, have no schedule, and have no one expecting results. I spend time on highly tangential ideas that have little hope for success. I can fail again and again in this daydream domain with no sense of loss. Get excited. Enjoy the thrilling early hours of a new idea. Stay up all night, lose sleep, and neglect your responsibilities. Freely explore tangents to your new idea. Digress fearlessly and entertain the absurd. Invent in the morning or whenever you are most energetic. Save your "real" work for when you are tired.

Master the fundamentals of your field. The most original and creative engineers I have known have an astonishing command of undergraduatelevel engineering. Invention in technology almost always stems from the novel application of elementary principles. Mastery of fundamentals allows you to consider, discard, and develop numerous ideas quickly, accurately, and fairly. I believe so much in this concept that I have begun taking undergraduate classes over again and paying very careful attention.

Honestly evaluate the utility of your new idea at the right time: late enough not to cut off explorations of alternatives and wild notions, but early enough that your creativity doesn't go stale. In this stage you must ask the hardest questions: "Is this new thing useful to anyone else? Exactly where and how is it useful? Is it really a better solution or just a clever configuration of parts?" Even if you discover that your creation has no apparent utility, savor the fun you had exploring it and be thankful that you don't have the very hard work of developing it.

Creativity is not a competitive process. It is sad that we engineers are so inculcated with the competitive approach that we use it even privately. You must suspend this internal competition because almost all of your new ideas will fail. This is a fact, but it doesn't detract a bit from the fun of inventing.

Now it's time to get on to a very old and interesting analog design problem where there is still a great deal of room for invention.

Requirements for Signal Conditioning in Oscilloscopes

Most of my tenure as an electrical engineer has been spent designing analog subsystems of digital oscilloscopes. A digital oscilloscope is a rather pure and wholesome microcosm of signal processing and measurement, but at the signal inputs the instrument meets the inhospitable real world. The input signal-conditioning electronics, sometimes referred to as the "front-end" of the instrument, includes the attenuators, highimpedance buffer, and pre-amplifier. Figure 7–1 depicts a typical frontend and is annotated with some of the performance requirements.

The combination of requirements makes the design of an oscilloscope front-end very difficult. The front-end of a 500MHz oscilloscope develops nearly 1GHz of bandwidth and must have a very clean step response. It operates at this bandwidth with a $1M\Omega$ input resistance! No significant resonances are allowed out to 5GHz or so (where everything wants to resonate). Because we must maintain high input resistance and low capacitance, transmission lines (the usual method of handling microwave

Steve Roach



signals) are not allowed! The designer's only defense is to keep the physical dimensions of the circuit very small. To obtain the 1GHz bandwidth we must use microwave components. Microwave transistors and diodes are typically very delicate, yet the front-end has to withstand $\pm 400V$ excursions and high-voltage electrostatic discharges. Perhaps the most difficult requirement is high gain flatness from DC to a significant fraction of full bandwidth.

A solid grasp of the relationships between the frequency and time domains is essential for the mastery of these design challenges. In the following I will present several examples illustrating the intuitive connections between the frequency magnitude and step responses.

The Frequency and Time Domains

Oscilloscopes are specified at only two frequencies: DC and the -3dB point. Worse, the manufacturers usually state the vertical accuracy at DC only, as if an oscilloscope were a voltmeter! Why is a time domain measuring device specified in the frequency domain? The reason is that bandwidth measurements are traceable to international standards, whereas it is extremely difficult to generate an impulse or step waveform with known properties (Andrews 1983, Rush 1990).

Regardless of how oscilloscopes are specified, in actual practice oscilloscope designers concern themselves almost exclusively with the step response. There are several reasons for focusing on the step response: (1) a good step response is what the users really need in a time domain instrument, (2) the step response conveys at a glance information about a very wide band of frequencies, (3) with practice you can learn to intuitively relate the step response to the frequency response, and (4) the step

Figure 7–1. Annotated diagram

of an oscilloscope front-end, showing specifications and requirements at each stage. response will be used by your competitors to find your weaknesses and attack your product.

Figure 7–2 defines the terms of the frequency and step responses and shows the meaning of flatness error. Response flatness is a qualitative notion that refers roughly to gain errors not associated with the poles that determine the cutoff frequency, or equivalently to step response errors following the initial transition. To assess flatness we generally ignore peaking of the magnitude near the 3dB frequency. We also ignore short-term ringing caused by the initial transition in the step response.

Figure 7–2. Definition of terms and relationships between the frequency magnitude and step responses.

Figure 7–2 illustrates the rough correspondence between the highfrequency portions of the magnitude response and the early events in the step response. Similarly, disturbances in the magnitude response at low frequencies generate long-term flatness problems in the step response



(Kamath 1974). Thus the step response contains information about a very wide band of frequencies, when observed over a long enough time period. For example, looking at the first ten nanoseconds (ns) of the step conveys frequency domain information from the upper bandwidth of the instrument down to approximately 1/(10ns) or 100MHz.

Figure 7-3 shows an RC circuit that effectively models most sources of flatness errors. Even unusual sources of flatness errors, such as dielectric absorption and thermal transients in transistors, can be understood with similar RC circuit models. The attenuator and impedance converter generally behave like series and parallel combinations of simple RC circuits. Circuits of this form often create flatness problems at low frequencies because of the high resistances in an oscilloscope front-end. In contrast, the high-frequency problems are frequently the result of the innumerable tiny inductors and inadvertent transmission lines introduced in the physical construction of the circuit. Notice how in Figure 7-3 the reciprocal nature of the frequency and step responses is well represented.

High Impedance at High Frequency: The Impedance Converter

Oscilloscopes by convention and tradition have $1M\Omega$ inputs with just a few picofarads of input capacitance. The $1M\Omega$ input resistance largely determines the attenuation factor of passive probes, and therefore must be accurate and stable. To maintain the accuracy of the input resistance, the oscilloscope incorporates a very high input impedance unity gain buffer (Figure 7-1). This buffer, sometimes called an "impedance converter," presents more than $100M\Omega$ at its input while providing a lowimpedance, approximately 50Ω output to drive the pre-amp. In a 500MHz oscilloscope the impedance converter may have 1GHz of bandwidth and very carefully controlled time domain response. This section



R.C. =

C2 too big

C₂ too big



Step Response

shows one way in which these and the many additional requirements of Figure 7–1 can be met (Rush 1986).

A silicon field effect transistor (FET) acting as a source follower is the only type of commercially available device suitable for implementing the impedance converter. For 500MHz instruments, we need a source follower with the highest possible transconductance combined with the lowest gate-drain capacitance. These parameters are so important in a 500MHz instrument that oscilloscope designers resort to the use of shortchannel MOSFETs in spite of their many shortcomings. MOSFETs with short channel lengths and thin gate oxide layers develop very high transconductance relative to their terminal capacitances. However, they suffer from channel length modulation effects which give them undesirably high source-to-drain or output conductance. MOSFETs are surface conduction devices, and the interface states at the gate-to-channel interface trap charge, generating large amounts of 1/f noise. The 1/f noise can contribute as much noise between DC and 1MHz as thermal noise between DC and 500MHz. Finally, the thin oxide layer of the gate gives up very easily in the face of electrostatic discharge. As source followers, JFETs outperform MOSFETs in every area but raw speed. In summary, short-channel MOSFETs make poor but very fast source followers, and we must use a battery of auxiliary circuits to make them function acceptably in the impedance converter.

Figure 7–4 shows a very basic source follower with the required $1M\Omega$ input resistance. The resistor in the gate stabilizes the FET. Figure 7–5 shows a linear model of a typical high-frequency, short-channel MOS-FET. I prefer this model over the familiar hybrid- π model because it shows at a glance that the output resistance of the source is $1/g_m$. Figure 7–6 shows the FET with a surface-mount package model. The tiny capacitors and inductors model the geometric effects of the package and the surrounding environment. These tiny components are called "parasitics" in honor of their very undesirable presence. Figure 7–7 depicts the parasitics of the very common "0805" surface-mount resistor. This type of resistor is often used in front-end circuits built on printed circuit boards. Package and circuit board parasitics at the 0.1pF and 1nH level seem negligibly small, but they dominate circuit performance above 500MHz.





Figure 7–5. A linear model of a BSD22, a typical high-frequency, short-channel MOSFET. The gate current is zero at DC because the controlled current source keeps the drain current equal to the source current.

In oscilloscope circuits I often remove the ground plane in small patches beneath the components to reduce the capacitances. One must be extremely careful when removing the ground plane beneath a high-speed circuit, because it always increases parasitic inductance. I once turned a beautiful 2GHz amplifier into a 400MHz bookend by deleting the ground plane and thereby effectively placing large inductors in the circuit.



Figure 7-6.

A MOSFET with SOT-143 surface-mount package parasitics. The model includes the effects of mounting on a 1.6mm (0.063") thick, six-layer epoxy glass circuit board with a ground plane on the fourth layer from the component side of the board.



Figure 7-7.

A model of an 0805 surface-mount resistor, including a 1mm trace on each end. The model includes the effects of mounting on a 1.6mm (0.063") thick, six-layer epoxy glass circuit board with a ground plane on the fourth layer from the component side of the board.

Parasitics have such a dominant effect on high-frequency performance that 500MHz oscilloscope front-ends are usually built as chip-and-wire hybrids, which have considerably lower parasitics than standard printed circuit construction. Whether on circuit boards or hybrids, the bond wires, each with about 0.5 to 1.0nH inductance, present one of the greatest difficulties for high-frequency performance. In the course of designing high-frequency circuits, one eventually comes to view the circuits and layouts as a collection of transmission lines or the lumped approximations of transmission lines. I have found this view to be very useful and with practice a highly intuitive mental model.

Figure 7–8 shows the magnitude and step responses of the simple source follower, using the models of Figures 7–5 through 7–7. The bandwidth is good at 1.1GHz. The rise time is also good at 360ps, and the 1% settling time is under 1ns!

Our simple source follower still has a serious problem. The high drain-to-source conductance of the FET forms a voltage divider with the source resistance, limiting the gain of the source follower to 0.91. The pre-amp could easily make up this gain, but the real issue is temperature stability. Both transconductance and output conductance vary with temperature, albeit in a self-compensating way. We cannot comfortably rely on this self-compensation effect to keep the gain stable. The solution is to bootstrap the drain, as shown in Figure 7–9. This circuit forces the drain and source voltages to track the gate voltage. With bootstrapping, the source follower operates at nearly constant current and nearly constant terminal voltages. Thus bootstrapping keeps the gain high and stable, the power dissipation constant, and the distortion low.

There are many clever ways to implement the bootstrap circuit (Kimura 1991). One particularly simple method is shown in Figure 7–10. The BF996S dual-gate, depletion-mode MOSFET is intended for use in television tuners as an automatic gain controlled amplifier. This device acts like two MOSFETs stacked source-to-drain in series. The current source shown in Figure 7–10 is typically a straightforward bipolar transistor current source implemented with a microwave transistor. An ap-



Time

proximate linear model of the BF996S is shown in Figure 7–11. The BF996S comes in a SOT-143 surface-mount package, with parasitics, as shown in Figure 7–6.

Figure 7-12 shows the frequency and step responses of the bootstrapped source follower. The bootstrapping network is AC coupled, so





Figure 7–9. The bootstrapped source follower. Driving the drain with the source voltage increases and stabilizes the gain.



it does not boost the gain at DC and low frequencies. The response therefore is not very flat, but we can fix it later. From 1kHz to 100MHz the gain is greater than 0.985 and therefore highly independent of temperature. The 1% settling time is very good at 1.0ns.

Several problems remain in the bootstrapped source follower of Figure 7–10. First, the gate has no protection whatever from overvoltages and electrostatic discharges. Second, the gate-source voltage will vary drastically with temperature, causing poor DC stability. Third, the 1/f noise of the MOSFET is uncontrolled. The flatness (Figure 7–12) is very poor indeed. Finally, the bootstrapped source follower has no ability to handle large DC offsets in its input.

Figure 7–13 introduces one of many ways to build a "two-path" impedance converter that solves the above problems (Evel 1971, Tektronix 1972). DC and low frequencies flow through the op amp, whereas high frequencies bypass the op amp via C1. At DC and low frequencies, feed-



Figure 7–11. Linear model of the BF996S dual-gate, depletion MOSFET.