A Designers Guide for the HA-5033 Video Buffer

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Introduction

Intersil Corporation is an industry leader in the high speed, wideband, monolithic operational amplifier market. Due to the high performance of Intersil products, designers in the more specialized areas of electronics have shown interest in utilizing these products in their applications. One such area is video design. In an effort to address this market, Intersil has introduced the HA-5033 video buffer.

This paper will discuss the HA-5033 design and provide additional performance characteristics not shown in the data sheet.

HA-5033 Description

The HA-5033 is a unity gain monolithic IC designed for any application requiring a fast wideband buffer. A voltage follower by design, this product is optimized for high speed 50Ω and 75Ω coaxial cable driver applications common in color video systems.

Critical performance characteristics are summarized in Table 1. Outstanding differential phase/gain characteristics combined with an output current capability of ±100mA makes the HA-5033 an excellent choice for the line driver applications required in video circuit design.

TABLE 1. HA-5033 SPECIFICATIONS: T_A = 25°C; V_{SUPPLY} = ±12V (UNLESS OTHERWISE SHOWN)

PARAMETER	MIN	TYP	MAX	UNITS
Input Offset Voltage			15	mV
Input Bias Current			35	µA
Differential Phase		0.1		Degree
Differential Gain		0.1		%
Slew Rate (±15V)	1000			V/µs
Output Current		±100		mA
Bandwidth (Small Signal)		250		MHz
Bandwidth (V_{IN} = 1V_{RMS})		65		MHz
Supply Current			20	mA

Other features, which include a minimum slew rate of 1000V/µs, make the HA-5033 useful in high speed A/D data conversion and sample/hold circuits.

The HA-5033 is offered in three package configurations: the 12 lead metal can, the 8 lead PDIP, and the 8 lead Power Small Outline Package (PSOP). The pinouts for each package are illustrated in Figure 1.

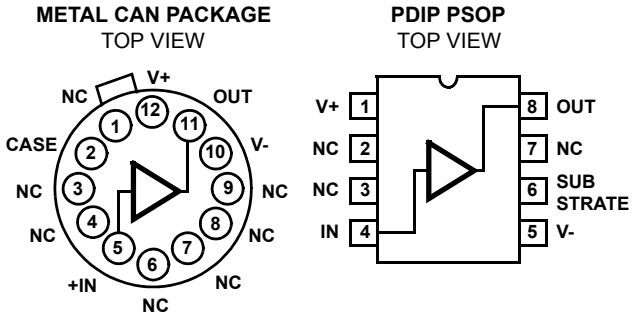


FIGURE 1. HA-5033 PINOUTS: METAL CAN-PIN COMPATIBLE WITH THE LH0033 HYBRID. 8-LEAD, PDIP-FABRICATED USING A COPPER LEAD FRAME. ADVANTAGES INCLUDE EXCELLENT THERMAL CHARACTERISTICS AND BOARD SPACE SAVINGS.

The high performance of this product (summarized in Table 1) is the result of the Intersil High Frequency Dielectric Isolation Process. A major feature of this process is that it provides both PNP and NPN high frequency transistors which make wide bandwidth designs, such as the HA-5033, practical.

A Closer Look

Most manufacturer's data sheets provide a schematic diagram and depending upon the complexity of the product, this schematic may be comprehensive or possibly a simplified version. Schematics are a visual means of presenting information, ranging from reliability data, such as transistor counts, to circuit information for circuit analysis or computer simulation. But the most important reason for the schematic is to communicate to the customer the internal structure of the product and therefore, some insight into its operation.

At first glance, a schematic may appear as nothing more than a collection of resistors and transistors. But upon closer examination, particular areas of operation should become evident. Using the HA-5033 as an example (Figure 2), it will be shown that the HA-5033 consists of a signal path, bias network, and performance optimization circuitry.

Signal buffering is accomplished by cascading two emitter followers. In order to achieve symmetrical positive and negative output drive capability, two pairs are paralleled. The first pair consists of Q_1 and Q_4 for positive drive while the second pair Q_2, Q_3, provide negative drive. The emitter resistors of Q_1, Q_2 ensure stability with respect to load resistance, enhance differential phase/gain performance, and stabilize the quiescent operating point. This signal path has been highlighted on the schematic.

The bias circuitry consists primarily of the diode-biasing located on the left portion of the schematic along with transistors Q_5, Q_6. This circuitry ensures the designed performance of the other active elements.

The performance optimization circuits are a slew enhancement circuit and a bias network buffer circuit. The transistors Q_7, Q_8, Q_9 and Q_{10} are for slew enhancement. If the input voltage exceeds the output by one V_{BE}, Q_7 will turn on Q_{10}, which in turn provides extra base drive to Q_1. Similarly, Q_9 will supply extra base drive to Q_2.

Transistors Q_{11}, Q_{12}, Q_{13} and Q_{14} prevent high frequency or transient signals from affecting the bias circuitry. This prevents C_{CB} multiplication of current sources Q_5 and Q_6, which also improves differential gain/phase performance.

Note that output current limiting was not designed into the HA-5033. If there is a possibility of the output being shorted to ground or the supplies, external current limiting will be necessary.

Any designer interested in using the HA-5033 should be aware of a characteristic related to output transistor operation. As the data sheet performance curves (reproduced in Figure 3) show, the output swing is a function of frequency. These curves show the point at which observable distortion occurs for a given frequency. However, if the signal amplitude, signal frequency or both are increased beyond the curves shown, thermal “runaway” will occur. This is due to both the NPN and PNP output transistors approaching a condition of being simultaneously on. This condition has been computer simulated and the results are shown in Figure 4.

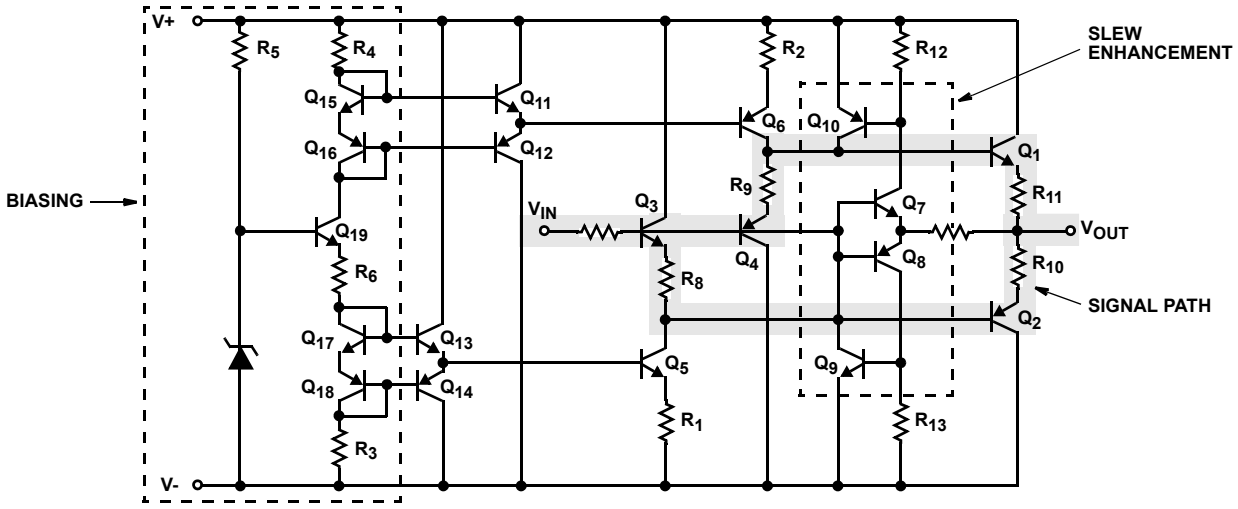


FIGURE 2. HA-5033 SCHEMATIC: VIDEO BUFFER DESIGN CONSISTS OF THREE OPERATING AREAS; SIGNAL PATH, BIAS NETWORK AND PERFORMANCE OPTIMIZATION CIRCUITRY.

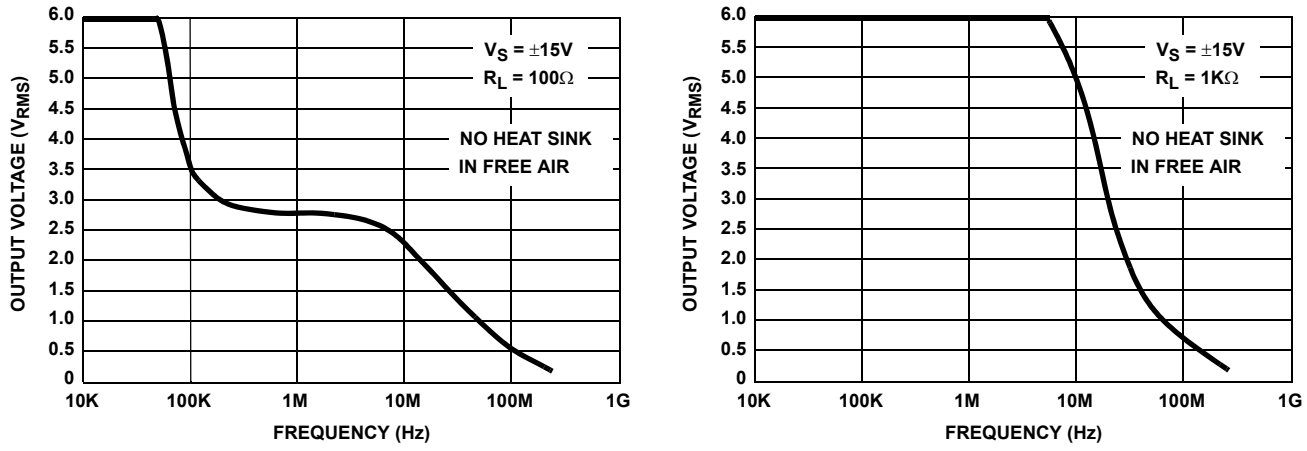


FIGURE 3. OUTPUT SWING vs FREQUENCY PERFORMANCE CURVES: CURVES SHOW POINT OF OBSERVABLE DISTORTION FOR GIVEN FREQUENCY. OPERATION BEYOND THE CURVES SHOWN WILL APPROACH CONDITIONS WHERE OUTPUT TRANSISTORS ARE SIMULTANEOUSLY ON. THE RESULTING INCREASE IN CHIP TEMPERATURE WILL LEAD TO THERMAL RUNAWAY.

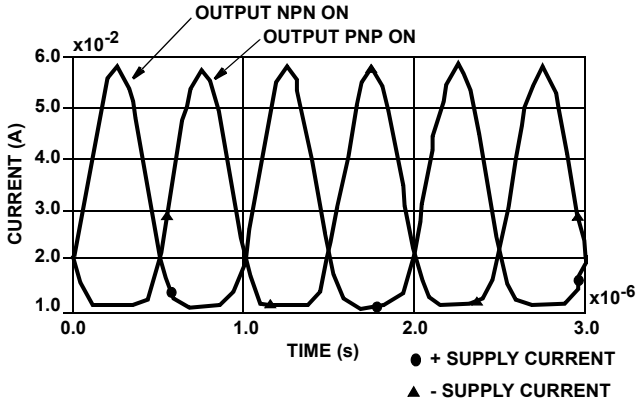


FIGURE 4A. V_{PEAK} = 5V, R_L = 100

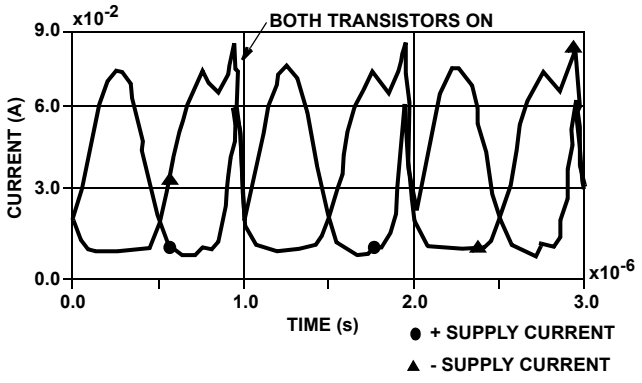


FIGURE 4B. V_{PEAK} = 7V, R_L = 100

FIGURE 4. OUTPUT TRANSISTOR COMPUTER SIMULATION RESULTS

This condition occurs if the frequency of the analog signal does not allow sufficient time for the output PNP transistor to turn off. The frequency which causes this “push-push” output stage can be determined by using the following relationship,

$$\text{Full Power Bandwidth (FPBW)} = \frac{SR}{2\pi V_{PEAK}}$$

Where: SR = Slew Rate
V_{PEAK} = Analog Signal Peak Voltage

Therefore, the designer can determine the approximate frequency of thermal runaway by supplying the peak analog voltage and measuring the buffer slew rate for a particular application.

For example, the slew rate for the HA-5033 with a load of R_L = 1kΩ and C_L = 1000pF was measured to be 83V/µs. The FPBW for a $5V_{PEAK}$ analog signal was calculated,

$$FPBW = \frac{83V/\mu s}{2\pi(5V)} = 2.6MHz$$

So the estimated frequency of thermal runaway for the given conditions is 2.6MHz. Measurements in the lab resulted in a thermal runaway frequency equal to 2.5MHz.

Although the FPBW relationship gives the designer a method of estimating the frequency of thermal runaway, it is recommended that the HA-5033 be operated to the left of the curves shown in Figure 3. Heat sinking the buffer will not prevent this condition from occurring.

The purpose of heat sinking a semiconductor is to maintain the device junction temperature below a specified maximum limit. This is a thermal problem and can be evaluated using the thermal analog of Ohm’s Law illustrated in Figure 5.

Where:

P_{DMAX} = Power Dissipated (P_{DC} + P_{AC}), Watts
T_J = Maximum Junction Temperature, ^oC
T_A = Ambient Temperature, ^oC
θ_{JC} = Junction to Case Thermal Resistance, $^oC/W$
θ_{CS} = Case to Heat Sink Thermal Resistance, $^oC/W$
θ_{SA} = Heat Sink to Ambient Thermal Resistance, $^oC/W$

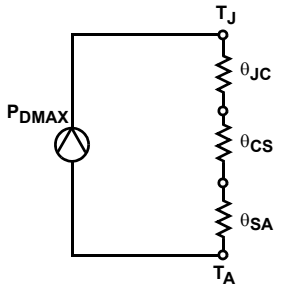


FIGURE 5. THERMAL ANALOG OF OHM’S LAW: SEMICONDUCTOR/HEAT SINK SYSTEM

In this thermal system, current is replaced by power, voltage by temperature, and electrical resistance by thermal resistance. By using Figure 5, the following expression is derived,

$$P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

This expression allows the designer to determine the maximum power dissipation of a semiconductor/heat sink system.

The expression for the semiconductor in free air is,

$$P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}}$$

In order to make use of these expressions, the following information is required. θ_{JC} and T_{JMAX}, from the semiconductor manufacturer and θ_{CS} and θ_{SA}, from the heat sink manufacturer.

For the HA-5033, the maximum junction temperature (T_{JMAX}) is 175^{o}C for the metal can package, and 150^{o}C for the PDIP and PSOP packages. The thermal impedances for the HA-5033 in the metal can package are θ_{JA} = 65^{o}C/W and θ_{JC} = 34^{o}C/W. The PDIP thermal resistance is θ_{JA} = 96^{o}C/W, while the PSOP package has θ_{JA} = 129^{o}C/W. These values have been used to generate the “Maximum Power Dissipation” graph in Figure 6.

Recommended heat sinks for the HA-5033 in the metal can package are the Thermalloy 2240A [1] and IERC-UP-T08-51CB [2] (base), IERC-UP-C7 (top). Thermal impedances are

θ_{SA} = 27°C/W and θ_{SA} = 10°C/W, respectively. θ_{CS} is dependent upon the type of insulator or thermal joint compound used. Both products are two piece heat sinks, but differ in design.

By using the given product information and supplying an operating ambient temperature, the designer can determine the maximum power the system will dissipate and not exceed the maximum junction temperature.

For example, Figure 6 shows the maximum power dissipation for the HA-5033 in a metal can package to be 2.31W at 25°C.

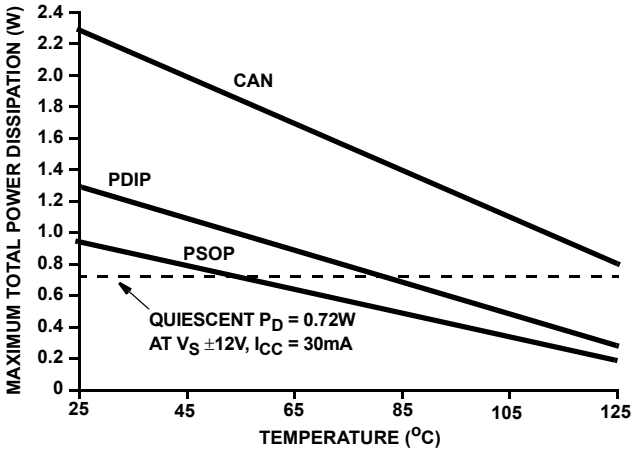


FIGURE 6. HA-5033 MAXIMUM POWER DISSIPATION VS AMBIENT TEMPERATURE: FREE AIR

The maximum power dissipation of the HA-5033/2240A metal can/heat sink system is calculated to be,

$$P_{DMAX} = \frac{175 - 25}{34 + 27} = 2.46$$

Therefore, the HA-5033 used with the Thermalloy 2240A can dissipate 2.46W at 25°C and not exceed the maximum junction temperature of 175°C.

The power dissipation limits shown in Figure 6 and those determined with the heat sink apply for both quiescent and load related power. Therefore,

$$P_{DMAX} \leq P_{DC} + P_{AC}$$

$$P_{DC} = (V+)(+I) + (V-)(-I)$$

$$P_{AC} = (1/T)_O \int T\ v(t)\ i(t)\ dt$$

Video Performance

The images which appear on your television picture tube are created by a process called scanning [3]. Scanning is a method of recreating the optical image of a scene one line at a time. Referring to Figure 7A, an electron beam moves or “scans” from left to right and quickly returns to a position below its starting spot. This process continues until the bottom of the picture is reached and the beam returns to the original top left hand position. This method is called sequential scanning.

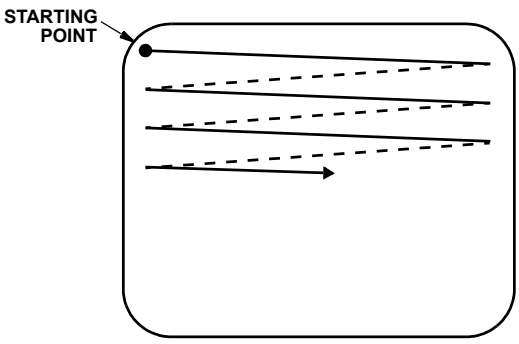


FIGURE 7A. SEQUENCIAL SCANNING

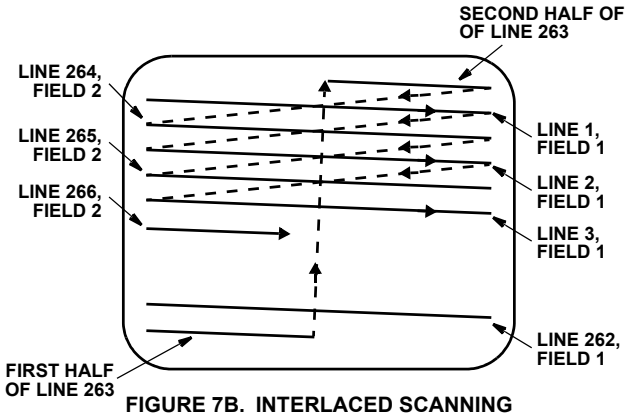


FIGURE 7B. INTERLACED SCANNING

FIGURE 7. SCANNING SEQUENCE

Incorporated into present television broadcast standards is a technique called interlaced scanning. Interlaced scanning recreates the scene by providing two half scans. As shown in Figure 7B, the first scan traces out the odd numbered lines, the second scan fills in the even numbered lines. This technique avoids the flicker problem and excessive bandwidths required for similar picture definition using sequential scanning.

The United States NTSC (National Television Systems Committee) broadcast standard is a 525 line standard. Each scan consists of 2621/2 lines. The first scan is known as field one, the second, field two. Therefore, the complete picture consists of two fields.

The first 21 lines of each field are blank. Those lines are left open and are not used to broadcast video information. Instead, these lines contain other important information, such as sync pulses, data transmission, and test signals. The test signals contained in these lines are called the Vertical Interval Test Signals (VITS) [4, 5], which allows realtime monitoring of the television broadcast signal quality. These test signals were used to evaluate the video performance of the HA-5033.

Four test signals are commonly used in the vertical interval. They are the multiburst, color bar, composite and vertical interval reference. These test signals are shown in Figures 8 through 11.

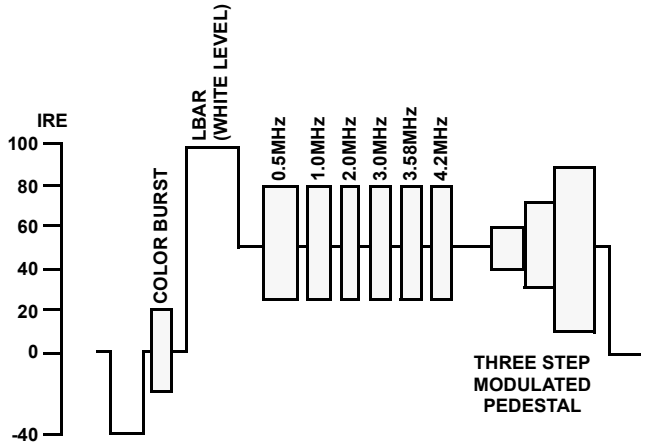


FIGURE 8. MULTIBURST SIGNAL (FIELD 1, LINE 17) ALLOWS FREQUENCY RESPONSE CHECKS

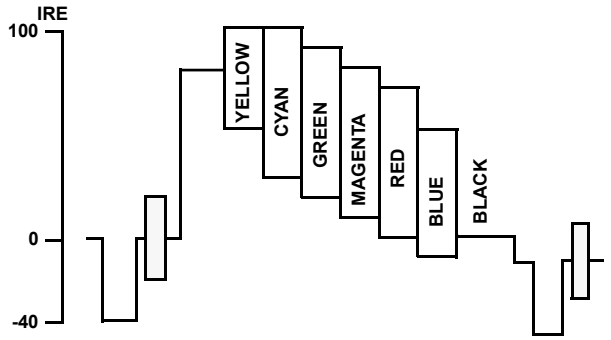


FIGURE 9. COLOR BAR (FIELD 2, LINE 17) ENABLES MONITORING OF COLOR TRANSMISSION QUALITY

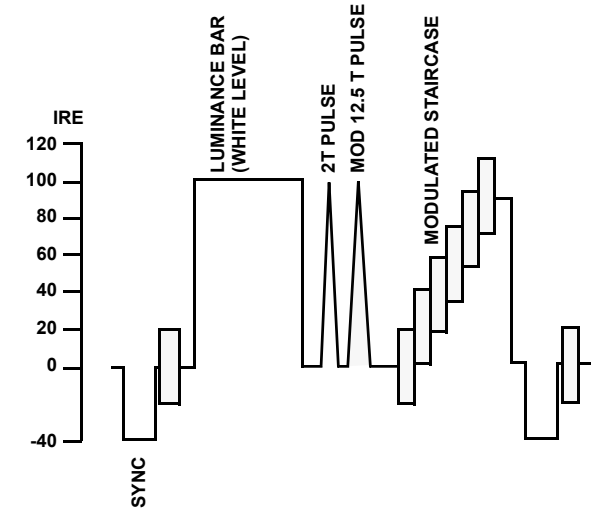


FIGURE 10. COMPOSITE SIGNAL (FIELD 1, AND 2, LINE 18) DESIGNED FOR GAIN AND TIME DELAY TESTS

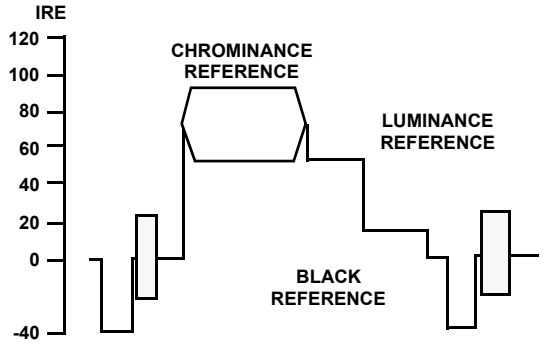
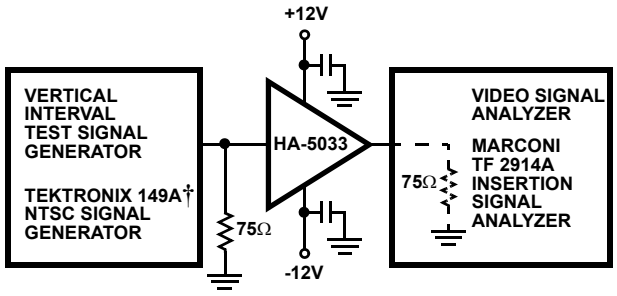


FIGURE 11. VERTICAL INTERVAL REFERENCE SIGNAL (FIELD 1 AND 2, LINE 19) PROVIDES COLOR AND GAIN REFERENCES

Each test signal was created to allow various distortions to be measured without interfering with the normal video transmission. These signal distortions which exist in television systems are defined as linear or non-linear. Non-linear distortion, such as differential phase and gain, vary with the amplitude of the picture signal. Linear distortions, usually dependent upon frequency response, are independent of signal level. For example, the multiburst test signal is very useful for frequency response checks, whereas the composite signal contains signals for checking gain error.

Determining the HA-5033's performance level with respect to the NTSC standard required the definition of a measurement method. Test equipment was needed that would produce the necessary NTSC test signals and also monitor the device under test performance. The test configuration, shown in Figure 12 consisted of a Tektronix 149A NTSC [6] generator and Marconi TF 2914A video analyzer [7].



†TEKTRONIX 1910 NTSC DIGITAL GENERATOR RECOMMENDED

FIGURE 12. HA-5033 NTSC PERFORMANCE TEST CONFIGURATION

The TF 2914A has the capability of measuring 24 separate video parameters. Other advantages include direct readout and much more accuracy than possible using scope methods. Table 2 lists the video parameters tested on the HA-5033 along with the particular VITS utilized by the TF 2914A.

TABLE 2. TF 2914A VIDEO MEASUREMENT PARAMETERS REFERRED TO VERTICAL INTERVAL TEST SIGNALS

VIDEO PARAMETER	VERTICAL INTERVAL TEST SIGNAL USED
Luminance Bar Amplitude	Luminance Bar, Composite Signal (Figure 10)
Sync Amplitude	Sync Pulse, Composite Signal (Figure 10)
2T Pulse to Bar Ratio	2T Pulse/Luminance Bar, Composite Signal (Figure 10)
Chrominance to Luminance Gain Inequality	Chrominance Component Amplitude of the 12.5T Pulse and Luminance Components of the 12.5T Pulse, Composite Signal (Figure 10)
Chrominance to Luminance Delay	Time Difference of Chrominance and Luminance Components of the 12.5T Pulse, Composite Signal (Figure 10)
Luminance Non-Linearity	Largest and Smallest Step Amplitude of the Modulated Step Staircase, Composite Signal (Figure 10)
Signal to Noise Ratio	Luminance Bar Level to Noise Voltage, Composite Signal (Figure 10)
Chrominance to Luminance Crosstalk	Chrominance Component of 3 Step Modulated Pedestal and Luminance Bar, Multiburst Signal (Figure 8)
Low Frequency Error	Amplitude of Low Frequency Signals
Bar Tilt	Difference of Luminance Bar Amplitude, Composite Signal (Figure 10)
2T K Factor	2T Pulse, Composite Signal (Figure 10)
Differential Gain	Amplitude Deviation of Modulated Step Staircase, Composite Signal (Figure 10)
Differential Phase	Phase Deviation of Modulated Step Staircase, Composite Signal (Figure 10)
Flag	Luminance Amplitude, Multiburst Signal (Figure 8)
Multiburst 1-6	Amplitude of Each Frequency Burst, Multiburst Signal (Figure 8)
Color Reference Burst Amplitude	Color Burst Amplitude, Multiburst Signal (Figure 8)

Since the TF 2914A measurement includes any inaccuracies of the NTSC signal generator, a “delta” measurement was neccesary. The NTSC generator was connected directly to the analyzer and the results recorded. Next, the HA-5033 was inserted and the results recorded. The difference between the two readings was considered the actual HA-5033 performance. Table 3 lists the video performance results of the HA-5033.

TABLE 3. HA-5033 NTSC VIDEO PERFORMANCE

VIDEO PARAMETER	HA-5033	UNITS
Luminance Bar Amplitude	93.6	IRE (Note)
Sync Amplitude	37.5	IRE
2T Pulse to Bar Ratio	99.9	IRE
Chrominance to Luminance Gain Inequality	99.9	IRE
Chrominance to Luminance Delay	1.5	ns
Luminance Non-Linearity	0.1	%
Signal-to-Noise Ratio	66	dB
Chrominance to Luminance Crosstalk	51.6	IRE
Low Frequency Error	0.3	mV
Bar Tilt	0.3	IRE
2T K Factor	0.1	K
Differential Gain	0.1	%
Differential Phase	0.1	Degree
Flag	99.5	IRE

TABLE 3. HA-5033 NTSC VIDEO PERFORMANCE (Continued)

VIDEO PARAMETER	HA-5033	UNITS
Multiburst 1 Amplitude	49.2	IRE
Multiburst 2 Amplitude	49.3	IRE
Multiburst 3 Amplitude	51.0	IRE
Multiburst 4 Amplitude	50.4	IRE
Multiburst 5 Amplitude	49.7	IRE
Multiburst 6 Amplitude	50.0	IRE
Color Reference Burst Amplitude	40.4	IRE

NOTE: IEEE Standard 205-1958 defines the levels of television video signal in terms of IRE units. 100 IRE units = 0.714V_{P-P}.

Applying the HA-5033

The most important consideration when designing with the HA-5033 is layout. The wide bandwidth of the buffer necessitates that high frequency layout procedures be followed. Recommended procedures include the use of a ground plane, minimization of all lead lengths, avoiding sockets, and proper power supply decoupling.

Standard practice in RF/Video layout is the use of a ground plane. A ground plane minimizes distributed circuit capacitance and inductance which degrade high frequency performance. The ground plane can also incorporate the metal case of the HA-5033, since pin 2 is internally tied to the package. This feature allows the user to make contact between the ground plane and the package which extends shielding, provides additional heat sinking and eliminates the use of a socket. IC sockets contribute bandwidth limiting interlead capacitance and should be avoided.

For the PDIP, additional heatsinking can be derived from soldering the no connection leads 2, 3, and 7 to the ground plane. Also, lead 6 can be tied to either supply, grounded or left open. But to optimize device performance and improve isolation, it is recommended that this pin be grounded.

Another method of enhancing device performance is power supply decoupling. For the HA-5033, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1mF will minimize high frequency variations in supply voltage. Solid tantalum capacitors 1mF or larger will optimize low frequency performance. It is also recommended that the bypass capacitors be connected as close to the HA-5033 as possible, preferably directly to the supply pins.

Finally, keeping all lead lengths as short as possible will minimize distributed capacitance and reduce board space. It is essential that the guidelines discussed above be followed to avoid marginal performance.

Another consideration when applying the HA-5033 is load capacitance. Although the HA-5033 is designed to handle load capacitance values up to 0.01μF, it has a worst case stability region in the area of 50pF. The computer simulation of the HA-5033 frequency response in Figure 13 illustrates the gain peaking which occurs in the 150MHz region.

There are three suggested methods of dealing with this particular characteristic of the HA-5033. Isolating the load capacitance from the buffer output is the object of the first method. This is accomplished by placing a series resistor between the output and the load.

A second technique utilizes the HA-5033 frequency response with respect to load capacitance. Referring once again to Figure 13, notice that the gain peaking is removed with additional load capacitance. This is the basis of method two, adding additional load capacitance to approach a region of stability.

A drawback to adding more load capacitance is that the buffer's dynamic characteristic will degrade and bandwidth performance will be less than data sheet specifications. The third method solves this trade-off by using a “bootstrap” technique of adding capacitance from input to output. This method achieves stability without sacrificing performance.

An explanation of why adding capacitance will stabilize the HA-5033 can be found in the Y parameter data shown in Figure 14. The expression for the buffer gain in terms of Y parameter is:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{-Y_{21}}{Y_{22} + Y_L}$$

Y_{21} = Forward Transmittance

Y_{22} = Output Admittance

Y_L = Load Admittance

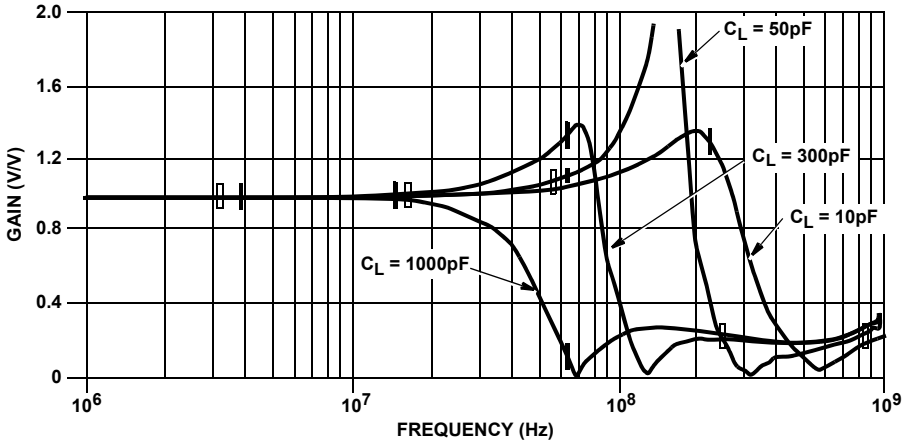


FIGURE 13. COMPUTER SIMULATION OF HA-5033 GAIN CHARACTERISTICS vs FREQUENCY AND LOAD CAPACITANCE

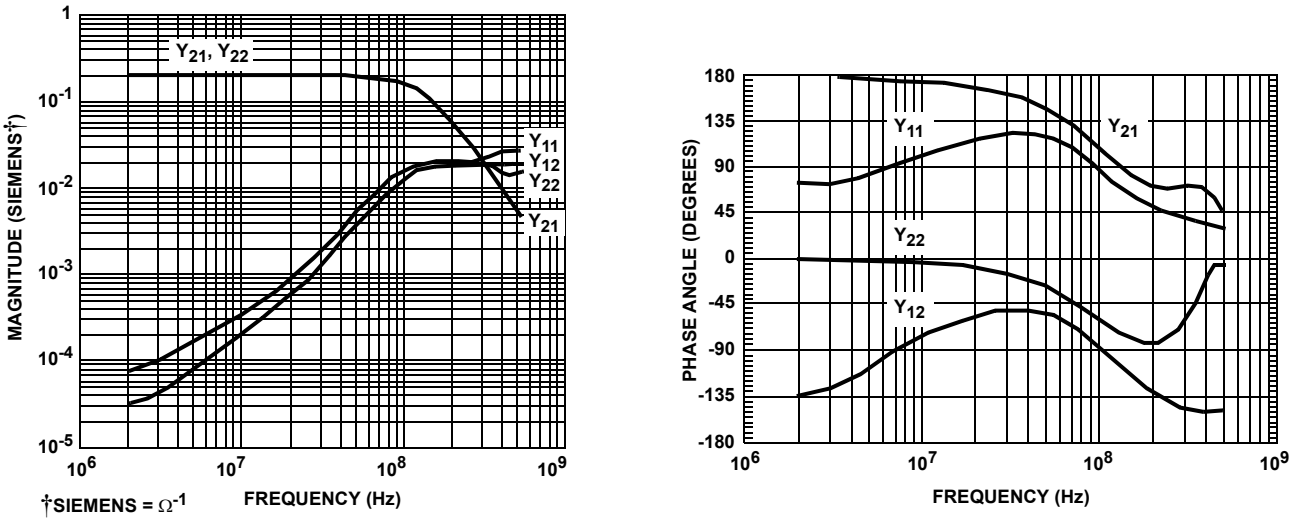


FIGURE 14. HA-5033 Y PARAMETER DATA

Notice that the output admittance, Y_{22}, phase becomes inductive ($-jY_L = -90^o$) at high frequency. So if the load, Y_L, is capacitive ($+jY_C = +90^o$) and the sum of $Y_{22} + Y_L$, become small, peaking occurs. Adding additional capacitance changes the effective phase angle and peaking can be reduced.

Using the HA-5033 as the analog input buffer of a flash converter is an example of an application where the suggested stabilization methods are useful. Although it has been stressed to keep all distributed capacitance to a minimum to optimize device operation, the load which a flash converter presents to the buffer represents a greater concern.

Flash or parallel converters are a special case, since the analog input circuit must drive a non-linear input impedance [8]. This non-linearity is due to the potential input impedance changes of the 255 parallel comparators which comprise the converter analog input. In addition to the non-linearity, the input capacitance of these converters tends to be relatively large, 100-300pF.

Examples of the various stabilization methods tested with the TRW 1007 8-bit video flash converter are shown in Figure 15. Figure 15A illustrates the series resistor method, Figure 15B is the load capacitance method, and Figure 15C is the bootstrap method. Photographs of the experimental results show the analog input sampling convert signal (pin 30), the MSB digital output (D1, pin 40), and the buffer output (converter input).

It is recommended that a complete evaluation for each method be conducted to determine the optimum component values. The value of the series resistor will depend upon the input capacitance of the particular converter used. A suggested starting value is 50Ω. With the capacitance methods, the distributed capacitance of the layout will affect component values. These experimental results were obtained using C = 240pF.

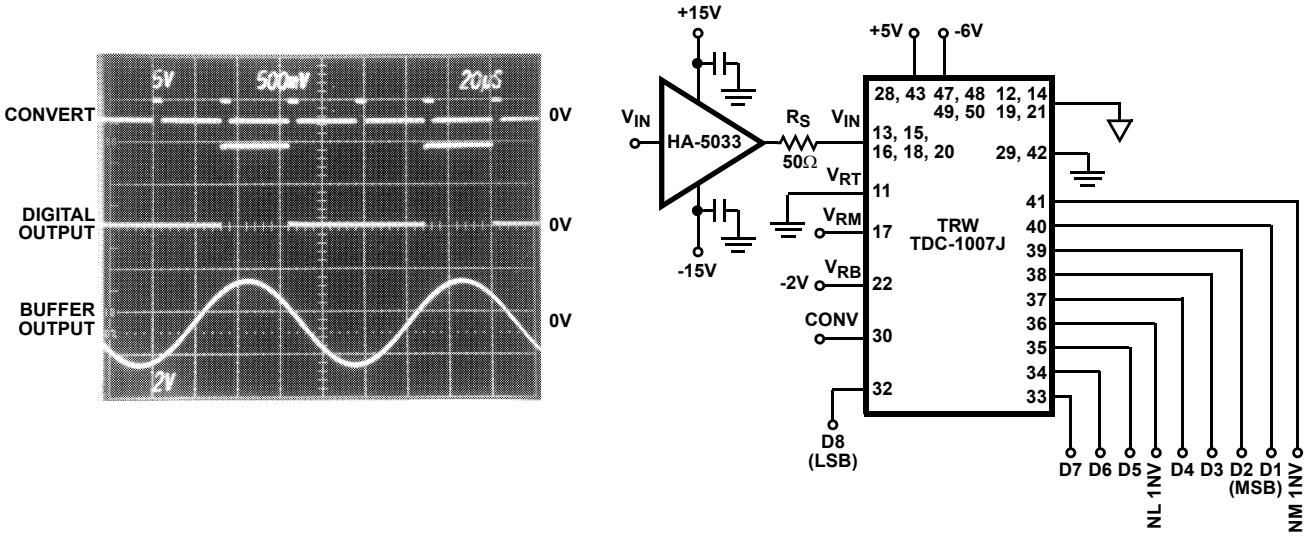


FIGURE 15A. ENHANCING 5033 PERFORMANCE IN FLASH CONVERTER APPLICATIONS: SERIES RESISTOR METHOD

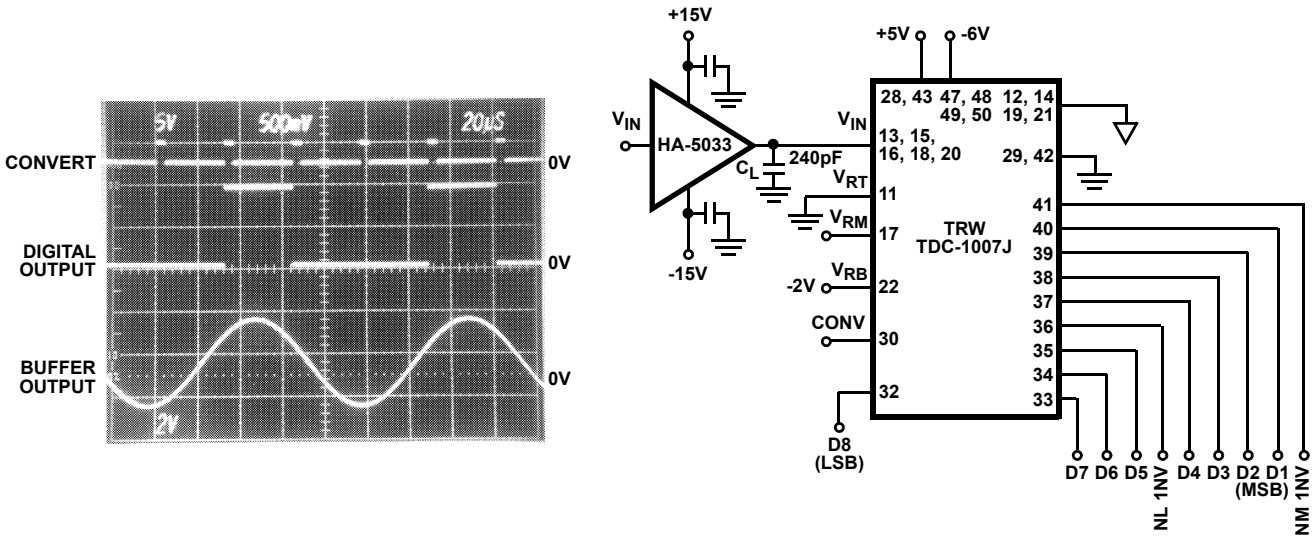


FIGURE 15B. LOAD CAPACITANCE METHOD

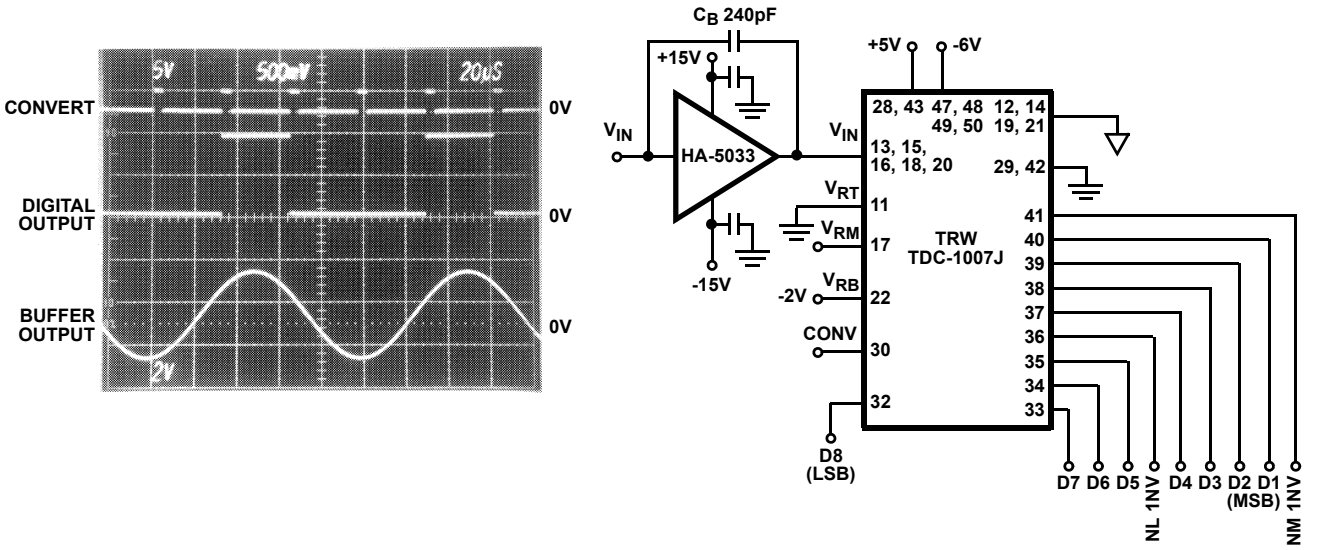
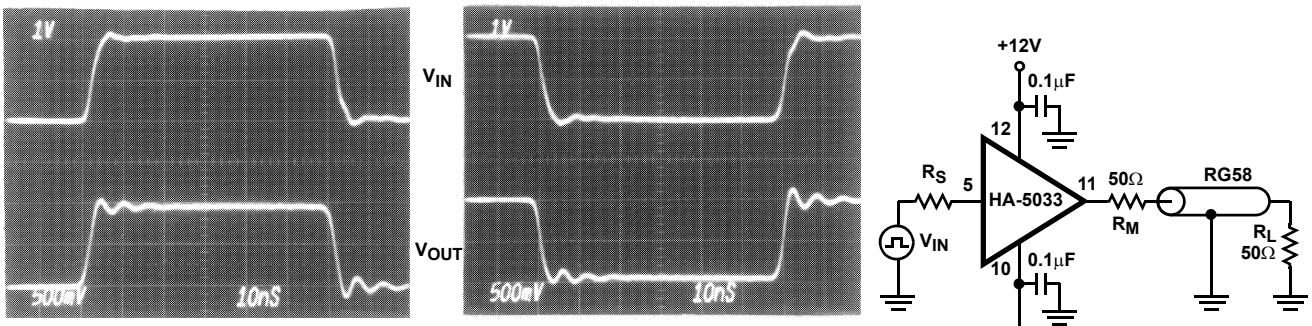


FIGURE 15C. BOOTSTRAP CAPACITANCE METHOD



POSITIVE PULSE RESPONSE
$T_A = 25^oC$
$R_S = 50\Omega$
$R_M = R_L = 50\Omega$

$$V_O = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = 1/2V_{IN}$$

NEGATIVE PULSE RESPONSE
$T_A = 25^oC$
$R_S = 50\Omega$
$R_M = R_L = 50\Omega$

$$V_O = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = 1/2V_{IN}$$

FIGURE 16. VIDEO COAXIAL LINE DRIVER - 50Ω SYSTEM

The signal levels in most video applications are $1V_{P-P}$ or less. Although the HA-5033 was shown with ±15V power supplies in the converter applications, lower power supplies will accommodate these video signal levels. For example, at ±5V power supplies, the HA-5033 can swing ±2V into a 75Ω load.

The HA-5033 is an excellent high speed line device capable of driving 50Ω and 75Ω coaxial cable.

These types of drive requirements are common in video circuit design. Figures 16 and 17 illustrate two typical application examples. Figure 16 is an example of a 50Ω system using the HA-5033 alone. R_M matches the buffer output impedance to the cables characteristic impedance. Depending upon the response required, this resistor may not be necessary. If used, the output voltage will be one-half the input voltage.

Figure 17 illustrates the use of the buffer within the feedback loop of an operational amplifier. This configuration provides additional output current capability for the HA-2539 op amp and gives the designer voltage gain control.

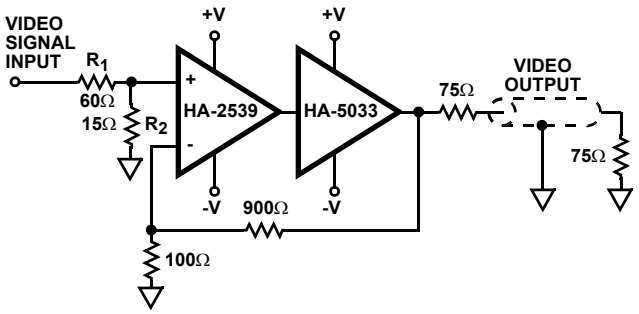


FIGURE 17. VIDEO GAIN BLOCK

Another application which utilizes the HA-5033's output drive capability is the high speed sample and hold circuit shown in Figure 18. The input buffer provides drive current to the hold capacitor while the output buffer functions as a data line driver.

The switching element in this application is the HI-201HS high speed CMOS switch which contributes it's own benefits to the application [9]. Depending upon the application requirements, using the HA-5033 as the output buffer in Figure 18A may not be acceptable. Lab tests have shown that the input bias current of the HA-5033 becomes a factor for low values of hold capacitance (<0.01μF) during the hold mode.

A solution is to add a low bias current FET input stage, as shown in Figure 18B. Q_1 acts as a voltage follower and Q_2 is a current source. Matching Q_1, Q_2 and R_1, R_2 are important considerations in order to minimize offset voltages.

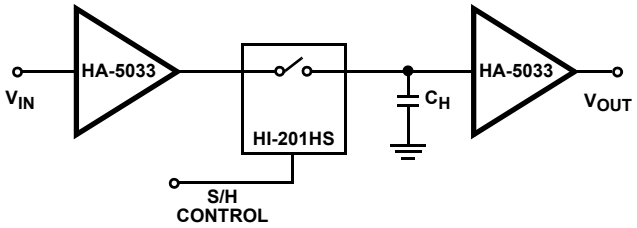


FIGURE 18A. HIGH SPEED SAMPLE/HOLD

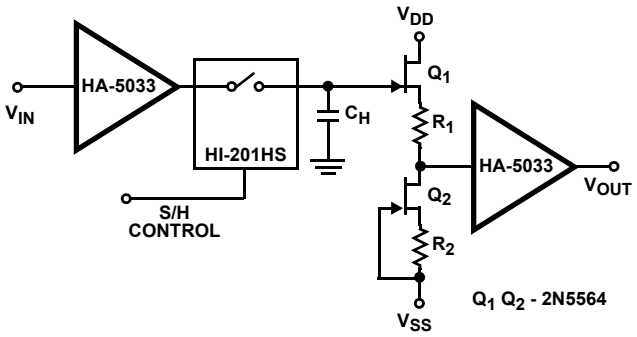


FIGURE 18A. MODIFIED OUTPUT BUFFER

When the drive capability of the HA-5033 is insufficient, consider adding an external output stage. Figure 19A illustrates an example where a push-pull complementary output stage has been added to the HA-5033. Although unable to drive the low impedances of speakers, typically 4Ω to 8Ω, the buffer can be used to drive audio output transistors. A variation of this configuration is shown in Figure 19B, where separate buffers individually drive each transistor base. A low noise input stage is provided by the HA-5102.

A common method of achieving an audio oscillator circuit is to use a transistor or IC amplifier with LC or RC feedback. An alternative technique of generating sinusoidal waveforms, using the HA-5033, is shown in Figure 20. Crystal oscillators offer improved frequency stability over time and temperature. This particular oscillator configuration [10] produces an 18.18MHz, 2.8V_{P-P} sinusoidal waveform into a 1kΩ load.

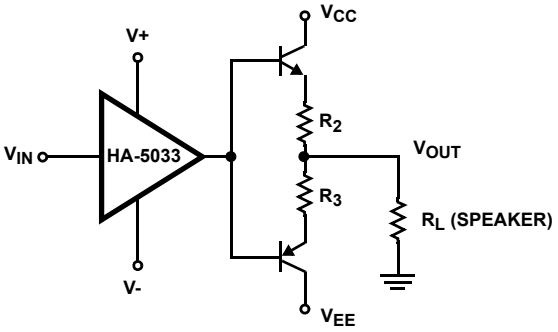


FIGURE 19A.

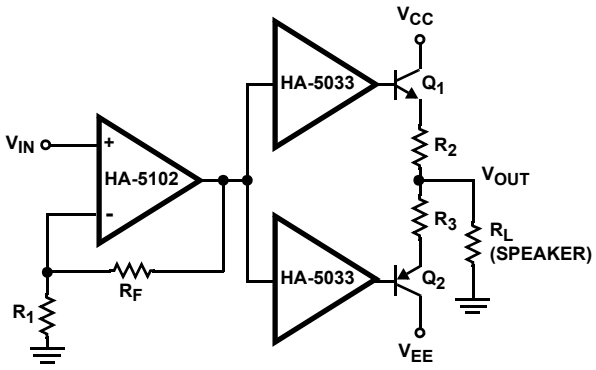


FIGURE 19B.
FIGURE 19. AUDIO DRIVERS

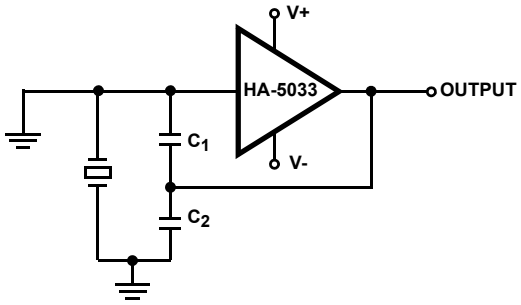


FIGURE 20. CRYSTAL OSCILLATOR: V_S = ±15V, C_1 = 12pF, C_2 = 39pF, 18MHz QUARTZ CRYSTAL

Conclusion

The HA-5033 is a high performance integrated circuit presently being utilized in a wide variety of applications. This paper has provided additional information to aid designers in applying the HA-5033 video buffer in future applications.

References

[1] Thermalloy Semiconductor Accessories Catalog, Thermalloy Inc.; Dallas, Texas.

[2] Heat Sink/Dissipator Products and Thermal Management Guide, International Electronic Research Corp.; Burbank, California

[3] William L. Hughes, “Television Fundamentals and Standards”, Electronic Engineers Handbook ed.; Donald G. Fink (McGraw-Hill, 1975) p. 20-3

[4] “VITS Analysis for TV Screening”, Tektronix Application Note #T900, 1978

[5] “Video Facility Testing/Technical Performance Objectives”, NTC Report No. 7, Published by the Public Broadcasting Service for the NTC, 1976.

[6] Tektronix 1984 Product Catalog.

[7] Marconi Instruments 1983-84 Product Catalog.

[8] “Monolithic Video A/D Converter”, TRW TDC1007J Data Sheet, 1978.

[9] “New High Speed Switch Offers Sub-50ns Switching Time” Intersil Application Note 543,1983.

[10] Tor Hougen, “Keep Your Oscillator Simple”, EDN, June, 1984, p. 236-238.

Further Reading

1. “TV/Video Sync Primer”, Hewlett-Packard Product Note 005-1,1981.
2. Stu Rasmussen and Clifford B. Schrock “Television Operational Measurements, Video and RF for NTSC Systems” Tektronix, 1980.
3. “Electrical Performance Standards for Television Relay Facilities” Electronic Industries Association Standard RS-250-B, 1976.
4. L. E. Weaver, Television Video Transmission Measurements, (London, Marconi Instruments, 1971).
5. F. F. Mazda, ed., Electronic Engineers Reference Book, 5th ed. (London Butterworth, 1982).

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