

LF351 Wide Bandwidth JFET Input Operational Amplifier

General Description

The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

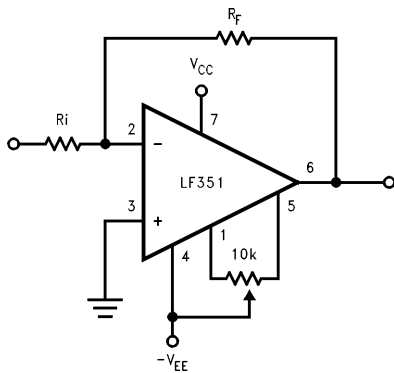
The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply

current is important, however, the LF351 is the better choice.

Features

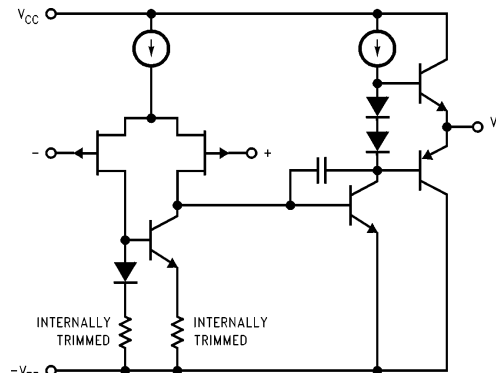
- Internally trimmed offset voltage 10 mV
- Low input bias current 50 pA
- Low input noise voltage 25 nV/ $\sqrt{\text{Hz}}$
- Low input noise current 0.01 pA/ $\sqrt{\text{Hz}}$
- Wide gain bandwidth 4 MHz
- High slew rate 13 V/ μs
- Low supply current 1.8 mA
- High input impedance $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $< 0.02\%$
- $R_L = 10\text{k}$, $V_O = 20\text{ Vp-p}$, $\text{BW} = 20\text{ Hz} - 20\text{ kHz}$
- Low 1/f noise corner 50 Hz
- Fast settling time to 0.01% 2 μs

Typical Connection



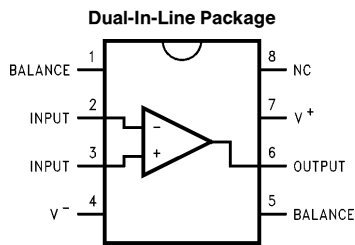
TL/H/5648-11

Simplified Schematic



TL/H/5648-12

Connection Diagrams



TL/H/5648-13

Order Number LF351M or LF351N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	± 18V
Power Dissipation (Notes 1 and 6)	670 mW
Operating Temperature Range	0°C to +70°C
T _J (MAX)	115°C
Differential Input Voltage	± 30V
Input Voltage Range (Note 2)	± 15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	-65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	
Metal Can	300°C
DIP	260°C

θ_{JA}	N Package	120°C/W
	M Package	TBD
Soldering Information		
	Dual-In-Line Package	
	Soldering (10 sec.)	260°C
	Small Outline Package	
	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD rating to be determined.		

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
V _{OS}	Input Offset Voltage	R _S = 10 k Ω , T _A = 25°C Over Temperature		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R _S = 10 k Ω		10		$\mu V/^{\circ}C$
I _{OS}	Input Offset Current	T _J = 25°C, (Notes 3, 4) T _J ≤ 70°C		25	100 4	pA nA
I _B	Input Bias Current	T _J = 25°C, (Notes 3, 4) T _J ≤ ±70°C		50	200 8	pA nA
R _{IN}	Input Resistance	T _J = 25°C		10 ¹²		Ω
A _{VOL}	Large Signal Voltage Gain	V _S = ±15V, T _A = 25°C V _O = ±10V, R _L = 2 k Ω Over Temperature	25	100		V/mV V/mV
V _O	Output Voltage Swing	V _S = ±15V, R _L = 10 k Ω	±12	±13.5		V
V _{CM}	Input Common-Mode Voltage Range	V _S = ±15V	±11	+15 -12		V V
CMRR	Common-Mode Rejection Ratio	R _S ≤ 10 k Ω	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I _S	Supply Current			1.8	3.4	mA

AC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V, T_A = 25^\circ C$		13		V/ μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V, T_A = 25^\circ C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25^\circ C, R_S = 100\Omega, f = 1000 \text{ Hz}$		25		nV/ \sqrt{Hz}
i_n	Equivalent Input Noise Current	$T_j = 25^\circ C, f = 1000 \text{ Hz}$		0.01		pA/ \sqrt{Hz}

Note 1: For operating at elevated temperature, the device must be derated based on the thermal resistance, θ_{JA} .

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

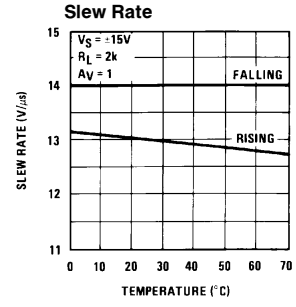
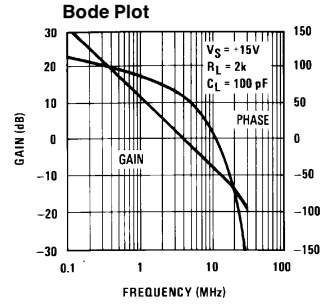
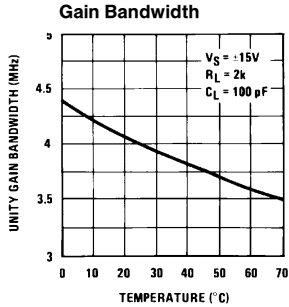
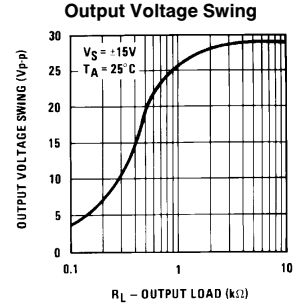
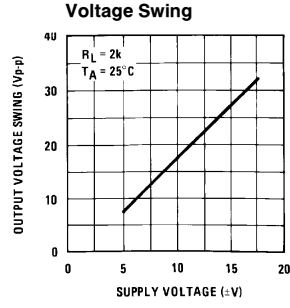
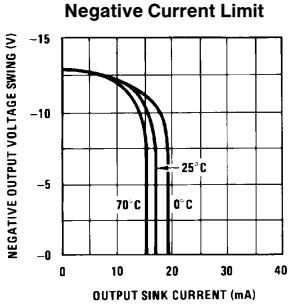
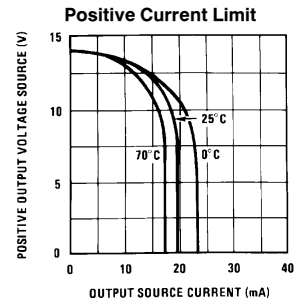
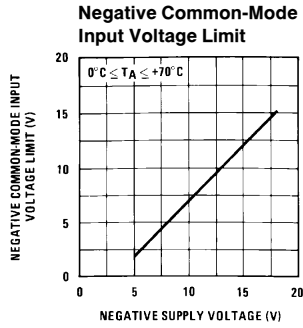
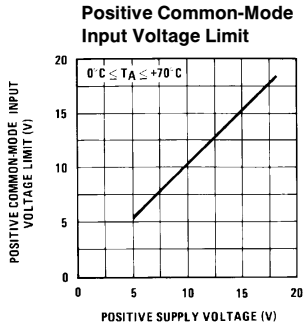
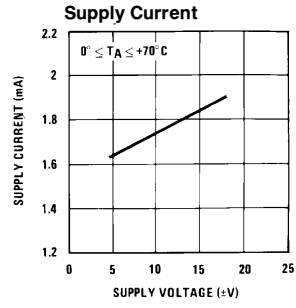
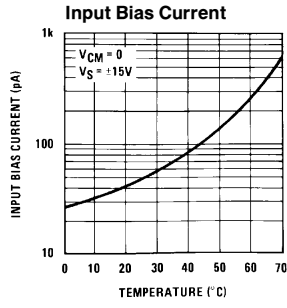
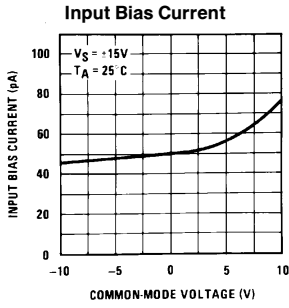
Note 3: These specifications apply for $V_S = \pm 15V$ and $0^\circ C \leq T_A \leq +70^\circ C$. V_{OS} , I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The input bias currents are junction leakage currents which approximately double for every $10^\circ C$ increase in the junction temperature, T_j . Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_j = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From $\pm 15V$ to $\pm 5V$.

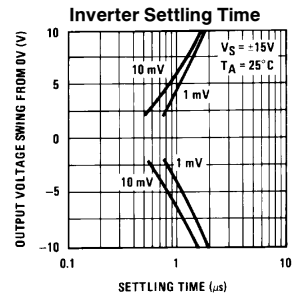
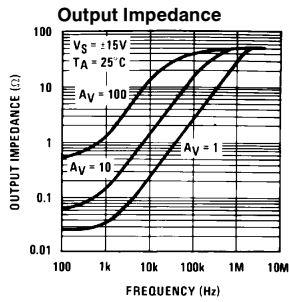
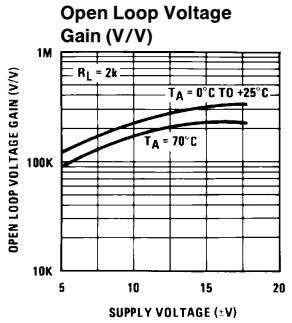
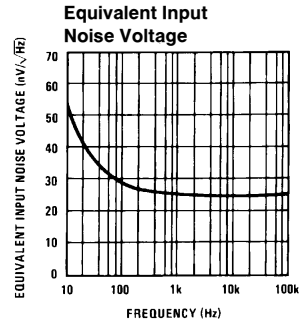
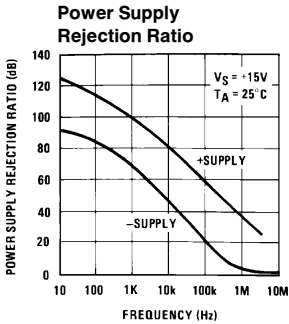
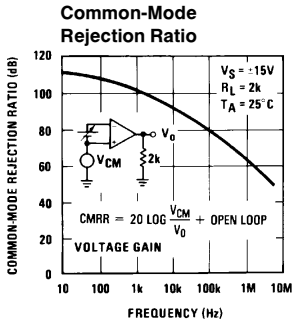
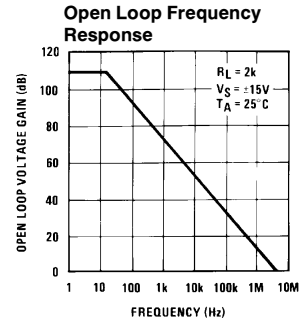
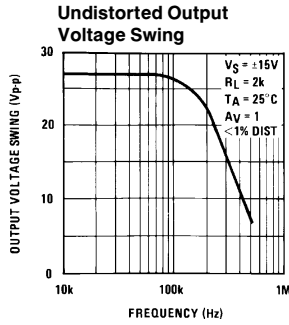
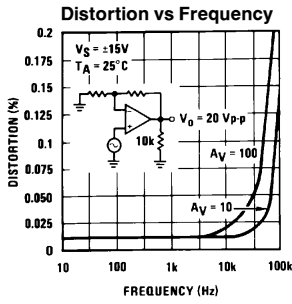
Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics



TL/H/5648-2

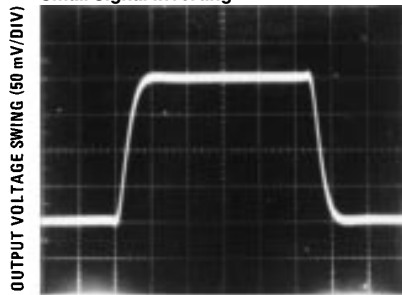
Typical Performance Characteristics (Continued)



TL/H/5648-3

Pulse Response

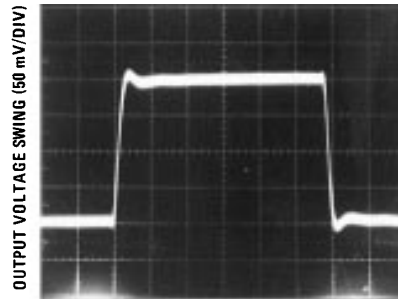
Small Signal Inverting



TIME (0.2 μs/DIV)

TL/H/5648-4

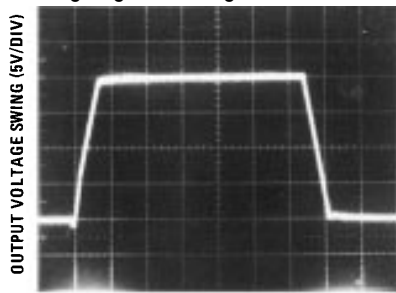
Small Signal Non-Inverting



TIME (0.2 μs/DIV)

TL/H/5648-5

Large Signal Inverting



TIME (0.2 μs/DIV)

TL/H/5648-6

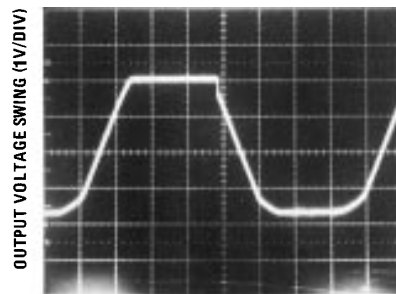
Large Signal Non-Inverting



TIME (0.2 μs/DIV)

TL/H/5648-7

Current Limit ($R_L = 100\Omega$)



TIME (5 μs/DIV)

TL/H/5648-8

Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will

cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

Application Hints (Continued)

common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on $\pm 4V$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF351 will drive a $2\text{ k}\Omega$ load resistance to $\pm 10V$ over the full temperature range of 0°C to $+70^\circ\text{C}$. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

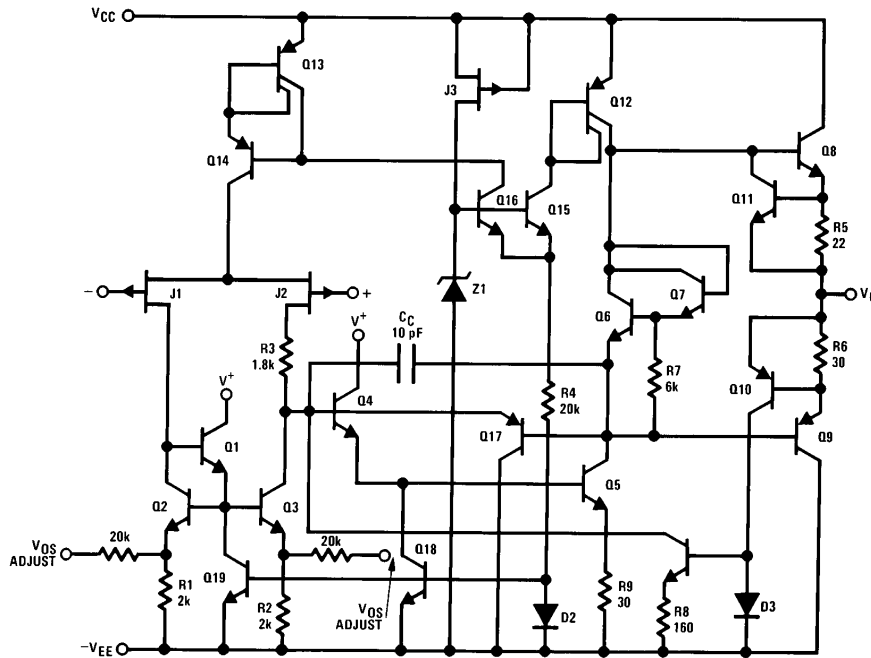
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed back-

wards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

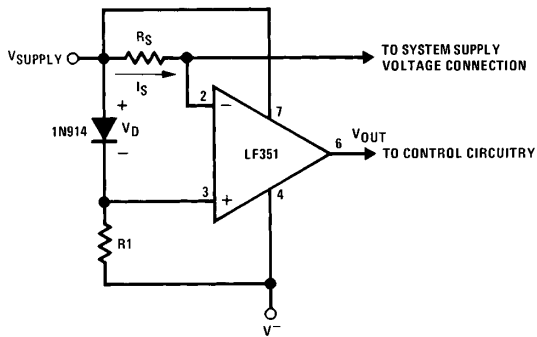
Detailed Schematic



TL/H/5648-9

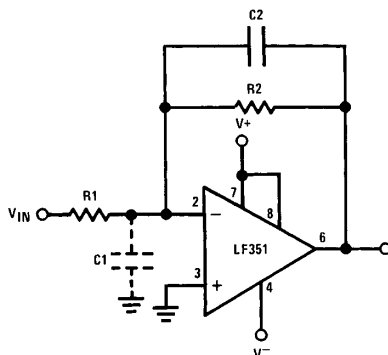
Typical Applications

Supply Current Indicator/Limiter



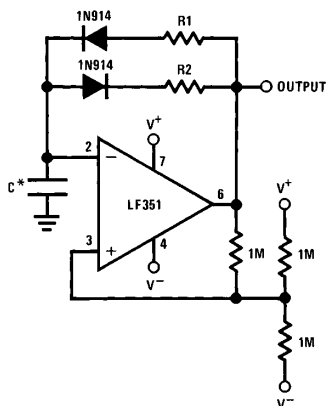
• V_{OUT} switches high when $R_S I_S > V_D$

Hi-Z_{IN} Inverting Amplifier



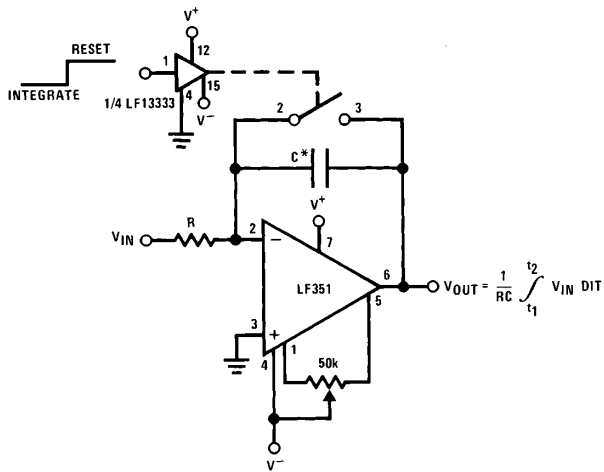
Parasitic input capacitance $C_1 \approx (3 \text{ pF for LF351 plus any additional layout capacitance})$ interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C_2 such that: $R_2 C_2 \approx R_1 C_1$.

Ultra-Low (or High) Duty Cycle Pulse Generator



• $t_{OUTPUT \text{ HIGH}} \approx R_1 C \ln \frac{4.8 - 2V_S}{4.8 - V_S}$
 • $t_{OUTPUT \text{ LOW}} \approx R_2 C \ln \frac{2V_S - 7.8}{V_S - 7.8}$
 where $V_S = V^+ + |V^-|$
 *low leakage capacitor

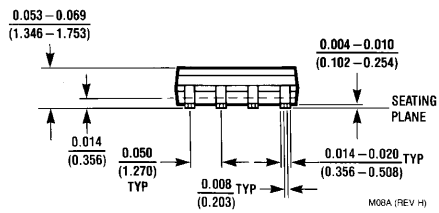
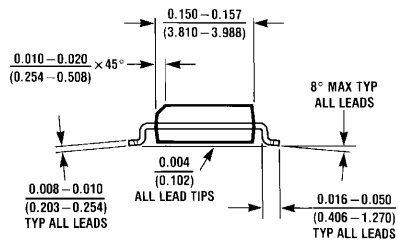
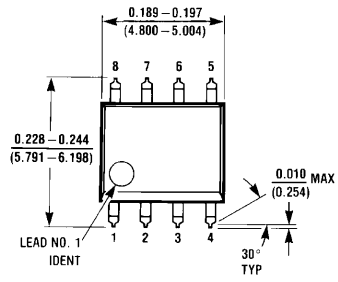
Long Time Integrator



*Low leakage capacitor
 • 50k pot used for less sensitive V_{OS} adjust

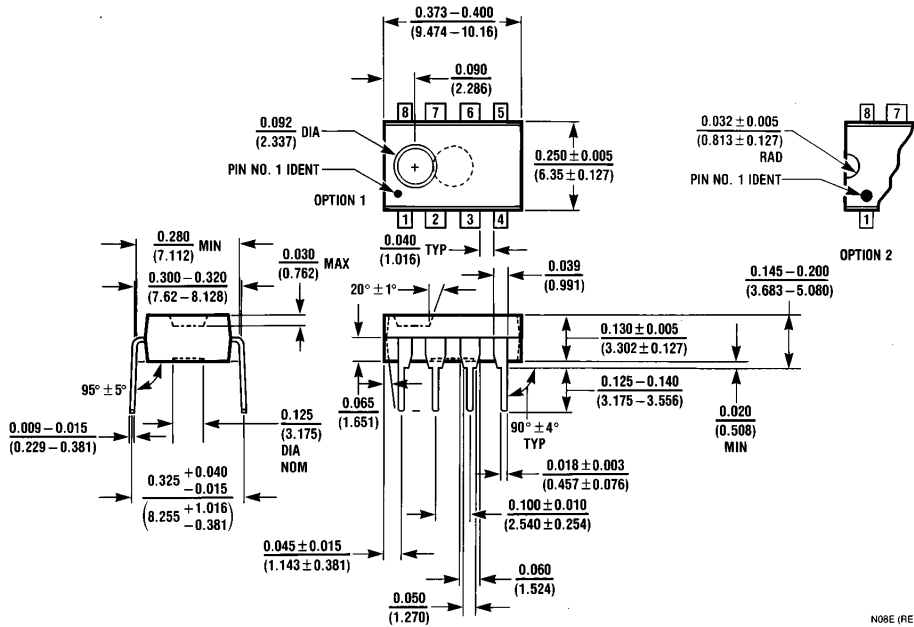
TL/H/5648-10

Physical Dimensions inches (millimeters)



SO Package (M)
Order Number LF351M
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LF351N
NS Package Number N08E

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