The self-aligned gate of LinCMOS transistors results in a gate-drain capacitance that is approximately one-seventh that of typical metal-gate CMOS integrated circuits. This enhances the bandwidth and speed of LinCMOS devices.

The TLC251 and TLC271 operational amplifiers offer a 2.3 MHz bandwidth, 60-ns rise-time with 25% overshoot, and a slew rate of 4.5 V/μs. These speeds are better than most bipolar operational amplifiers, approach those of BIFET operational amplifiers, and are several times faster than their metal-gate CMOS counterparts.

ADVANTAGES OF LinCMOS OPERATIONAL AMPLIFIERS

The TLC251 and TLC271 series operational amplifiers provide a low input offset voltage (10 mV maximum) that remains highly stable over time and temperature and is not sensitive to input-overdrive voltages. They are also available with tightened, guaranteed input offset voltages.

The TLC251 and TLC271 series operational amplifiers can be adjusted for low-, medium- or high-bias operation. This is accomplished by connecting the bias-select pin to V_{DD} for low bias, to ground for high bias, or to 1/2 V_{DD} for medium bias. By providing a choice of bias conditions, the TLC251 and TLC271 allow users to select between ac performance and power consumption to meet a wide range of circuit requirements. When operated in high-bias with V_{DD} equal to 10 V, these devices draw 100 μA of I_{DD} for 10-mW power dissipation and feature 4.5-V/μs slew rate and 2.3-MHz bandwidth. In the low bias mode with V_{DD} equal to 10 V and I_{DD} equal to 10 μA (100 μW power dissipation), the devices have a slew rate of 0.04 V/μs and a bandwidth of 100 kHz. In low-bias, and at 1 V, the TLC251 consumes just 10 μW making it the ideal choice for battery-operated applications. The bias-select pin can be driven with a logic signal from a microprocessor, allowing the operational amplifier performance to be software-controlled.

Additional features of the TLC251 and TLC271 include a common-mode rejection ratio of 88 dB and a low input-noise voltage of 30 to 70 nV/$\sqrt{\text{Hz}}$ (depending upon whether the device is operating in high, medium, or low bias).

These capabilities make the TLC251 and TLC271 suited for a wide range of applications. These applications include active filters, transducer interfacing, current drivers, voltage-to-current converters, long-interval timers, and many types of amplifiers. The TLC251 and TLC271 series are particularly suited for low-power designs and instrumentation amplifiers that require stable offsets.

When using the TLC251 or TLC271 LinCMOS devices for design, the following characteristics must be considered:

- Supply Voltage, V_{DD}
  - TLC251 ..... 1 V to 16 V
  - TLC271 ..... 4 V to 16 V
- True Single Supply or a Maximum of ±8 V
- Adjustable Supply Current, I_{DD}
  - Low Bias = 10 μA typical
  - Medium Bias = 150 μA typical
  - High Bias = 1000 μA typical
- Extremely Low Input Bias and Offset Currents: 1 pA Typical
- Low Input Offset Voltage: 3 mV typical
- Ultra Stable Input-Offset Voltage: 0.1 μV/Month Typical
- Noise: 30 nV/Hz Typical
- Slew Rate, SR
  - High Bias ..... 4.5 V/μs typical
  - Medium Bias..... 0.6 V/μs typical
  - Low Bias..... 0.04 V/μs typical
- Bandwidth, BW
  - High Bias ..... 2.3 MHz
  - Medium Bias..... 0.7 MHz
  - Low Bias..... 0.1 MHz

COMPARATORS

A basic comparator is similar to a differential amplifier operating in the open-loop mode. Because of high gain, the output is normally saturated in either the high state or the low state depending upon the relative amplitudes of the two input voltages. With these conditions, the comparator provides a logic-state output which is indicative of the amplitude relationship between two analog input signals.

In typical applications, a comparator provides an indication of the relative state of the two input signals. Figure 2 -34 illustrates a basic comparator and its transfer function.

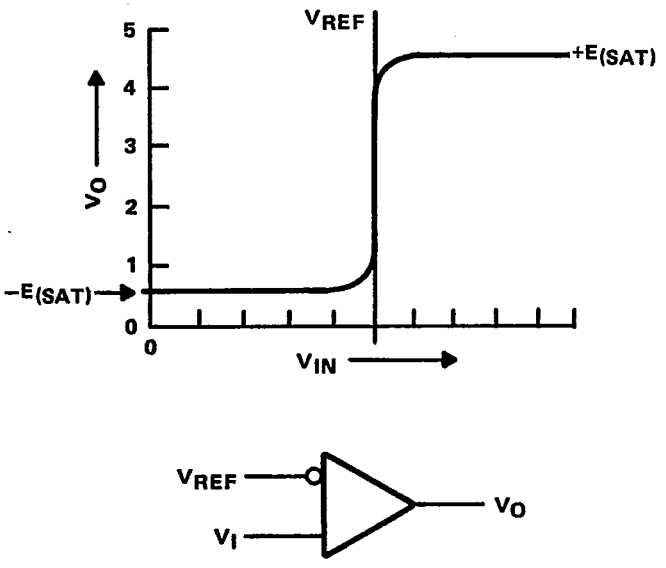


Figure 2-34. Basic Comparator and Transfer Function

In the circuit in Figure 2-34, if a reference voltage is applied to the inverting input and an unknown potential to the noninverting input, the output will reflect the relationship between the two inputs. When V_I is more negative that V_{REF}, the device output will be in saturation at a logic low level. When V_I becomes more positive than V_{REF}, the output will change states and become saturated at a logic high level.

Because comparators are normally used to drive logic circuits, the output must change states as rapidly as possible. High open-loop gain, wide bandwidth and slew rate are key factors in comparator speed. Operation in the open-loop mode (no feedback), with minimum or no frequency compensation, results in maximum gain-bandwidth product for best performance. Most comparators operate in this manner.

The ideal comparator has the same characteristics as the ideal operational amplifier. Those characteristics are as follows:

- Differential Gain = → ∞
- Common-Mode Gain = 0
- Input Impedance = → ∞
- Output Impedance = 0
- Bandwidth = → ∞
- Offset Voltage and Current = 0

Initially operational amplifiers were used in the open-loop mode to perform comparator functions. However, devices designed specifically for this operation resulted in improvements in recovery time, switching speed, and output levels. Since the comparator amplifier stage is usually followed by a TTL logic stage, output logic-state levels normally match those required by TTL loads.

Circuits designed as a comparator use none of the phase/frequency compensation usually required for operational amplifier stabilization with feedback. In fact, these compensation components are detrimental because they slow the response time of the comparator. Although any operational amplifier may be used as a comparator, a compensated device (such as the TL071) will result in longer response times and an output that is not directly TTL compatible.

COMPARATOR PARAMETERS

Some of the common comparator parameters are discussed in the following paragraphs.

Source Impedance

The input bias current of a bipolar comparator is approximatley 10 μA. When the differential input voltage makes the comparator switch, the input bias current is present at one of the inputs and is almost zero at the other. If the source impedances are not negligible, feedback will lower the gain of the comparator and create parasitic oscillations. Figure 2-35 shows this phenomenon occuring with a TL810. The comparator is driven by a ramp voltage at a rate of 1 mV/μs as represented by the center waveform. The upper output waveform shows the response of the comparator with a source impedance of 50 Ω. The lower output waveform represents the response of the same comparator with a source impedance of 10 kΩ. The initial switching occurs sooner with a high source impedance because the bias current characteristics produce an additional offset voltage. However, the subsequent oscillations make this circuit configuration unusable with low-slew-rate input signals.

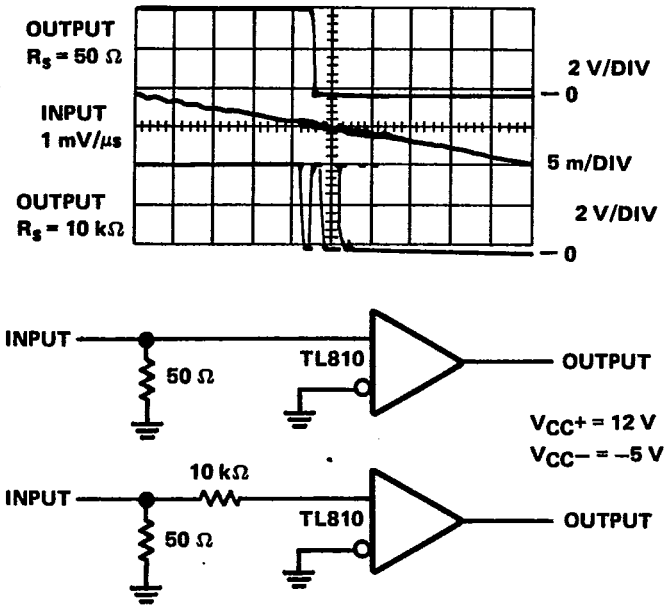


Figure 2-35. Influence of Source Impedance

Differential Voltage Gain

Differential voltage gain (A_{VD}) determines the sensitivity and threshold accuracy of a comparator. In the ideal comparator, the gain would be infinite and an extremely small voltage applied between the two inputs would cause a change in the output. In actual practice, the gain is not infinite and some minimum voltage variation at the input is required to obtain a change in the output. The ratio of the variation of output voltage to that of input voltage is the voltage gain of the comparator. The voltage gain of the comparator may be expressed by the following equation:

$$A_{VD} = \frac{\Delta V_O}{\Delta V_I}$$

The quantity ΔV_O (the difference between the high and low states of the output) is normally set at 2.5 V to ensure matching between the comparator and a TTL load. For example, if the TL810 has a minimum A_{VD} of 12,500, then (for an output swing of 2.5 V) $\Delta V_{I(min)}$ = 2.5 V/12,500, or 0.2 mV.

Output Characteristics

Although some comparators have a full TTL fanout capability of 10 or greater, others have a fanout that is limited to one TTL load. An evaluation of the output circuits should indicate the basic limiting factors and how maximum performance can be obtained.

In the active pull-down mode [see Figure 2-36(a)], the output low-level sink current (I_{OL}) is limited. The emitter of Q2 is clamped at one base-emitter voltage drop or −0.7 V with Q3 providing another base-emitter voltage drop. The

resulting low-level output current (I_{OL}) may be calculated from the following equation:

$$I_{OL} = \frac{V_{CC} - 2\,V_{BE}}{1.77\ k\Omega}$$

$$= \frac{-6\ V + 1.4\ V}{1.77\ k\Omega} = -2.6\ mA$$

The resulting value is near the typical value for this device. The minus sign indicates a sink current. The corresponding $V_{OL} = V_E\ (Q2) + V_{CE(SAT)(Q2)}$ or $(-0.7\ V + 0.2\ V) = -0.5\ V$, which is the typical data sheet value.

In a logic low-level ouput state, the TL810 can handle one standard TTL gate with its maximum requirement of -1.6 mA. Increased fanout capability can be obtained by connecting an external resistor between the comparator output and the negative supply.

In the active pull-up mode, the typical high-level output voltage (V_{OH}) is 3.2 V for the TL810. The voltage at the base of the pull-up transistor [Q1, Figure 2-36(b)] is defined by the following equation:

$$V_{OH} + V_Z + V_{BE(Q1)}$$

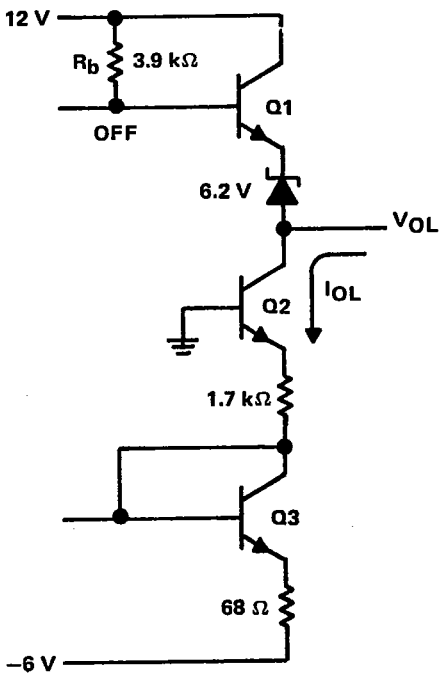
Where:

$V_Z = 6.2\ V$
$V_{BE(Q1)} = 0.7\ V$

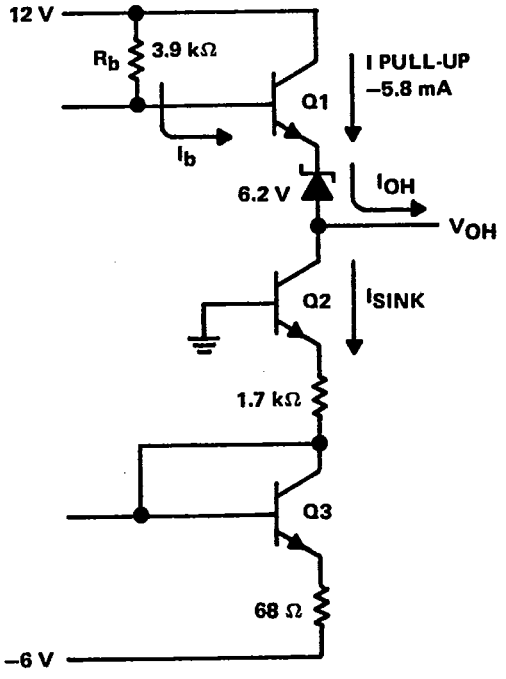
The base vaoltage is (3.2 + 6.2 + 0.7), 10.1 V. The resulting base drive is determined by the following equation:

$$I_b = \frac{V_{CC+} - V_B}{R_b}$$

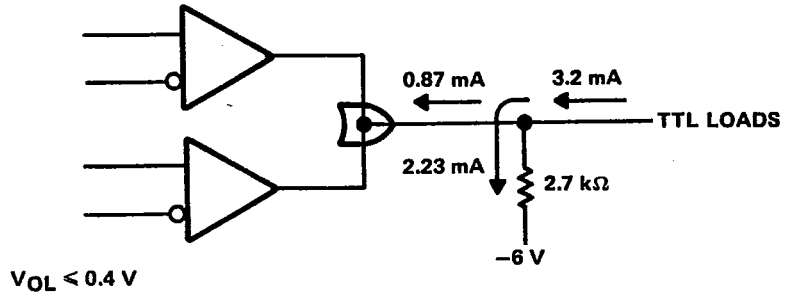
$$= \frac{12\ V - 10.1\ V}{3.9\ k\Omega}\ 0.488\ mA$$



(a) TL810 LOW STATE



(b) TL810 HIGH STATE



(c) TL811 FANOUT OF 2

Figure 2-36. Comparator Output Configurations

Assuming a typical saturated h_{FE} of 12, the resulting pull-up drive capability is (0.488 mA) (12) or 5.8 mA. Only part of the 5.8-mA drive is available to the external circuit. Since the current sink is not turned off during the logic-high output condition, the remainder of the current will be shunted through the pull-down circuit. For TL810, the resulting I_{OH} level available for external drive will be the difference between the pull-up drive of 5.8 mA and the pull-down sink of 2.6 and is 3.2 mA [Figure 2-36(c)]. The 3.2 mA is adequate because the logic high level (I_{OH}) required is only 40 μA per TTL load. Similar calculations for the TL811 comparator yield an I_{OL} level of 0.87 mA and an I_{OH} of 4.3 mA. For example, a fanout capability of 2 requires an I_{OL} level of 3.2 mA. With the TL811 [see Figure 2-36(c)], a 2.7-kΩ resistor is connected between the output and the negative supply. The resulting I_{OL} is 3.2 mA at a 0.4-V maximum V_{OL}. The effective I_{OH} capability, therefore, is reduced to 1.19 mA at a minimum V_{OH} of 2.4 V.

STANDARD COMPARATORS

The typical comparator consists of a high-gain stage followed by a logic-state output. Standard comparators with many performance features, including strobes and high-output current capabilities, are available today.

The LM311 is a popular bipolar device that will operate from single or dual supplies from 5 V to 30 V (or $\pm$ 15 V). The LM311 has an uncommitted output transistor with an available emitter and collector. This allows source or sink output drive. The output is compatible with most standard logic levels. The TLC311, built with LinCMOS technology, is an improved version of the LM311. The LinCMOS process allows common-mode input levels down to and including the negative V_{CC} rail or ground and the input impedance is increased from 10^6 Ω to greater than 10^{12} Ω. Figure 2-37 is a basic diagram of the TLC311 and LM311 comparators.

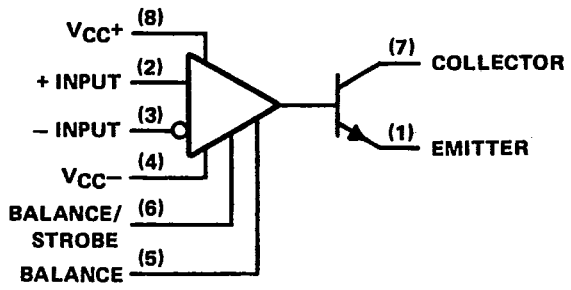


Figure 2-37. TLC311 or LM311 Comparator

USE OF HYSTERESIS

Applications in which the input signal slowly varies can cause the ouput to change proportionally. This becomes a problem when the comparator is used to trigger a logic stage requiring fast rise and fall inputs. One solution to the problem is the introduction of positive feedback. This causes a fast or Schmitt trigger action. This action is accomplished by feeding a portion of the output signal back to the noninverting input. Depending upon the amount of positive feedback, a new trip-level will be introduced after each transition. The result is two (rather than one) threshold points. These are called the upper threshold point (UTP) and lower threshold point (LTP). the difference between these two points is the hysteresis. A comparator with hysteresis is shown in Figure 2-38.

A typical hysteresis loop diagram for this type of circuit is shown in Figure 2-39.

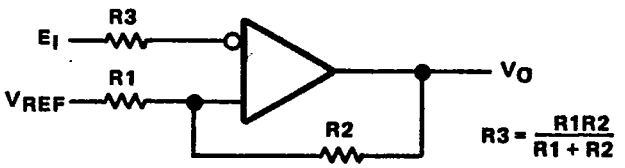


Figure 2-38. Comparator with Hysteresis

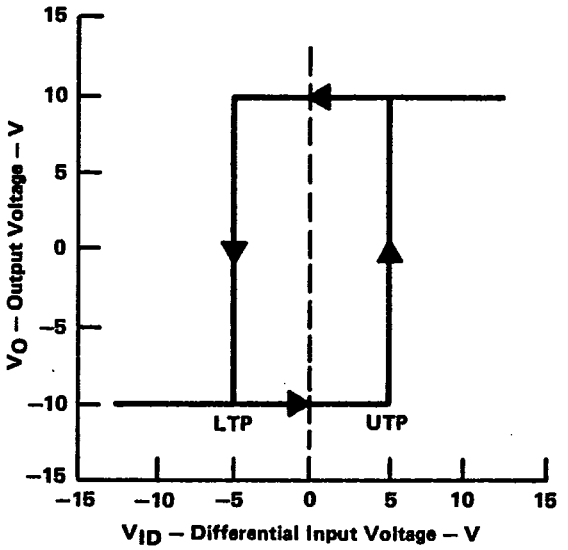


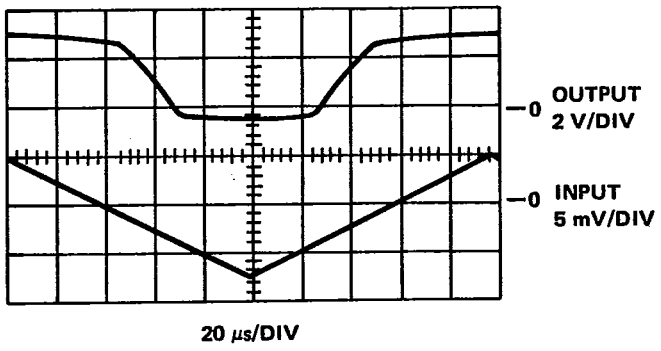
Figure 2-39. Typical Comparator Hysteresis Loop

APPLICATION PRECAUTION

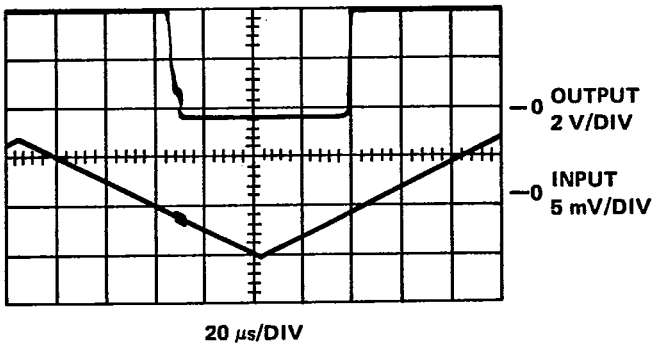
The rise time of the input signal is a critical parameter in comparator applications. The comparator is basically a differential amplifier with very high open-loop gain. The output is compatible in voltage and current with the inputs of TTL circuits. However, this type of logic requires switching times of less than 150 ns to function correctly without going into oscillation. The comparator input signal must vary rapidly enough to avoid this problem.

Figure 2-40(a) shows the output of a TL710 being driven by a ramp voltage which varies at approximately 0.1 mV/μs. The switching times of the output, taken between 0.8 V and 2 V, are approximately 10 μs for the fall and rise times. In this mode, the output of the comparator is not compatible with TTL circuits.

Figure 2-40(b) shows a TL810 under the same conditions as described for the TL710. With a higher gain than the TL710, the switching speed for the TL810 is also higher,



(a) TL710



(b) TL810

Figure 2-40. Response of a TL710 and a TL810 to a Ramp Input

and the rise time is compatible with TTL circuits. However, some oscillation is present during the periods of switching. This occurs because the input signal remains in the high-gain linear range of the comparator for an excessive period of time. For the output of a comparator to be good, the input must force the output to vary between 0.8 V and 2 V in 150 ns or less.

When the minimum gain (A_{VD}) of the comparator is known, the input signal must vary at a minimum rate determined by the following equation:

$$\frac{2\text{ V} - 0.8\text{ V}}{150\text{ ns} \times A_{VD}}$$

For the TL710, the minimum rate is determined as follows:

$$\frac{2\text{ V} - 0.8\text{ V}}{150\text{ ns} \times 500} = 16\text{ mV}/\mu\text{s}$$

For the TL810, the minimum rate is determined as follows:

$$\frac{2\text{ V} - 0.8\text{ V}}{150\text{ ns} \times 8000} = 1.0\text{ mV}/\mu\text{s}$$

When these input conditions are not being met, some positive feedback must be added or a Schmitt trigger configuration must be designed (see Figure 2-41) to accelerate the switching speed. However, the resulting hysteresis makes the comparator less voltage sensitive.

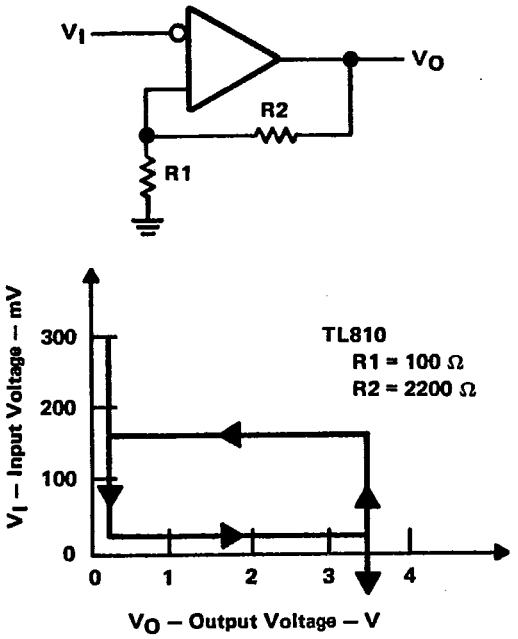


Figure 2-41. Use of Hysteresis to Prevent Oscillations