National Semiconductor™

LMX2322 PLLatinum™ 2.0 GHz Frequency Synthesizer for RF Personal Communications

General Description

The LMX2322 is a high performance frequency synthesizer with integrated 32/33 dual modulus prescaler designed for RF operation up to 2.0 GHz. Using a proprietary digital phase locked loop technique, the LMX2322's linear phase detector characteristics can generate very stable, low noise control signals for UHF and VHF voltage controlled oscillators.

Serial data is transferred into the LMX2322 via a three-line MICROWIRE™ interface (Data, LE, Clock). Supply voltage range is from 2.7 V to 3.9 V. The LMX2322 features very low current consumption, typically 3.5 mA at 3.75V. The charge pump provides 4mA output current.

The LMX2322 is manufactured using National's ABiC V BiCMOS process and is packaged in a 16 pin TSSOP and a 16 pin Chip Scale Package (CSP).

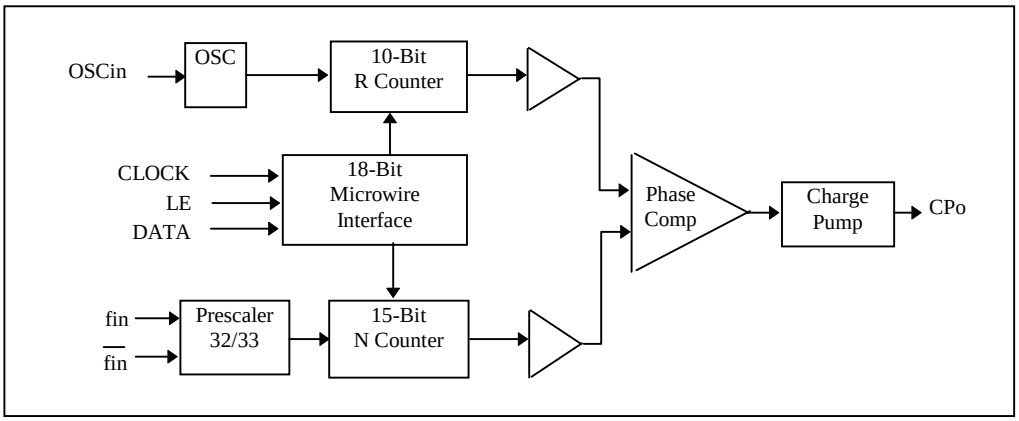
Features

- RF operation up to 2.0 GHz
- 2.7 V to 3.9 V operation
- Low current consumption: I_{CC} = 3.5 mA (typ) at V_{CC} = 3.75 V
- Dual modulus prescaler: 32/33
- Internal balanced, low leakage charge pump

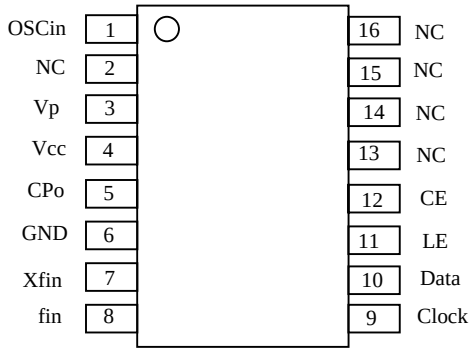
Applications

- Cellular telephone systems (GSM, NADC, CDMA, PDC, PHS)
- Personal wireless communications (DCS-1800, DECT, CT-1+)
- Wireless local area networks (WLANs)
- Other wireless communication systems

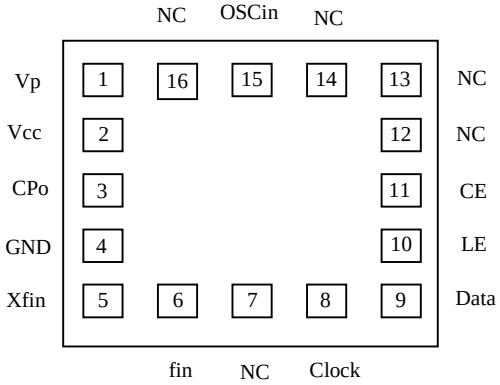
Functional Block Diagram



Connection Diagram



TSSOP 16



CSP 16 (TOP VIEW)

Pin Description

Pin No.		Pin Name	I/O	Description
TSSOP 16	CSP 16			
1	15	OSCin	I	Oscillator input. A CMOS inverting gate input. The input has a Vcc/2 input threshold and can be driven from an external CMOS or TTL logic gate. May also be used as a buffer for an externally provided reference oscillator.
3	1	Vp	-	Power supply for charge pump. Must be ≥ Vcc
4	2	Vcc	-	Power supply voltage input. Input may range from 2.7V to 3.9V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
5	3	CPo	O	Internal charge pump output. For connection to a loop filter for driving the voltage control input of an external oscillator.
6	4	GND	-	Ground.
7	5	Xfin	I	RF prescaler complimentary input. In single-ended mode, a bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. The LMX2322 can be driven differentially when a bypass capacitor is omitted.
8	6	fin	I	RF prescaler input. Small signal input from the voltage controlled oscillator.
9	8	Clock	I	High impedance CMOS Clock input. Data is clocked in on the rising edge, into the various counters and registers.
10	9	Data	I	Binary serial data input. Data entered MSB first. LSB is control bit. High impedance CMOS input.
11	10	LE	I	Load enable input. When Load Enable transitions HIGH, data is loaded into either the N or R register (control bit dependent). See timing diagram.
12	11	CE	I	PLL Enable. A LOW on CE powers down the device asynchronously and TRI-STATEs the charge pump output.
2,13,14, 15, 16	7,12,13 14, 16	NC		No Connect

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	Vcc	-0.3		4.3	V
Power Supply for Charge Pump	Vp	Vcc		4.3	V
Voltage on any pin with GND=0 volts	Vi	-0.3		Vcc+0.5	V
Storage Temperature Range	T_S	- 65		+ 150	^{o} C
Lead Temp. (solder 4 sec)	T_L			+ 260	^{o} C
ESD - whole body model (Note 2)			2		kV

Recommended Operating Conditions (Note 1)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	Vcc	2.7	3.75	3.9	V
Power Supply for Charge Pump	Vp	Vcc		3.9	V
Operating Temperature	T_A	- 40		+ 85	^{o} C

Notes:

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Conditions indicate conditions for which the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

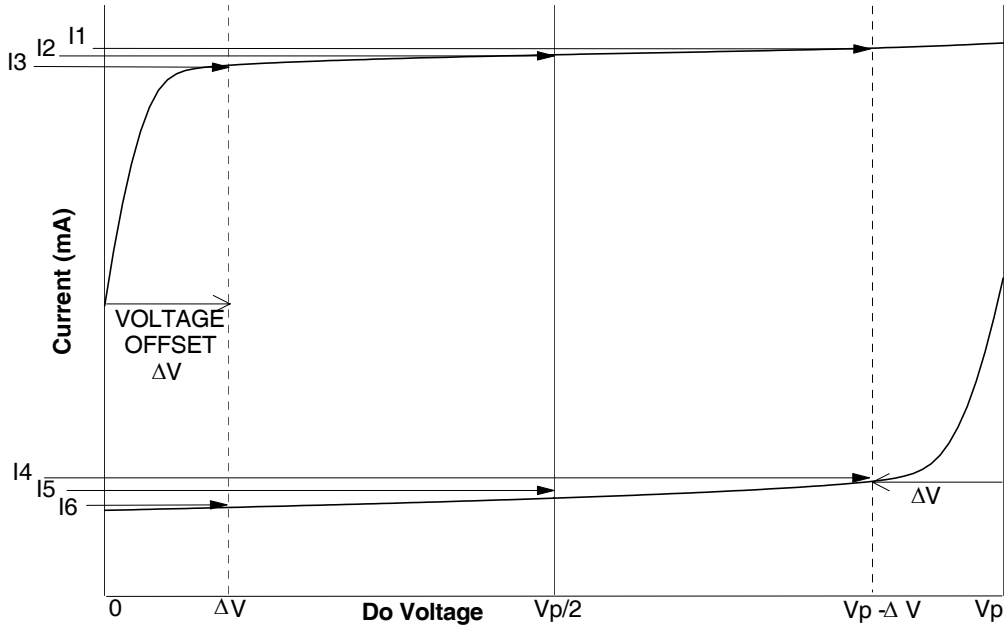
2. This device is a high performance RF integrated circuit and is ESD sensitive. Handling and assembly of this device should on be done on ESD protected workstations.

Electrical Characteristics Vcc = 3.75, Vp = 3.75V ; -40°C <TA< 85°C except as specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Icc	Power Supply Current	Vcc = 3.75 V		3.5		mA
Icc		Vcc=2.7V to 3.9V			7.0	mA
Icc-PWDN		Vcc = 3.9V (Note 1)		10	20	µA
		Vcc = 3.9V (Note 2)			300	µA
fin	RF Operating Frequency		0.7		2.0	GHz
fosc	Oscillator Frequency		5	13	40	MHz
f φ	Phase Detector Frequency			0.2	10	MHz
Vfin	Input Sensitivity	Vcc = 2.7 to 3.9 V Balanced input	45		450	mV_{RMS}
Zin	Input Impedance	f=900MHz (Note 3)	130	360		Ω
		f=1900MHz (Note 3)	100	150		Ω
Vosc	Oscillator Sensitivity	OSCin	0.4	0.8	1.2	Vpp
	Phase Noise (Note 4)	Fin=900MHz, Vosc>=0.8Vpp		-86	Note 6	dBc/Hz
		Fin=900MHz, Vosc>=0.4Vpp		-82	Note 6	
		Fin=1800MHz, Vosc>=0.8Vpp		-82	Note 6	
		Fin=1800MHz, Vosc>=0.4Vpp		-80	Note 6	
VIH	High-level Input Voltage	(Note 5)	2.5			V
VIL	Low-level Input Voltage	(Note 5)			0.4	V
IIH	High-level Input Current (Clock, Data, Load Enable)	VIH = Vcc = 3.9 V	-1.0		1.0	µA
IIL	Low-level Input Current (Clock, Data, Load Enable)	VIL = 0, Vcc = 3.9 V	-1.0		1.0	µA
IIH	Oscillator Input Current	VIH = Vcc = 3.9 V			100	uA
IIL		VIL = 0, Vcc = 3.9 V	-100			uA
ICPo-source	Charge Pump Output Current	VCPo = Vp/2		-4.0		mA
ICPo-sink		VCPo = Vp/2		4.0		mA
ICPo-Tri	Charge Pump Tri-State Current	0.5 ≤ VCPo ≤ Vp - 0.5 T= 25° C	-2.5	0.1	2.5	nA
ICPo vs VCPo	Charge Pump Output Current magnitude variation vs. Voltage	0.5 ≤ VCPo ≤ Vp - 0.5 T = 25° C		10		%
ICPo-sink vs. ICPo-source	Charge Pump Output Current Sink vs. Source Mismatch	VCPo = Vp/2 T = 25° C		5		%
ICPo vs. T	Charge Pump Output Current Magnitude Variation vs. Temperature (Note 4)	VCPo = Vp/2 -40° C ≤ T ≤ +85° C		8		%
tCS	Data to Clock Set Up Time	See Data Input Timing	50			ns
tCH	Data to Clock Hold Time	See Data Input Timing	10			ns
tCWH	Clock Pulse Width High	See Data Input Timing	50			ns
tCWL	Clock Pulse Width Low	See Data Input Timing	50			ns
tES	Clock to Enable Set Up Time	See Data Input Timing	50			ns
tEW	Enable Pulse Width	See Data Input Timing	50			ns

Note 1: This Icc-PWDN represents CLK, DATA, LE and CE being tied to either higher than 0.8Vcc or lower than 0.2Vcc.
Note 2: This Icc-PWDN represents a software power down condition of CE = VIH = 2.5V while LE, CLK and DATA = VIL = 0.4V. Worst case Icc-PWDN of 300µA occurs when CE, LE, CLK and DATA are all held at VIH = 2.5V (4x75µA).
Note 3: Balanced input, | Z | = | R - jXc |
Note 4: Phase noise is measured 1kHz off from the carrier frequency. Comparison frequency is 200kHz. OSCin frequency is 13MHz.
Note 5: except fin and OSCin
Note 6: Typical values are determined from measurements on the reference evaluation boards. A 3dB (3 sigma) degradation is estimated from statistical distribution in manufacturing. Units will NOT be tested in production.

Charge Pump Current Specification Definitions



I1 = CP sink current at VCPo = Vp - ΔV

I2 = CP sink current at VCPo = Vp/2

I3 = CP sink current at VCPo = ΔV

I4 = CP source current at VCPo = Vp-ΔV

I5 = CP source current at VCPo = Vp/2

I6 = CP source current at VCPo = ΔV

ΔV = Voltage offset from positive and negative rails. Dependant on VCO tuning range relative to Vcc and ground. Typical values are between 0.5V and 1.0V

1. I_{CPo} vs V_{CPo} = Charge Pump Output Current magnitude variation vs. Voltage =

$$[\ 1/2 * \{|I1| - |I3|\ \}\ /\ [\ 1/2 * \{\ |I1| + |I3|\}\ ]\ *100\% \quad \text{and} \quad [\ 1/2 * \{|I4| - |I6|\}\ ]\ /\ [\ 1/2 * \{\ |I4| + |I6|\}\ ]\ *100\%$$

2. $I_{CPo\text{-}sink}$ vs. $I_{CPo\text{-}source}$ = Charge Pump Output Current Sink vs. Source Mismatch =

$$[\ |I2| - |I5|\ ]\ /\ [\ 1/2 * \{\ |I2| + |I5|\ \}\ ]\ * 100\%$$

3. I_{CPo} vs T_A = Charge Pump Output Current magnitude variation vs. Temperature =

$$[\ |I2 @ temp| - |I2 @ 25° C|\ ]\ /\ |I2 @ 25° C|\ * 100\% \quad \text{and} \quad [\ |I5 @ temp| - |I5 @ 25° C|\ ]\ /\ |I5 @ 25° C|\ * 100\%$$

1.0 Functional Description

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX2322, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, as well as programmable reference [R] and feedback [N] frequency dividers. The VCO frequency is established by dividing the crystal reference signal down via the R counter to obtain a frequency that sets the comparison frequency. This reference signal, fr, is then presented to the input of a phase/frequency detector and compared with another signal, fp, the feedback signal, which was obtained by dividing the VCO frequency down by way of the N counter. The phase/frequency detector's current source outputs pump charge into the loop filter, which then converts the charge into the VCO's control voltage. The phase/frequency comparator's function is to adjust the voltage presented to the VCO until the feedback signal's frequency (and phase) match that of the reference signal. When this 'phase-locked' condition exists, the RF VCO's frequency will be N times that of the comparison frequency, where N is the divider ratio.

1.1 Oscillator

The reference oscillator frequency for the PLL is provided by an external reference TCXO through the OSCin pin. OSCin block can operate to 40MHz with a minimum input sensitivity of 0.4Vpp. The inputs have a Vcc/2 input threshold and can be driven from an external CMOS or TTL logic gate.

1.2 Reference Divider (R Counter)

The R Counter is clocked through the oscillator block. The maximum input frequency is 40MHz and the maximum output frequency is 10MHz. The R Counters is a 10 bit CMOS binary counters with a divide range from 2 to 1,023. See programming description 2.2.1.

1.3 Programmable Divider (N Counter)

The N counter is clocked by the small signal fin input. The LMX2322 RF N counter is a 15 bit integer divider. The N counter is configured as a 5 bit A Counter and a 10 bit B Counter, offering a continuous integer divide range from 992 to 32,767. The LMX2322 is capable of operating from 700MHz to 2.0GHz with a 32/33 precaler.

1.3.1 Prescaler

The RF inputs to the prescaler consist of the fin and $\overline{\text{fin}}$ pins which are the complimentary inputs of a differential pair amplifier. The differential fin configuration can operate to 2GHz with a minimum input sensitivity of 45mVrms. The input buffer drives A counter's ECL D-type flip-flops in a dual modulus configuration. The LMX2322 has a 32/33 prescaler ratio. The prescaler clocks the subsequent CMOS flip-flop chain comprising the fully programmable A and B counters.

1.4 Phase/Frequency Detector

The phase/frequency detector is driven from the N and R counter outputs. The maximum frequency at the phase detector inputs is 10 MHz. The phase detector outputs control the charge pumps. The polarity of the pump-up or pump-down control is programmed using PD_POL, depending on whether RF VCO characteristics are positive or negative (see programming description 2.2.2). The phase detector also receives a feedback signal from the charge pump, in order to eliminate dead zone.

1.5 Charge Pump

The phase detector's current source output pumps charge into an external loop filter, which then converts the charge into the VCO's control voltage. The charge pumps steer the charge pump output, Cpo, to Vcc (pump-up) or Ground (pump-down). When locked, Cpo is primarily in a Tri-state mode with small corrections. The RF charge pump output current magnitude is set to 4.0mA. The charge pump output can also be used to output divider signals as detailed in section 2.2.3.

1.6 Microwire Serial Interface

The programmable functions are accessed through the Microwire serial interface. The interface is made of three functions: clock, data and latch enable (LE). Serial data for the various counters is clocked in from data on the rising edge of clock, into the 18- bit shift register. Data is entered MSB first. The last bit decodes the internal register address. On the rising edge of LE, data stored in the shift register is loaded into one of the two

appropriate latches (selected by address bits). A complete programming description is included in the following sections.

1.7 Power Control

The PLL can be power controlled in two ways. The first method is by setting the CE pin LOW. This asynchronously powers down the PLL and TRI-STATEs the charge pump output, regardless of the PWDN bit status. The second method is by programming through MICROWIRE, while keeping the CE HIGH. Programming the PWDN bit in the N register HIGH (CE=HIGH) will disable the N counter and de-bias the fin input (to a high impedance state). The R counter functionality also becomes disabled. The reference oscillator block powers down when the power down bit is asserted. The OSCin pin reverts to a high impedance state when this condition exists. Power down forces the charge pump and phase comparator logic to a TRI-STATE condition. A power down counter reset function resets both N and R counters. Upon powering up the N counter resumes counting in "close" alignment with the R counter (The maximum error is one prescaler cycle). The MICROWIRE control register remains active and capable of loading and latching in data during all of the power down modes.

2.0 Programming Description

2.1 MICROWIRE™ Interface

The MICROWIRE™ interface is comprised of an 18 bit shift register, a R register and a N register. The shift register consists of a 17 bit DATA field and a 1 bit address (ADDR) field as shown below. When Latch Enable transitions HIGH, data stored in the shift register is loaded into either the R or N register depending on the ADDR bit as described in Table 2.1.1. The data is loaded MSB first. The DATA field assignment for the R and N registers are shown in Table 2.1.2 below.

MSB **LSB**

DATA [16:0]	ADDR
17 **1**	**0**

2.1.1 Address bit Truth Table

When LE is transitioned high, data is transferred from the 18-bit shift register into either the 14-bit R register, or the 17 bit N register depending upon the state of the ADDR bit.

ADDR	DATA Location
0	N register
1	R register

2.1.2 Register Content Truth Table

	First Bit					SHIFT REGISTER BIT LOCATION											Last Bit
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N register	NB_CNTR										NA_CNTR					CTL_WORD		0
R register	X	X	X	TEST	RS	PD_POL	CP_TRI	R_CNTR										1

2.2 R REGISTER

If the Address Bit (ADDR) is 1, when LE is transitioned high data is transferred from the 18-bit shift register into the 14-bit R register. The R register contains a latch which sets the PLL 10-bit R counter divide ratio. The divide ratio is programmed using the bits R_CNTR as shown in Table 2.2.1. The ratio must be ≥ 2. The PD_POL, CP_TRI and TEST bits control the phase detector polarity, charge pump tri-state, and test mode respectively, as shown in Table 2.2.2 . The RS bit is reserved and should always be set to zero. X denotes a don't care condition.

First Bit					SHIFT REGISTER BIT LOCATION												Last Bit
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	TEST	RS	PD_POL	CP_TRI	R_CNTR[9:0]										1

2.2.1 10-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER)

R_CNTR										
Divide Ratio	9	8	7	6	5	4	3	2	1	0
2	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•
1,023	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio: 2 to 1,023 (Divide ratios less than 2 are prohibited)
R_CNTR - These bits select the divide ratio of the programmable reference dividers

2.2.2 R Register Truth Table

BIT	LOCATION	FUNCTION	0	1
CP_TRI	R[11]	Charge Pump TRISTATE	Normal operation	TRISTATE
PD_POL	R[12]	Phase Detector Polarity	Negative	Positive
TEST	R[14]	Test mode bit	Normal operation	Test mode

If the test mode is NOT activated (R[14]=0), the charge pump is active when CP_TRI is set LOW. When CP_TRI is set HIGH, the charge pump output and phase comparator are forced to a TRI-STATE condition. This bit must be set HIGH if the test mode is ACTIVATED (R[14]=1).
If the test mode is NOT activated (R[14]=0), PD_POL sets the VCO characteristics to positive when set HIGH. When PD_POL is set LOW, the VCO exhibits a negative characteristic where the VCO frequency decreases with increasing control voltage.
If the test mode is ACTIVATED (R[14]=1), the outputs of the N and R counters are directed to the CPo output to allow for testing. The PD_POL bit selects which counter output according to Table 2.2.3.

2.2.3 Test mode truth table (R[14] = 1)

CPo Output	CP_TRI R[11]	PD_POL R[12]
R divider output	1	0
N divider output	1	1

2.3 N REGISTER

If the address bit is LOW (ADDR=0), when LE is transitioned high, data is transferred from the 18-bit shift register into the 17-bit N register. The N register consists of the 5-bit swallow counter (A counter), the 10 bit programmable counter (B counter) and the control word. Serial data format is shown below in tables 2.3.1 and 2.3.2. The pulse swallow function which determines the divide ratio is described in section 2.3.3.

First Bit	SHIFT REGISTER BIT LOCATION																Last Bit
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NB_CNTR [9:0]										NA_CNTR[4:0]					CTL_WORD[1:0]		0

2.3.1 5-BIT SWALLOW COUNTER DIVIDE RATIO (A COUNTER)

Swallow Count	NA_CNTR				
(A)	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0
1	0	0	0	0	1
•	•	•	•	•	•
31	1	1	1	1	1

Notes: Swallow Counter Value: 0 to 31

NB_CNTR $\geq$ NA_CNTR

2.3.2 10-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (B COUNTER)

	NB_CNTR									
Divide Ratio	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
3	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•
1023	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio: 3 to 1,023(Divide ratios less than 3 are prohibited)

NB_CNTR $\geq$ NA_CNTR

2.3.3 PULSE SWALLOW FUNCTION

The N divider counts such that it divides the VCO RF frequency by (P+1) A times, and then divides by P(B-A) times. The B value (NB_CNTR) must be $\geq$ 3. The continuous divider ratio is from 992 to 32,767. Divider ratios less than 992 are achievable as long as the binary counter value is greater than the swallow counter value (NB_CNTR $\geq$ NA_CNTR).

$fvco = N \times (fosc / R)$

$N = (P \times B) + A$

fvco: Output frequency of external voltage controlled oscillator (VCO)

fosc: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 10-bit programmable reference counter (3 to 1023)

N: Preset divide ratio of main 15-bit programmable integer N counter (992 to 32,767)

B: Preset divide ratio of binary 10-bit programmable B counter (3 to 1023)

A: Preset value of binary 5-bit swallow A counter ($0 \leq A \leq 31$, $A \leq B$)

P: Preset modulus of dual modulus prescaler (P=32)

2.3.4 CTL_WORD

MSB **LSB**

CNT_RST	**PWDN**

2.3.4.1 Reserve Word Truth Table

CE	CNT_RST	PWDN	FUNCTION
1	0	0	Normal Operation
1	0	1	Synchronous Powerdown
1	1	0	counter reset
1	1	1	Asynchronous Powerdown
0	X	X	Asynchronous Powerdown

Notes:

X denotes don't care.

1. The **Counter Reset** bit when activated allows the reset of both N and R counters. Upon powering up the N counter resumes counting in "close" alignment with the R counter. (The maximum error is one prescalar cycle).

2**.** Both synchronous and asynchronous **power down** modes are available with the LMX2322 to be able to adapt to different types of applications. The MICROWIRE control register remains active and capable of loading and latching in data during all of the powerdown modes

Synchronous Power down Mode

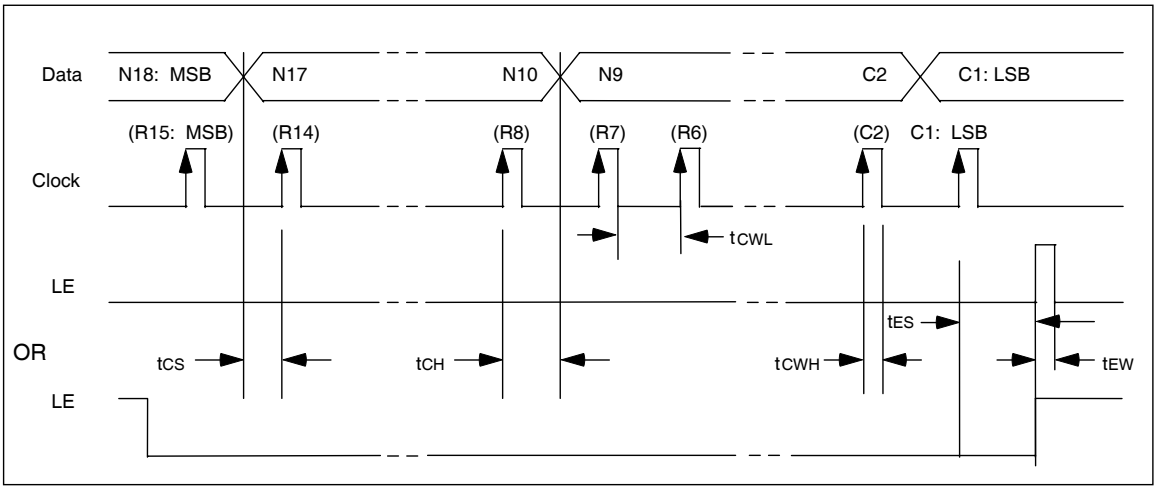
The PLL loops can be synchronously powered down by setting the counter reset mode bit to LOW (N[2] = 0) and its power down mode bit to HIGH (N[1] = 1). The power down function is gated by the charge pump. Once the power down mode and counter reset mode bits are loaded, the part will go into power down mode upon the completion of a charge pump pulse event.

Asynchronous Power down Mode

The PLL loops can be asynchronously powered down by setting the counter reset mode bit to HIGH (N[2] = 1) and its power down mode bit to HIGH(N[1] = 1). The power down function is NOT gated by the charge pump. Once the power down and counter reset mode bits are loaded, the part will go into power down mode immediately.

The R and N counters are disabled and held at load point during the synchronous and asynchronous power down modes. This will allow a smooth acquisition of the RF signal when the PLL is programmed to power up. Upon powering up, both R and N counters will start at the 'zero' state, and the relationship between R and N will not be random.

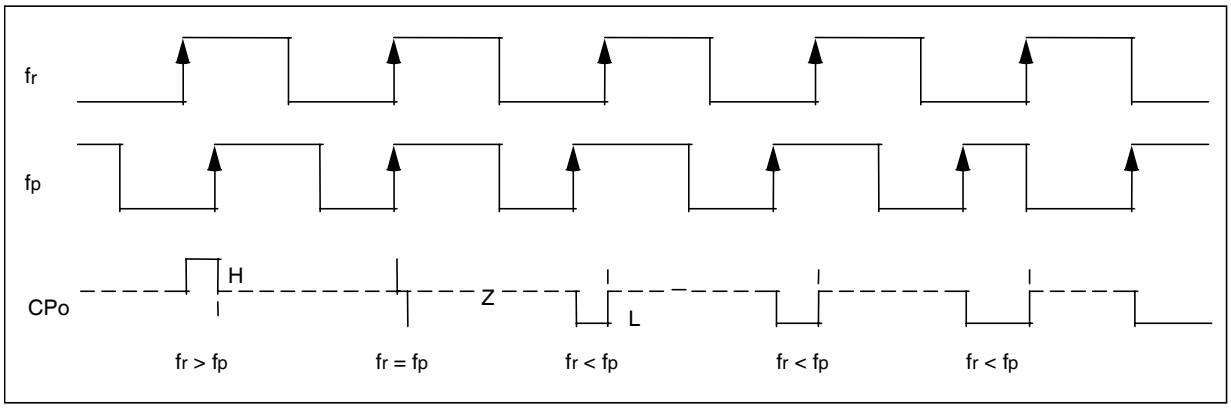
SERIAL DATA INPUT TIMING



NOTES: Parenthesis data indicates programmable reference divider data.
Data shifted into register on clock rising edge.
Data is shifted in MSB first.

TEST CONDITIONS: The Serial Data Input Timing is tested using a symmetrical waveform around Vcc/2. The test waveform has an edge rate of 0.6 V/nsec with amplitudes of 2.2V @ Vcc=2.7 V and 2.6V @ Vcc = 3.9 V.

PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



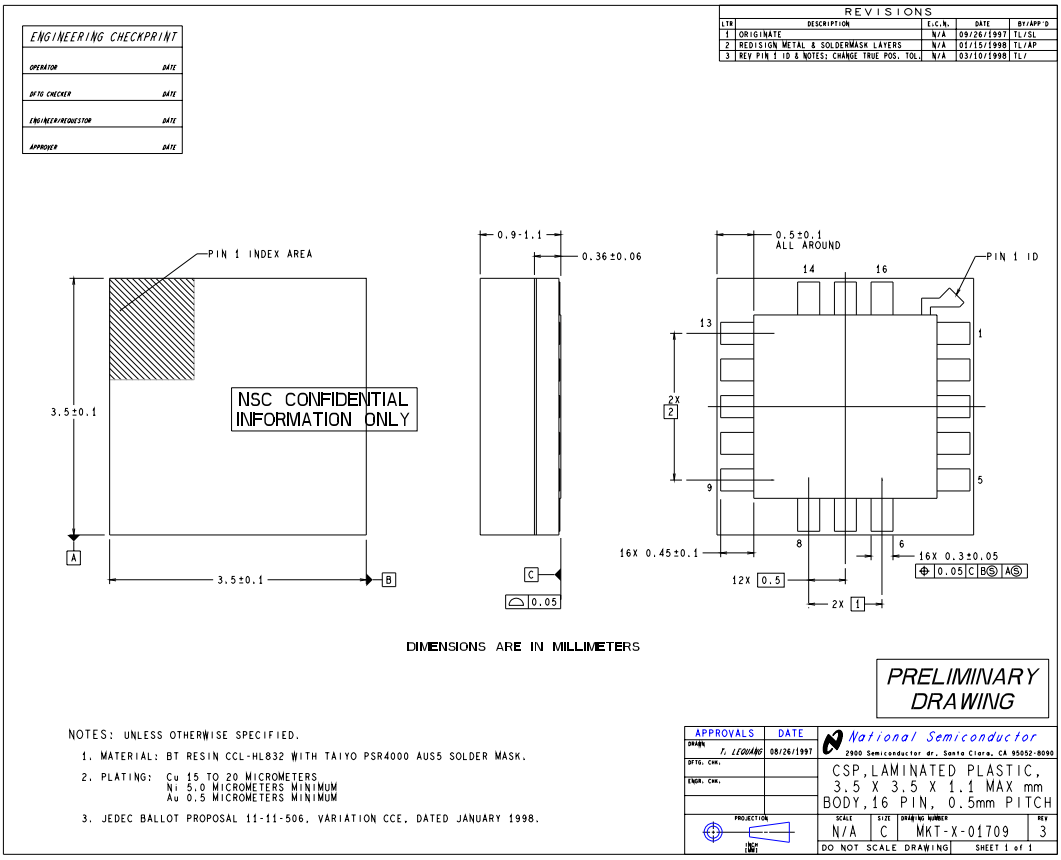
NOTES: Phase difference detection range: - 2π to + 2π
The minimum width pump up and pump down current pulses occur at the CPo pin when the loop is locked.
PD_POL = 1

f_r: Phase comparator input from the R Divider

f_p: Phase comparator input from the N divider

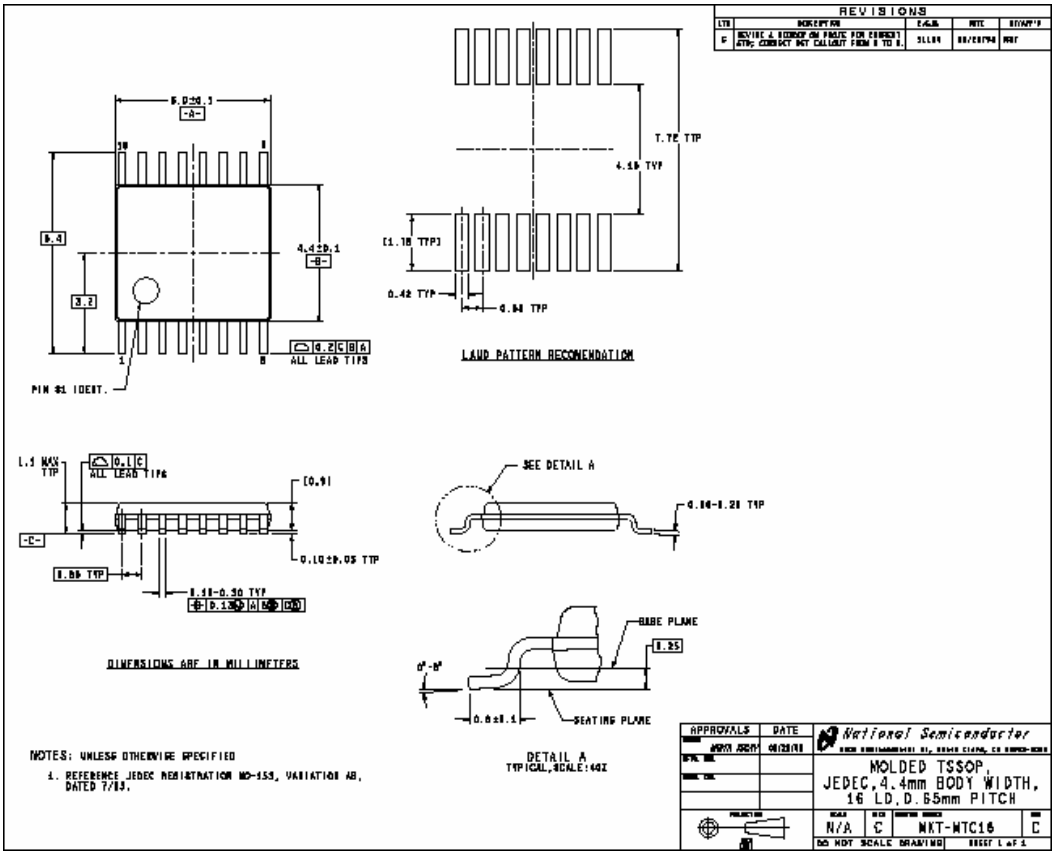
CPo: Charge pump output

Physical Dimensions



16pin Chip Scale Package

Physical Dimensions (continued)



16pin Thin Shrink Small Outline Packages