

Application Note AN-51

HiperTFS™ Family



Design Considerations

Introduction

The HiperTFS is highly integrated, very efficient integrated offline switcher IC mainly intended for PC main and standby applications. The IC includes the control, drivers and switches for a two-switch forward high power main converter and the control and power switch for a flyback standby converter. A minimal count of external components are required for full operation. The HiperTFS package (eSIP-16B) requires no electrical isolation of the exposed back tab, enabling direct mounting to a heat sink for maximally effective heat sinking and minimal mounting hardware. The HiperTFS series covers a range from 170 W to 415 W continuous power output (at 25 °C ambient) and in applications such as PC power supplies which require very dense and compact layout and high efficiency. HiperTFS provides significant advantages to the designer whether it be for 70 PLUS, 80 PLUS or 80 PLUS Bronze compliant designs.

The main forward converter is intended to work with a PFC boost front end provides a regulated voltage from 290 VDC to 420 VDC input (385 VDC typical). The standby section of HiperTFS is intended for wide range operation from 100 VDC to 420 VDC. High efficiency is made possible by using an asymmetrical version of the two-switch forward which allows an operating duty cycle greater than 50%, hence lower RMS switch currents and lower output diode voltage ratings. A proprietary protection circuit guarantees safe operation by limiting the forward

transformer single cycle flux and guaranteeing transformer reset, eliminating transformer saturation under all conditions. Special functions include OVP latch for standby, remote-ON/OFF capability for the main converter, programmable maximum primary current limit ranges for main and standby supplies, frequency jitter for low EMI, and flat standby output overload characteristics with respect to input voltage.

Basic Circuit Configuration

The circuit shown in Figure 1 shows the basic configuration of a PC power supply design using HiperTFS, including main and standby converters. The high level of integration of HiperTFS, provides many of the needed functions that would otherwise require external circuitry saving development time and material costs. One common external circuit configuration is useful for a range of applications. Advanced features like line undervoltage and overvoltage protection, reset and flux density limiter for main transformer, external current limit selection, start-up features, and remote-ON/OFF are easily implemented with a minimal number of external components.

Other application specific issues such as constant current, and constant power outputs, etc. are beyond the scope of this design guide. However, if required such specifications may be satisfied by adding additional circuitry to the basic converter configuration.

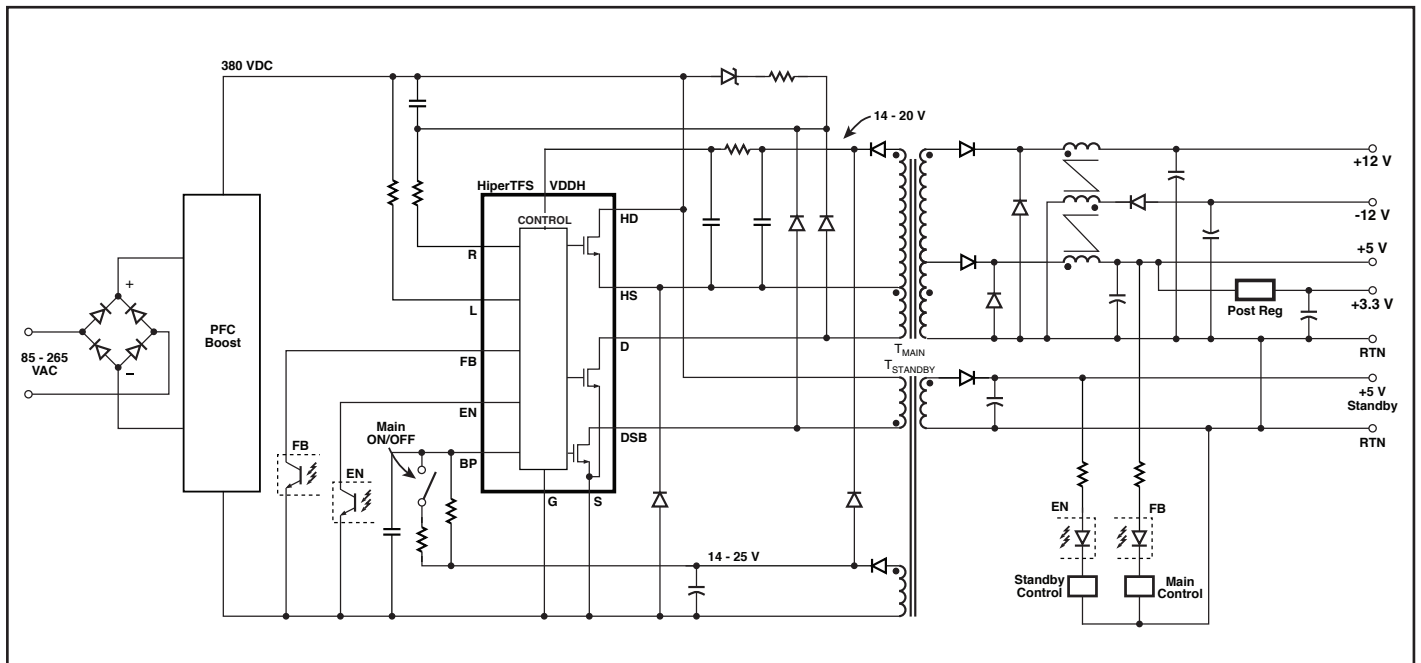


Figure 1. A Simplified Schematic of HiperTFS With PC Main Supply With 3.3 V, 5 V, 12 V, -12 V and One +5 V Standby Output.

Scope

This application note is intended for engineers designing an isolated AC-DC forward power supply with flyback standby using the HiperTFS family of devices. It is assumed that there is a power factor converter boost stage (HiperPFS) providing 385 VDC to the input of the main converter. The standby converter must operate with the PFC boost stage both on or off so the standby has a wide DC operating input range of 100 VDC to 420 VDC. For detailed information on PFC stage refer to HiperPFS application note. Guidelines and a step-by-step walk through of the HiperTFS design spreadsheet are given to enable an engineer to quickly select key components and design a suitable main transformer, standby transformer and main output inductor design for a PC power supply. This application note refers directly to the PIXIs design spreadsheet that is part of the PI Expert™ design software suite. The basic configuration used in PC power supply is shown in Figure 1, which also serves as the reference circuit for component identifications used in the description throughout this application note.

In addition to this application note the reader may also find the HiperTFS Reference Design Kit (RDK-249) containing an engineering prototype board, engineering report and device samples useful as an example of a working power supply. There is also an engineering report available describing a full multiple output design for PC main applications. Further details on downloading PI Expert, obtaining a RDK and updates to this document can be found at www.powerint.com.

Overview of Design Method

Readers needing to start immediately can use the following information to quickly design the transformer and select the components for a first prototype. The information described below needs to be entered into the PIXIs design spreadsheet. Other parameters will be automatically selected based on a typical design. References to spreadsheet cell locations are provided in square brackets [cell reference].

Design Using PIXIs

Description of PIXIs Format

There are four major sections in this spreadsheet:

1. Input parameters and device selection and device configuration.
2. Transformer core selection and winding design for main forward converter.
3. Output coupled inductor core size and core material selection and winding design for main forward.
4. Standby transformer design.

Each of these sections have grayed cells that are locations for user enterable parameters. When PIXIs is first opened these grayed cells will contain default values already entered for a typical 300 W output main 17 W output standby design. The designer is advised to leave these cells unchanged unless they have more precise information.

Output Voltages and Currents of Main Converter

There are commonly four output voltages provided by a PC main converter. These are +5 V, +12 V, +3.3 V and -12 V. The main transformer usually has only two output windings which source the +5 V and +12 V outputs. The outputs of these two windings are rectified and drive the input of a coupled main output inductor. The third output, commonly a 3.3 V output, is derived from a switching post regulator, which is typically a mag amp sourced from the +5 V winding or a synchronous buck converter sourced from the +12 V output. Finally, there is commonly a -12 V output sourced from a flyback winding on the coupled output inductor (intended for light loads only).

Section 1 – Input Parameters, Device Selection and Device Configuration

Step 1 – Enter Output Current and Voltages

*note

brackets [] indicate actual spreadsheet name

parentheses () indicates typical value

- Enter output current and voltage values for $[V_{MAIN}]$ and $[I_{MAIN}]$ (+12 V).
- *note - V_{MAIN} is highest power output.
- Enter output current and voltage values for $[V_{OUT2}]$ and $[I_{OUT2}]$ (+5 V).
- Enter output current and voltage values for post regulator $[V_{OUT3}]$ and $[I_{OUT3}]$ (+3.3 V).
- Select type of post regulation [Post Regulator] (MAG AMP, Buck or NONE).
- If buck post regulator is selected enter estimated efficiency of buck stage $[n_{PR}]$. This is ignored if MAG AMP was chosen.
- Enter voltage and current of inductor derived output (-12 V), $[V_{OUT4}]$ and $[I_{OUT4}]$.
- $[P_{OUT(MAIN)}]$ is the total maximum output power of the main converter which is the sum of the output power of all main converter outputs.
- If there is a peak power requirement then enter the peak power in $[P_{OUT_PEAK(MAIN)}]$. The additional power over continuous maximum output power is assumed to be sourced from V_{MAIN} .
- $[P_{OUT(STANDBY)}]$ and $[P_{OUT_PEAK(STANDBY)}]$ have default values entered. These will later change when entering actual standby output power in standby section of spreadsheet.
- $[V_{BIAS}]$ is typically 17 V which is used for bias support of HiperTFS bootstrap high-side drive, and the source for the +12 V regulator which is used for remote, ON/OFF and bias for HiperPFS boost controller. Changing the target voltage of V_{BIAS} could be detrimental to supply performance.

HiperTFS MAIN OUTPUT (TWO-SWITCH FORWARD STAGE)				
OUTPUT VOLTAGE AND CURRENT				
VMAIN	12.00		V	Design Title
IMAIN	15.00		A	Main output voltage
VOUT2	5.00		V	Main output current
IOUT2	15.00		A	Output2 voltage
POST REGULATED OUTPUT				
Post Regulator	MAG-AMP			Output2 current
V_SOURCE	5.00		V	Select post regulator from Mag-Amp or Buck
VOUT3	3.30	3.3	V	Select source of input voltage for post regulator
IOUT3	10.00	10.0	A	Enter postregulator output voltage
n_PR		1		Enter post rehelator output current
COUPLED-INDUCTOR (LOW POWER) DERIVED OUTPUT				
VOUT4	12.00		V	Enter postregulator efficiency (Buck only)
IOUT4	0.10		A	Coupled-Inductor derived (low power) output voltage (typically -12 V)
POUT(Main)		289.2	W	Coupled-Inductor derived (low power) output current
POUT_PEAK(Main)		289.2	W	Total output power (Main converter)
POUT(Standby)		10.3	W	Peak Output power(Main converter). If there is no peak power requirement enter value equal to continuous power
POUT_PEAK(Standby)		17.5	W	Continuous output power from Standby power supply
POUT(System Total)		299.5	W	Total system continuous output power
POUT_PEAK(System Total)		306.7	W	Peak output power from Standby section
VBIAS	17.00		V	Total system peak output power
				DC bias voltage from main transformer aux winding

Figure 2. Main Converter Design Parameters.

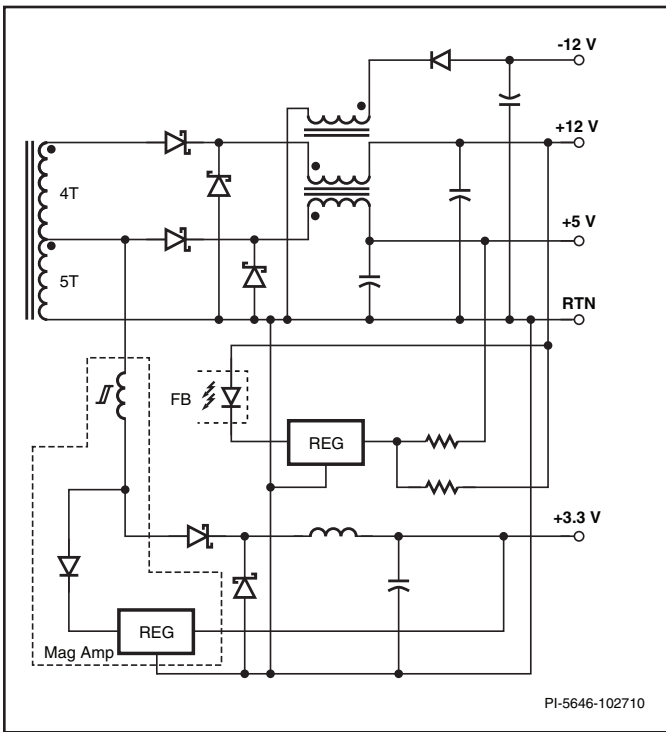


Figure 3. Typical Output Configurations for Post Regulator. Mag Amp Regulated.

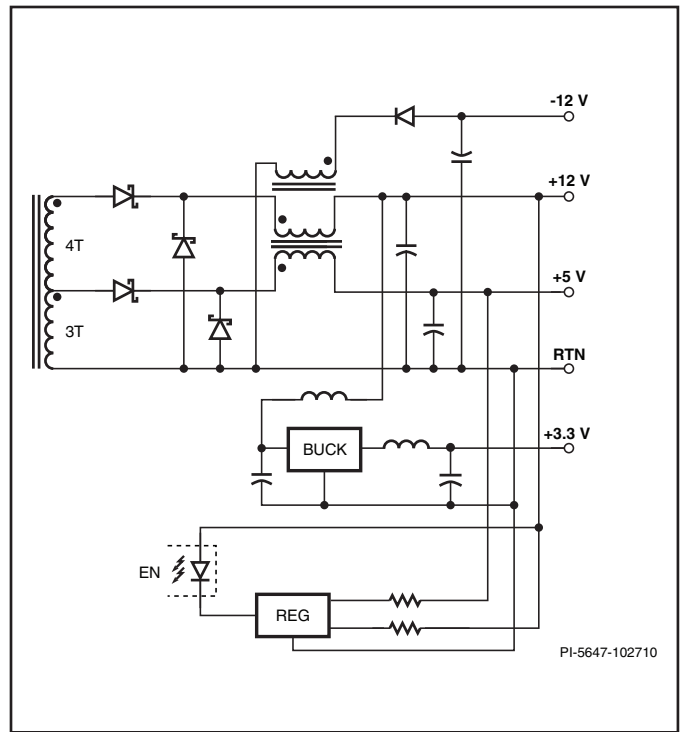


Figure 3a. Typical Output Configurations for Post Regulator. Buck Regulated.

Undervoltage Lockout and Hold-Up Time

The DC input voltage to the converter is sensed by the LINE-SENSE (L) pin which receives current from the line sense resistor. The line sense resistor is typically 4 MΩ and the chart below shows the UV threshold for the Standby and Main converters with this value. Also note that there is a fixed 12 ms delay between the time [V_{OV(NOM)}] is reached for the main converter and the actual start of main converter switching (this gives time for the PFC output voltage to settle).

Critical inputs for determining hold-up time [T_{HOLDUP}] are the nominal operating voltage [V_{NOM}] and the minimum input voltage [V_{MIN}] that guarantees regulation at maximum specified continuous output power. By specifying a holdup time at a given output power and knowing V_{NOM} and V_{MIN}, the input minimum output capacitor can be computed.

$$C_{MIN} = \frac{2 \times P_{OUT_TOTAL} \times T_{HOLDUP}}{0.86 \times ((V_{NOM})^2 - (V_{MIN})^2)}$$

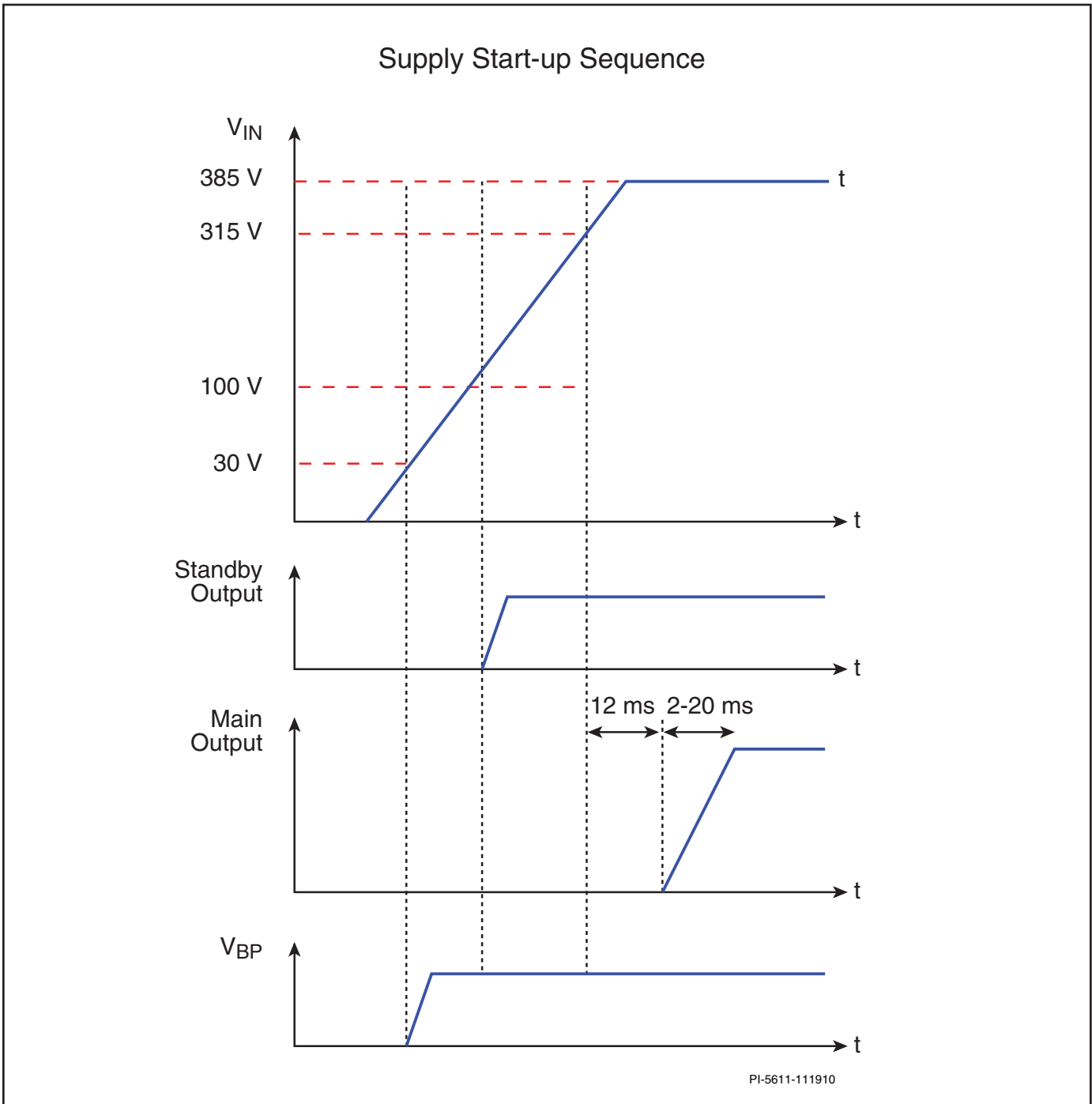


Figure 4. Power Supply Start-Up Sequence (Voltages Shown Assume a 4 MΩ Line Sense Resistor).

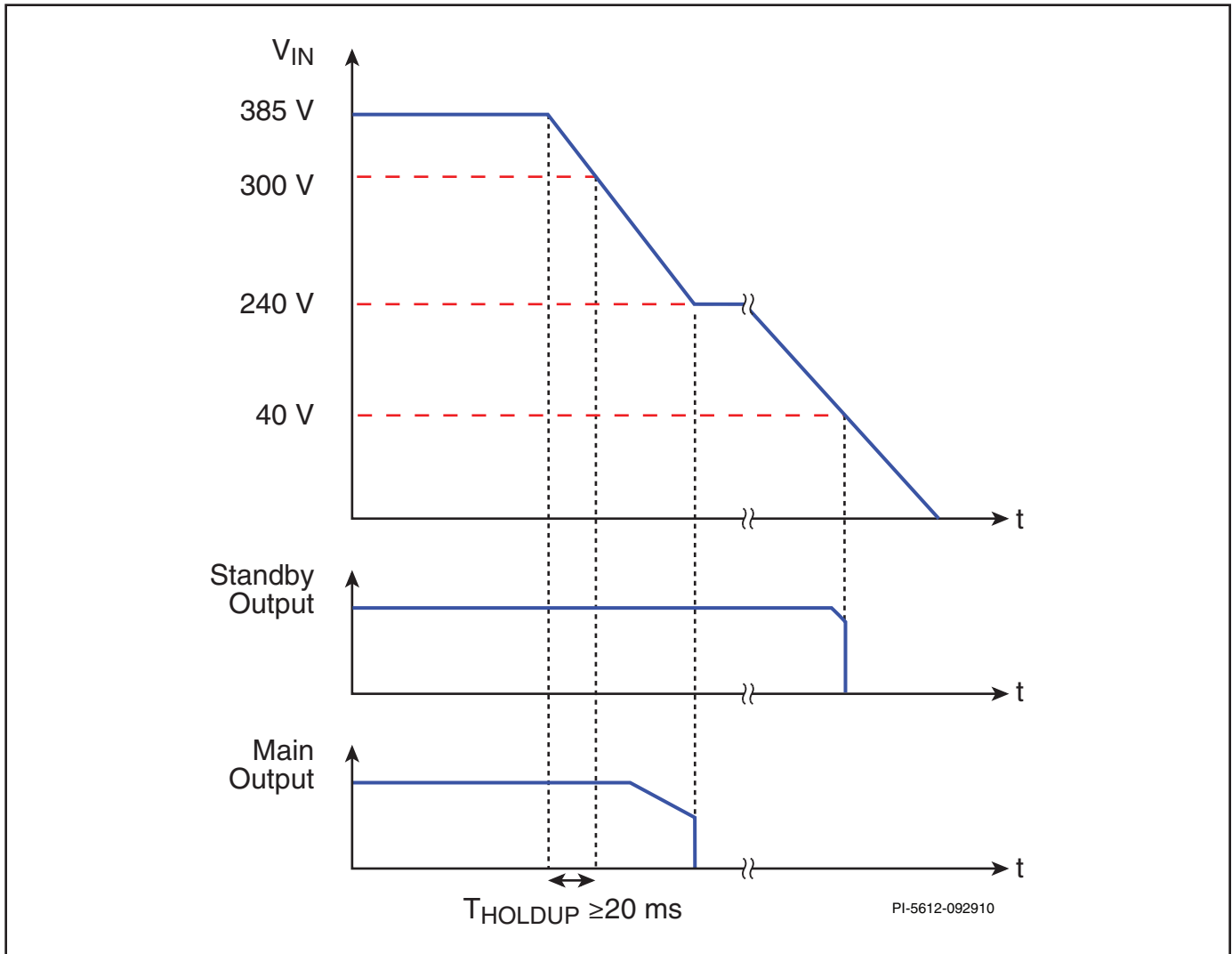


Figure 5. Power Supply Shutdown Sequence (AC Turn-Off).

Step 2 – Hold-Up Time and Input Voltage Range

Below are the steps for defining hold-up time and input voltage range.

- Enter desired minimum holdup time $[T_{\text{HOLDUP}}]$ at maximum continuous output power $[P_{\text{OUT(SYSTEM TOTAL)}}]$.
- Enter minimum $[V_{\text{MIN}}]$ and nominal $[V_{\text{NOM}}]$ input voltages to define regulation range for the forward converter. $[V_{\text{NOM}}]$ is the nominal output voltage from the PFC boost stage DC bus.
- After these values are entered view $[C_{\text{IN}}]$ to see the minimum required input capacitance. If nothing is entered for $[V_{\text{MIN}}]$, $[V_{\text{NOM}}]$ and $[T_{\text{HOLDUP}}]$ the spreadsheet will show default values $[V_{\text{MIN}}] = 300$, $[V_{\text{NOM}}] = 385$, and $[T_{\text{HOLDUP}}] = 20$ ms. If desired holdup time is different than the default value, then enter required holdup time $[T_{\text{HOLDUP}}]$ and check required $[C_{\text{IN}}]$.
- Enter maximum input voltage $[V_{\text{MAX}}]$. This is used to determine maximum voltage stress on switching components.
- R_{R} and R_{L} are computed resistor values for L and R pin functions which include $[V_{\text{UV(ON)}}]$ and $[V_{\text{UV(OFF)}}]$. The default values are 4 M Ω . These values normally do not need adjusting.
- $[V_{\text{UV(ON)}}]$ is the start-up threshold for the main converter and $[V_{\text{UV(OFF)}}]$ is the shut down threshold for the main converter.
- The values of R_{R} and R_{L} are nominally 4 M Ω unless an override value is entered for R_{L} . Entering a different value for R_{L} which will create a new identical value for R_{R} . Lowering R_{L} and R_{R} value will lower both $V_{\text{UV(ON)}}$ and $V_{\text{UV(OFF)}}$ threshold, but will also reduce maximum operating duty cycle $[D_{\text{MAX}_{\text{VNOM}}}]$ and $[D_{\text{MAX}_{\text{VMIN}}}]$. A value that is too low will usually cause the spreadsheet to flag inadequate hold-up time. A value higher than 4 M Ω is not advised as this may cause the spreadsheet to flag core reset problems $[BP_{\text{MAX}}]$.

INPUT VOLTAGE AND UV/OV					
CIN			262.23	uF	Input Capacitance. To increase CMIN, increase T_HOLDUP
T_HOLDUP			20.00	ms	Holdup time
VMIN			300	V	Minimum input voltage to guarantee output regulation
VNOM			380	V	Nominal input voltage
VMAX			420	V	Maximum DC input voltage
UV / OV / UVOV		min			
VUV OFF		236.0	287.9	V	Minimum undervoltage On-Off threshold
VUV ON		300.0	344.7	V	Maximum undervoltage Off-On threshold (turn-on)
VOV ON		480.4	-	V	Minimum overvoltage Off-On threshold
VOV OFF		664.5	-	V	Minimum overvoltage On-Off threshold (turn-off)
RR			4.03	M-ohm	R pin resistor
RL			4.03	M-ohm	Line Sense resistor value (L-pin) - goal seek (VUV OFF) for std 1% resistor series

Figure 6. Power Supply Under/Overvoltage and Input Capacitor Parameters.

Step 3 – Selecting HiperTFS Device, Current Limit Setting and KDI Goal and Clamp Selection

There are several HiperTFS devices available in the family. The appropriate device depends on the output power, type of application and thermal environment. For example in PC power supplies two different ambient requirements are commonly used. Original equipment manufacturer (OEM) power output is specified at 50 °C ambient where as clones typically are specified at 25 °C ambient. Table 1 shows which device is best suited for a given ambient temperature. There is also the option to select one of three current limit values. Selection is made by entering a value for KI [KI] of either 1, 0.8 or 0.6. These values correspond to the data sheet parameters $I_{LIM(3)MA}$, $I_{LIM(2)MA}$ and $I_{LIM(1)MA}$ respectively. The resultant minimum device current limit is shown in cell [LIMITSELECT]. Implementing the selected KI is achieved by selecting the value of pull-up resistor from the FEEDBACK to the BYPASS pin of the HiperTFS device. [R_{FB}] shows the appropriate value for the pull-up resistor for the selected KI. Table 2 shows the relationship between I_{FB} and selected current limit.

Output Power Table

Part Number	P _{OUT} T _A = 25 °C	P _{OUT} T _A = 50 °C	P _{OUT} PK	P _{OUT} Standby
TFS757HG	193 W	163 W	228 W	20 W
TFS758HG	236 W	200 W	278 W	20 W
TFS759HG	280 W	235 W	309 W	20 W
TFS760HG	305 W	258 W	358 W	20 W
TFS761HG	326 W	276 W	383 W	20 W
TFS762HG	360 W	304 W	407 W	20 W
TFS763HG	388 W	327 W	455 W	20 W
TFS764HG	414 W	344 W	530 W	20 W

Table 1. HiperTFS Output Power Table.

I _{FB} (Threshold)	Datasheet Parameters	Percent of I _{LIM(3)MA}	R _{FB} (1%)	
0.0-5.1 μA	I _{LIM(1)MA}	60	Open	
5.1-11.9 μA	I _{LIM(2)MA}	80	511.0	kΩ
11.9-23.8 μA	I _{LIM(3)MA}	100	232.0	kΩ

Table 2. FEEDBACK Pin Main Current Limit Selection.

For a two-switch Forward topology, power is delivered during the on-time of the main switches. During the off-time, both leakage and magnetizing energy in the main transformer must

be reset and recovered in a safe manner. There are two options for main transformer reset within [CLAMP SELECTION]: clamp-to-rail and clamp-to-ground (see Figure 7 for both clamp schematics). Clamp-to-rail clamps the bottom main switch to a constant value above the input DC bus (385 VDC). This is the simplest and least expensive clamp method and also has the convenience of allowing the standby converter to share the clamp network. Clamp-to-ground is the second option which creates a constant reset voltage with respect to primary ground and has the advantage of allowing wider nominal operating duty cycle, which offers either the advantage of lower RMS current for the primary main switches of HiperTFS or allows the use of a smaller input bulk capacitor. The default nominal duty cycle [D_{VNOM}] for clamp-to-rail is 0.45 and the default for clamp-to-ground is 0.49.

Step 4 – Spreadsheet Procedure for Device Selection and Configuration

- Review the output power table and decide appropriate HiperTFS device depending on application, ambient temperature and output power.
- Select HiperTFS device [DEVICE] from drop down list.
- Selected HiperTFS device and key device parameters are displayed [Line 42-48].
- Select primary current limit factor [KI]. 1, 0.8, 0.6. [LIMIT] default value is 1.
- The default nominal operating duty cycle is 45% for clamp-to-rail. Notice from Figure 7 the circuit includes a 150 V Zener. This allows a maximum duty cycle at V_{MIN} to be greater than 58% for the example spreadsheet shown. [D_{MAX} V_{MIN}] is typically 60% for clamp-to-rail setting. The value of the clamp Zener is selectable; however, a value range from 130 V to 150 V is advised. Care should be taken when entering a duty cycle higher than 45% for clamp-to-rail as it may cause a T_{HOLDUP} warning. Generally higher nominal operating duty cycles require changing the clamp mode to clamp-to-ground to increase reset voltage across transformer during brownout. A nominal operating duty cycle of up to 50% can be achieved with clamp-to-ground. The default value of [V_{CLAMP}] in clamp-to-ground configuration is 530 V.

Another option to allow higher operating duty cycle is to raise V_{MIN} for the same holdup time and use a higher C_{IN} value. Note that in both configurations of clamp circuit DR1 is a slow recovery diode (1N4007G) which allows recycling of the magnetizing and leakage energy. A 1N4007G which is glass passivated is preferred over 1N4007 because it has well controlled reverse recovery characteristics. Using a slow recovery diode rather than a fast recovery type increases overall

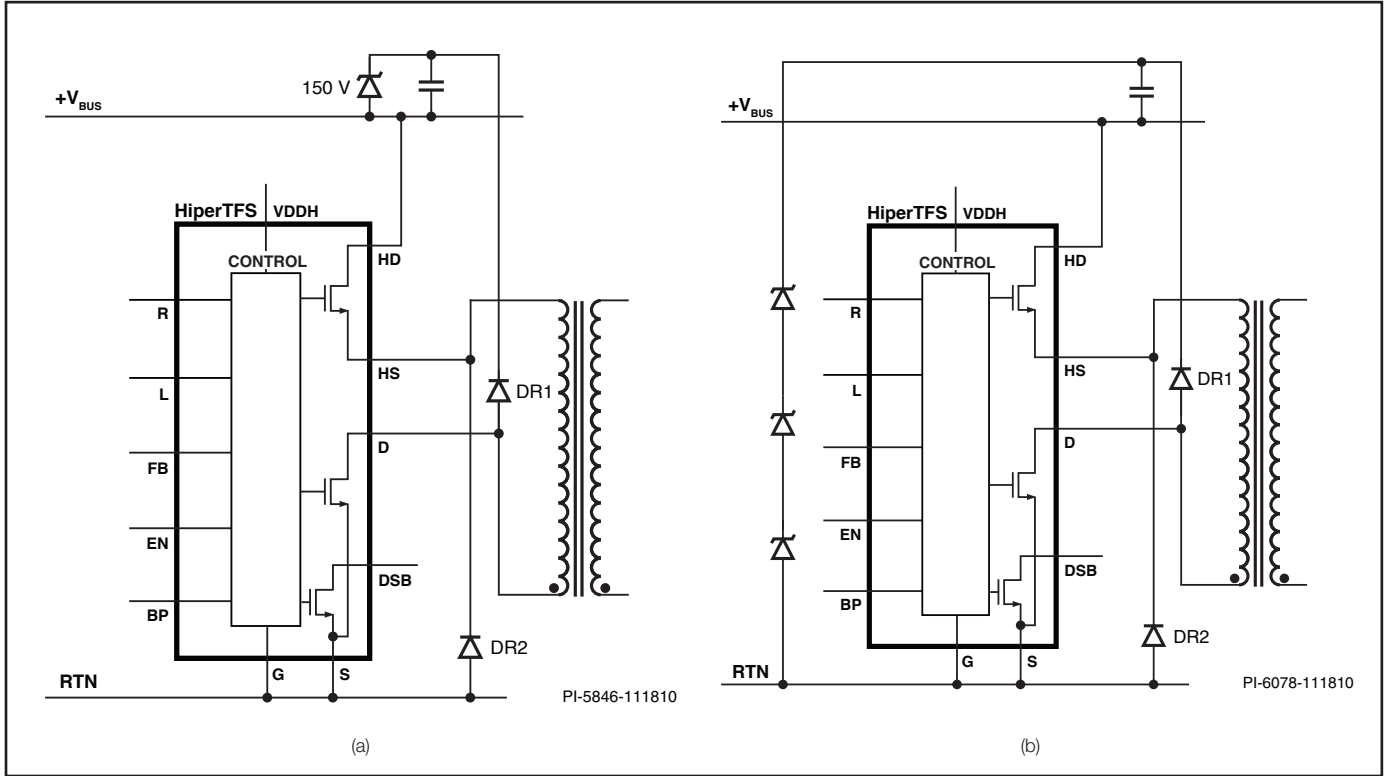


Figure 7. Clamp-to-Rail (a) and Clamp-to-Ground (b).

ENTER DEVICE VARIABLES					
Device	TFS762				Selected HiperTFS device
Chosen Device			TFS762		
ILIMIT_MIN			3.25	A	Device current limit (Minimum)
ILIMIT_TYP			3.50	A	Device current limit (Typical)
ILIMIT_MAX			3.75	A	Device current limit (Maximum)
fSMIN			61500	Hz	Device switching frequency (Minimum)
fS			66000	Hz	Device switching frequency (Typical)
fSMAX			70500	Hz	Device switching frequency (Maximum)
KI	1.0		1.0		Select Current limit factor (KI=1.0 for default ILIMIT, or select KI=0.8 or KI=0.6)
R(FB)			232.0	k-ohms	Feedback Pin Resistor value
ILIMIT_SELECT			3.25	A	Selected current limit
RDS(ON)			2.73	ohms	Rds(on) at 100°C
DVNOM_GOAL			0.45		Target duty cycle at nominal input voltage (VNOM)
VDS			4.80	V	HiperTFS average on-state Drain to Source Voltage
Clamp Selection	CLAMP TO RAIL				Select either "CLAMP TO RAIL" (default) or "CLAMP TO GND"
VCLAMP			150.00	V	Asymmetric Clamp Voltage
VDSOP			570.00	V	Maximum HiperTFS Drain voltage (at VOVOFF_MAX)

Figure 8. HiperTFS Main Current Limit, Device Selection and Other Design Parameters.

efficiency and reduces dissipation of clamp Zener (D3) by recycling energy clamp. The bottom catch diode DR2 is typically an ultra fast type rectifier (UF4005).

Prevention of Core Saturation by LINE-SENSE and RESET Pin Maximum Duty Cycle Limit Function

By sensing the input voltage through the LINE-SENSE pin and the clamp voltage through the RESET pin, HiperTFS can determine the duty cycle boundary for safe operation and will limit the maximum duty below this level. Figure 9 shows the allowable duty cycle range as a function of V_{IN} .

Saturation of the main transformer can commonly occur by one of two possible mechanisms:

1. Lack of sufficient reset volt-seconds for the core during the off-time.

2. Applying excessive volt-seconds to the core during the on-time cycle.

HiperTFS safely limits the duty cycle to avoid these two possible conditions.

The equations below determine the maximum duty cycle allowed by LINE-SENSE and RESET pin limiter for reset of core.

Clamp-to-Rail:

$$D_{MAX_FORWARD(VMIN)} = \frac{V_{CLAMP} + (V_{MIN} - V_{DS})}{2(V_{MIN} - V_{DS}) + V_{CLAMP}}$$

Clamp-to-Ground:

$$D_{MAX_RESET(VMIN)} = \frac{V_{CLAMP}}{(V_{MIN} - V_{DS}) + V_{CLAMP}}$$

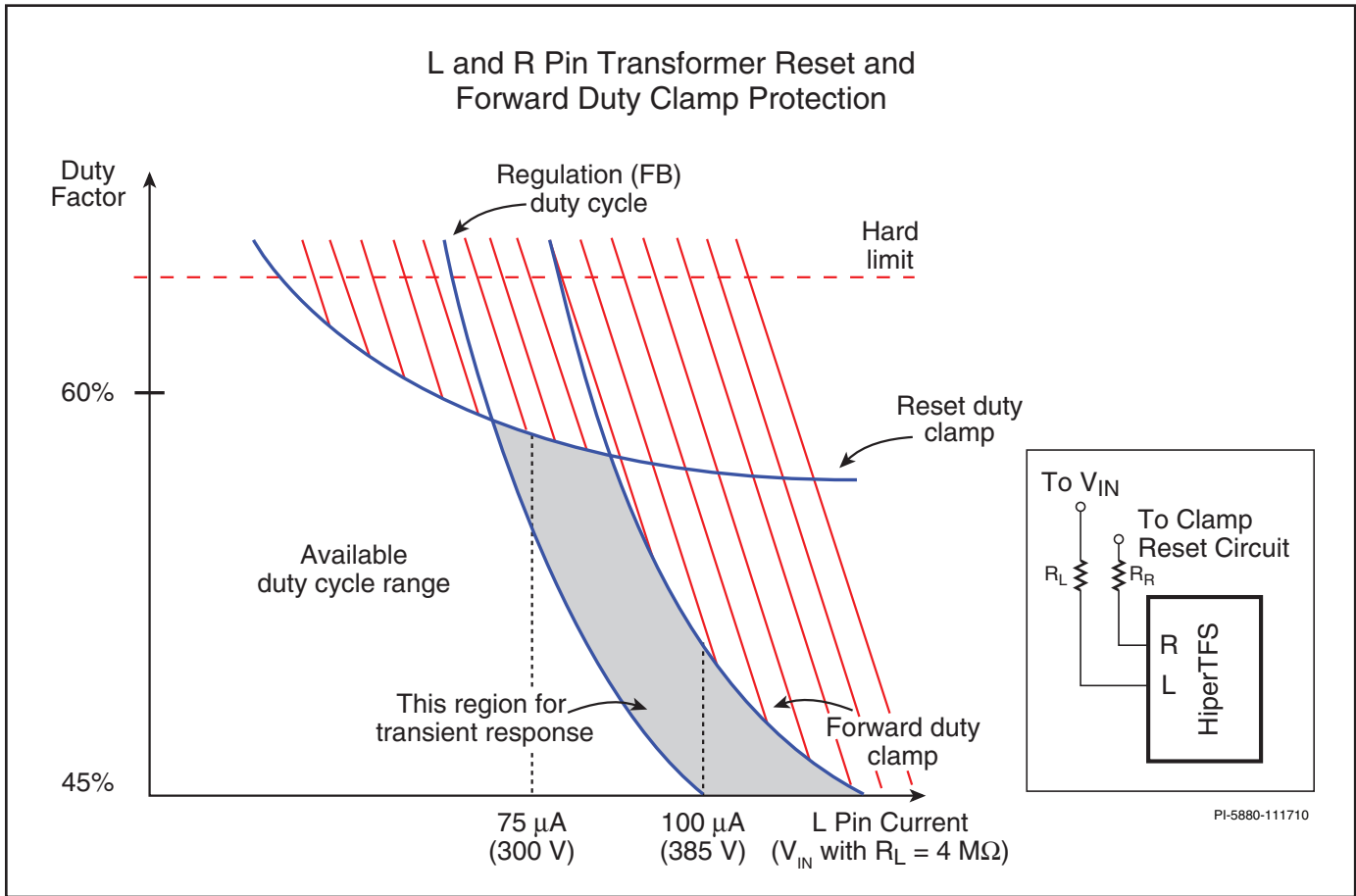


Figure 9. Duty Cycle Limiter (Clamp-to-Rail using 150 V Zener Diode Network).

The equation below determines the maximum duty cycle allowable to avoid excessive peak flux density resulting from on-time volt-seconds.

$$D_{MAX(ON)} = \frac{5.2 \times 10^{-5} \times R_L}{V_{IN(MAX)}}$$

Step 5 – Output Diode Selection

- Select appropriate diodes for the various outputs. Figure 10 shows typical forward voltage drops used for diodes +5 V, +12 V, +3.3 V, and standby. Depending on output current and data sheet values for diode forward voltage drop, the section below allows the designer to enter expected voltage drop

across output diode at maximum continuous output current for that output. These values will effect computed nominal duty cycle and turns ratio of main transformer.

- The default values for output diodes are 0.5 V for Schottky and 0.7 V for PN junction type. For a lower forward drop Schottky enter appropriate value [B62-B65].

Keep in mind that the wide operating duty cycle of HiperTFS results in a lower peak output diode reverse voltage for the output catch diode. Choose diodes with lower reverse voltage to take advantage of lower V_f (and lower dissipation) where possible.

DIODE Vf SELECTION					
VDMAIN			0.5	V	Main output diodes forward voltage drop
VDOUT2			0.5	V	Secondary output diodes forward voltage drop
VDOUT3			0.5	V	3rd output diodes forward voltage drop
VDB			0.7	V	Bias diode forward voltage drop

Figure 10. Output Diode Forward Voltage Parameters.

Step 6 – Choose Core and Bobbin Based on Output Power and Enter A_E , L_E , A_L , BW , M , L , N_S

- When a core is selected, key parameters of the core are displayed, including A_E , L_E , A_L , BW and L_G . The default selected core is an EER35 and the default main output turns [N_{MAIN}] is 7 which is a typical core and turn set used for a 250-400 W PC application. EER28L is the smallest allowable core where N_{MAIN} can be set to 7 turns for +12 V main output without violating maximum allowable flux density. Select a core [CORE TYPE] and secondary turns [N_{MAIN}], check [BM_{MAX}] in the transformer design parameters section to determine whether flux density and current density are within safe limits. The spreadsheet will flag a warning if there is excessive flux density or current density for main transformer core.
- If a core of interest does not exist in the spreadsheet drop down list then enter specific core parameters from vendor data sheet directly into the spreadsheet.
- The default value is 7 turns for (+12 V) output. 7 turns creates a well centered ratio with N_{S2} (+5 V) at 3 turns. N_{S2} is computed by the spreadsheet to give the closest value possible to the [V_{OUT2}] target. V_{OUT2_ACTUAL} and V_{BIAS_ACTUAL} are the actual computed values of those outputs relative to the selected value of V_{MAIN} and the entered value of [V_{OUT2}]. There is an option to override the default turns for [N_{S2}], but it should be appreciated that the limitation of practical integral secondary turns values means that no solution will be perfect and that improved centering between V_{MAIN} and V_{OUT2_ACTUAL} may not be possible by simply changing N_{S2} .

- Enter number of primary layers. The default value is 3. Increasing layers should be avoided as it will increase the leakage inductance and possibly reduce current density (CMA), both aspects making the transformer less efficient.
- Enter the safety margin width. This parameter is half of the total primary plus secondary safety margin. For designs that have asymmetric 6 mm spacing on pin side and 3 mm spacing on non-pin side (a total of 9 mm), enter 4.5 mm in [BW].
- The items in the rows below are computed values for transformer design parameters including total primary turns [N_p] and peak flux density of core. [BM_{MAX}] is the nominal absolute peak flux excursion during normal operation. [BP_{MAX}] is the absolute peak flux excursion allowed by the L and RESET pin reset limiter circuit. The external clamp circuit, including the standard recovery diode DR1 (Figure 7) and the effective primary winding capacitance help set the core flux significantly negative at the end of the reset (off-time) cycle. This is why [BM_{MAX}] and [BP_{MAX}] are a lower value than [BM PK-PK] and [BP PK-PK]. [BM_{MAX}] and [BP_{MAX}] are important parameters to determine flux density margin below core saturation during transient conditions. [BM PK-PK] and [BP PK-PK] are useful for determining core loss.

TRANSFORMER CORE SELECTION					
Core Type	EER35				Selected core type
Core		EER35		P/N:	PC40EER35-Z
Bobbin		EER35_BOBBIN		P/N:	BEER-35-1116CPH
A_E			1.07	cm ²	Core Effective Cross Sectional Area
L_E			9.08	cm	Core Effective Path Length
A_L			2770	nH/T ²	Ungapped Core Effective Inductance
BW			26.1	mm	Bobbin Physical Winding Width
M			4.5	mm	Bobbin safety margin tape width (2 * M = Total Margin)
LG MAX			0.002	mm	Maximum zero gap tolerance, default 2um
L			3.00		Transformer primary layers (split primary recommended)
NMAIN			7.0		Main rounded turns
NS2			3.0		Vout2 rounded secondary turns (AC stacked winding)
NBIAS			5		VBias rounded turns (forward bias winding)
VOUT2 ACTUAL			4.9	V	Approximate Output2 voltage of with NS2 = 3 turns (AC stacked secondary)
VBIAS ACTUAL			16.2	V	Approximate Forward Bias Winding Voltage at VMIN with NB = 5 turns

Figure 11. Main Transformer Core Parameters.

TRANSFORMER DESIGN PARAMETERS					
NP			89		Primary rounded turns
BM_MAX			1791	Gauss	Max positive operating flux density at minimum switching frequency
BM_PK-PK			2714	Gauss	Max peak-peak operating flux density at minimum switching frequency
BP_MAX			2310	Gauss	Max positive flux density at Vmax (limited by DVMAX clamp)
BP_PK-PK			3501	Gauss	Max peak-peak flux density at Vmax (limited by DVMAX clamp)
LP MIN			21.07	mHenries	Minimum primary magnetizing inductance (assumes LG MAX=2um)
IMAG			0.122	A	Peak magnetizing current at minimum input voltage
OD_P			0.58	mm	Primary wire outer diameter
AWG_P			23	AWG	Primary Wire Gauge (rounded to maximum AWG value)

Figure 12. Main Transformer Flux Density and Other Parameters.

Duty Cycle Values

The rows in Figure 13 define typical and maximum duty cycle values. The three most significant values are:

[DV_{NOM}] is the normal operating duty cycle for continuous operation at nominal input voltage.

[DV_{MIN}] is the duty cycle at the defined minimum input voltage where regulation can be maintained. [DV_{MIN}] is typically only at the end of the hold-up period as the input voltage collapses during AC shutdown.

[D_{MAX-V_{NOM}}] is the absolute maximum duty cycle allowed at nominal input voltage (limited by L and RESET pin limiter function).

Current Waveshape Parameters

Figure 15 shows the key primary switch current parameters. The main primary switch path current [I_p] during the on-time cycle is measured at maximum input voltage and maximum continuous output power. [I_{P-PEAK}] is the peak current during the defined peak output load [P_{OUT-PEAK(MAIN)}]. [I_{PRMS(NOM)}] is the RMS current flowing through the main switches at maximum continuous output power.

The primary current waveform is complex when a mag amp post regulator is used. The mag amp will cause the primary current to step to a higher amplitude after the mag inductor has switched on (saturated), connecting the source potential of the +5 V winding to the mag amp output inductor current. The diagrams below show the approach to computing RMS current that accounts for the effect of mag amp post regulator on primary RMS current. As can be seen, the first step in computation is to divide the primary current waveform into two components, one of being which is main switch current before mag amp switches and the second component after the mag amp switches on. The RMS value of these two components are calculated independently, then added in quadrature for the total RMS current value of [I_{PRMS(NOM)}].

Note: When using a buck post regulator, the current waveform is uniform, so this complication does not arise. If either [I_p] or [I_{P-PEAK}] are too high then a warning will show up in the text section that the current limit selection of HiperTFS device or device [I_{LIM}] configuration is not adequate for the

DUTY CYCLE VALUES (REGULATION)					
DV _{MIN}			0.57		Duty cycle at minimum DC input voltage
DV _{NOM}			0.45		Duty cycle at nominal DC input voltage
DV _{MAX}			0.41		Duty cycle at maximum DC input voltage
DOV _{OFF} MIN			0.26		Duty cycle at over-voltage DC input voltage(DOV _{OFF} MIN)
MAXIMUM DUTY CYCLE VALUES					
D _{MAX} UV _{OFF} MIN			0.62		Max duty cycle clamp at VU _{VOFF} MIN
D _{MAX} V _{MIN}			0.60		Max duty clamp cycle at V _{MIN}
D _{MAX} V _{NOM}			0.58		Max duty clamp cycle at V _{NOM}
D _{MAX} V _{MAX}			0.52		Max duty clamp cycle at V _{MAX}
D _{MAX} OV _{OFF} MIN			0.33		Max duty clamp cycle at VO _{VOFF} MAX

Figure 13. HiperTFS Main Duty Cycle Parameters.

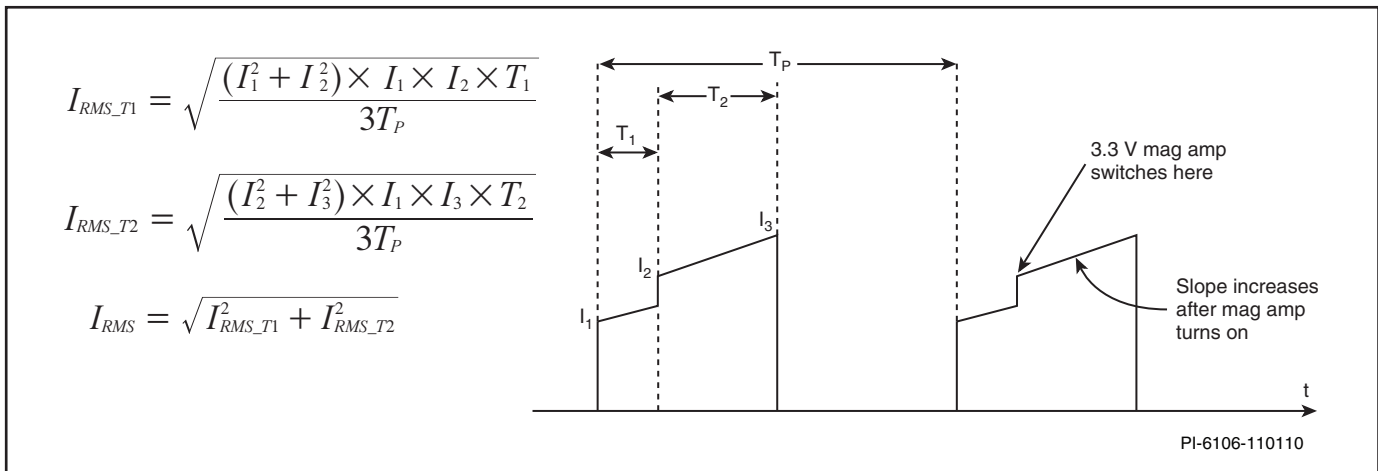


Figure 14. Primary Main Drain Current Waveshape Parameter.

required peak current. A higher current limit setting or a larger HiperTFS device will be advised. $[I_{PRMS(NOM)}]$ is helpful in computing losses for the main switches

Transformer Construction

The spreadsheet will guide proper transformer design in terms of core size, turns, wire gauge and safety margin spacing. Figure 16 below (not included in spreadsheet) shows construction of a main transformer. Aspects of a typical main transformer

design that are not shown in the spreadsheet are the use of split primary for improved coupling, and the use of foil, multi-strand or litz wire for lower R_{AC} associated losses. The secondary high current outputs are commonly foil construction. To determine required foil thickness use the RMS current information in secondary output parameters section (Figure 23) $[ISFWRMS]$ for the main output and $[ISFWD2RMS]$ for $[V_{OUT2}]$. Be sure to use appropriate thickness of foil or multi-strand to keep the current density above 200 CMA

CURRENT WAVESHAPES PARAMETERS					
IP			2.43	A	Maximum peak primary current at maximum DC input voltage
IP_PEAK			2.43	A	Peak primary current at Peak Output Power and max DC input voltage
IPRMS(NOM)			1.36	A	Nominal primary RMS current at nominal DC input voltage

Figure 15. HiperTFS Main Current Parameter.

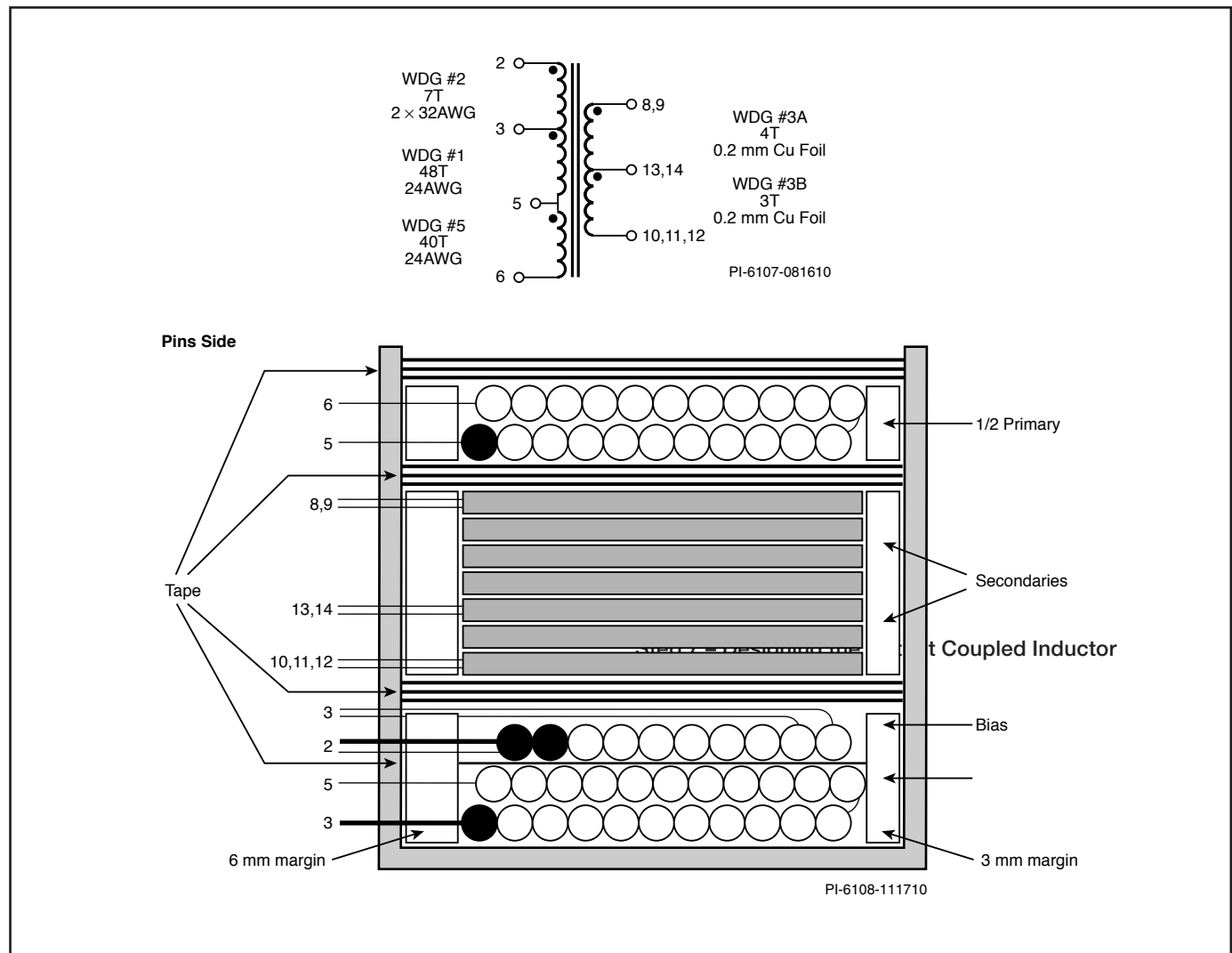


Figure 16. 300 W Main Transformer Schematic and Construction.

An essential part of designing a PC main converter is the design of the output coupled inductor. Core material and size, number of turns, and turns ratio are the major aspects of the inductor design. The output inductor should operate in continuous mode for the normal operating load range to keep good regulation between the +12 V and +5 V outputs. A coupled inductor is preferred as compared to discrete separate inductors, as it is much easier to maintain continuous conduction operation, since either output can force the core into continuous conduction mode. Powdered material such as Kool Mu or powdered iron also helps to maintain continuous conduction mode due to the non-linear A_L nature of the material, allowing the inductance to be significantly higher at lighter loads than at high load. At higher loads it is important to know the value for ripple factor (KDI) as shown in Figure 17. Excessively high ripple will cause the converter to run less efficiently from associated RMS current losses in primary converter switches, main transformer windings, output inductor windings and output capacitors. Restricting core loss of the output inductor is also an significant factor in improving efficiency. As an example, for Kool Mu, the AC peak flux density should be kept below [BAC_IND] 500 gauss.

When designing a coupled inductor, first choose the type of core material to be used. Kool Mu (Sendust) is usually the material selected for high efficiency designs. Powdered iron is generally chosen when cost is more of a factor than efficiency in overall design goals. There is an option to select ferrite material, although this material is not normally used as a coupled inductor core at 66 kHz.

Step-by-Step Procedure

- Select core material in [Core Type] from the drop down menu (optimal core size is automatically selected). Notice that there is a separate section in the spreadsheet are for powder core (Sendust and KoolMu) and ferrite computations.
- The spreadsheet automatically selects core [Core] and turns [Turns] to give a minimum core size for a KDI (ripple current factor) of approximately 0.26 and an AC flux density [BAC_IND] below 500 Gauss.
- If another core size is desired, then enter the core size in [Core]. When selecting a core other than the automatically selected size, check for excessive AC flux density warning [BAC_IND]. Also make sure KDI is below 0.5 and the layer build is below 2.
- Inductance [LMAIN_ACTUAL] and KDI of LMAIN can be changed by changing the number of turns [NMAIN_INDUC-TOR] of the main output inductor winding. The default turns for the coupled inductor is 3 times the associated main transformer secondary turns. To change inductor turns, enter a multiplier value [INDUCTOR TURNS MULTIPLIER] other than the default 3X. When selecting a multiplier other than the default value, check for an excessive AC flux density warning [BAC_IND]. Also make sure KDI is below 0.5 (to maintain continuous inductor operation) and the layer build is below 2.

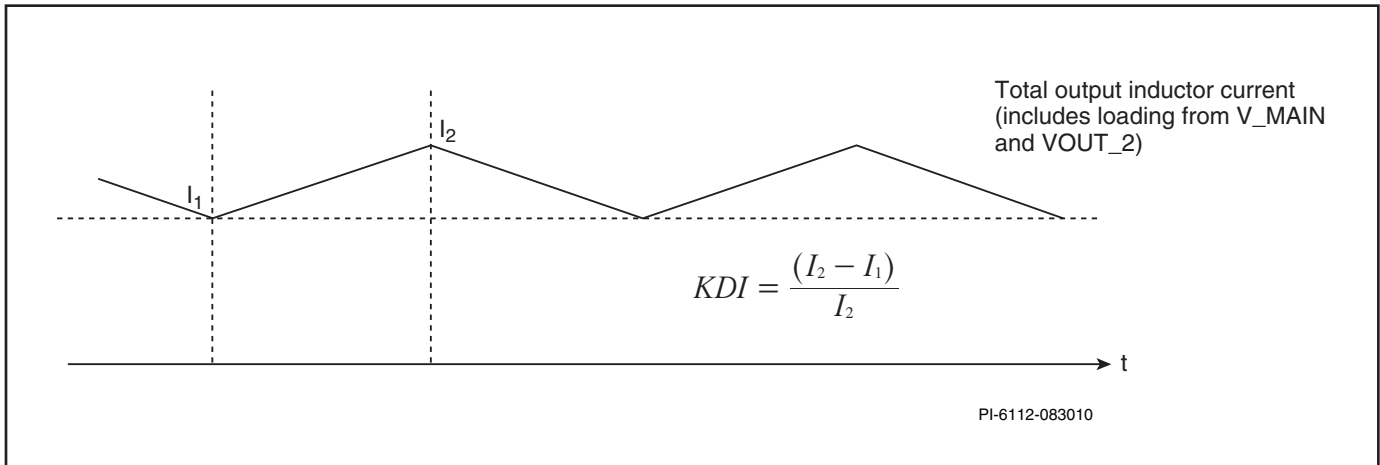


Figure 17. Secondary Coupled Inductor Current Waveshape.

OUTPUT INDUCTOR OUTPUT PARAMETERS					
KDI ACTUAL			0.28		Current ripple factor of combined Main and Output2 outputs
Core Type	Auto Auto		Kool Mu 125u		Select core type
Core			77930(O.D)=27.7)		Coupled Inductor - Core size
AE			65.4	mm^2	Core Effective Cross Sectional Area
LE			63.5	mm	Core Effective Path Length
AL			113.0	nH/T^2	Ungapped Core Effective Inductance
BW			44.3	mm	Bobbin Physical Winding Width
VE			4150.0	mm^3	

Figure 18. Output Coupled Inductor Parameter.

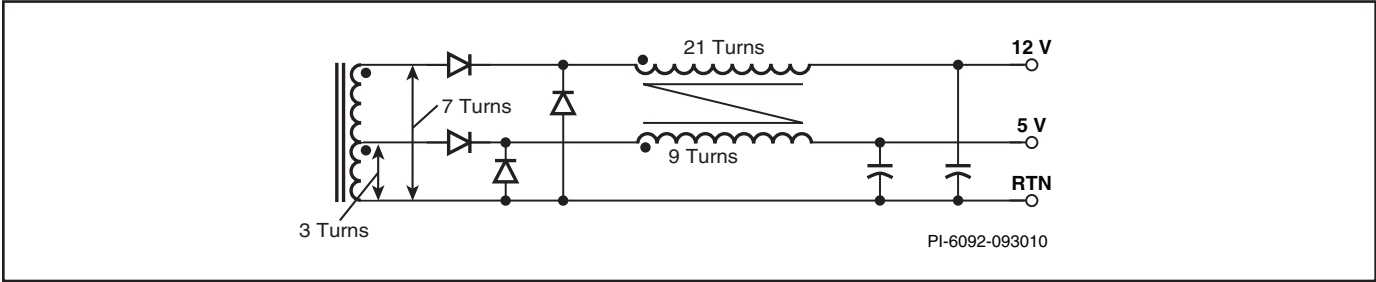


Figure 19. Coupled Inductor and Main Transformer Typical Turns for 5 V and 12 V Outputs.

Powder cores (Sendust and Powdered Iron) Cores					
MUR			90.0		Relative permeability of material
H			84.9	AT/cm	Magnetic field strength
MUR_RATIO			0.31		Percent of permeability as compared to permeability at H = 0 AT/cm
LMAIN_ACTUAL			15.7	uH	Estimated inductance of main output at full load
LMAIN_Obias			49.8	uH	Estimated inductance of main output with 0 DC bias
LOUT2			2.9	uH	Estimated inductance of auxilliary output at full load
BM_IND			2931.7	Gauss	DC component of flux density
BAC_IND			444.6	Gauss	AC component of flux density
Turns					
INDUCTOR_TURNS_MULTIPLIER			3.0		Multiplier factor between main number of turns in transformer and inductor (default value = 3)
NMAIN_INDUCTOR			21.0		Main output inductor number of turns
NOUT2_INDUCTOR			9.0		Output 2 inductor number of turns
NOUT4_INDUCTOR			22.0		Bias output inductor number of turns (for bias or control circuit VDD supply)

Figure 20. Output Coupled Inductor Flux Density.

- Wire parameters section of the spreadsheet are common to both powder core and ferrite designs.
- There is an option to change wire gauge and number of strands. If foil is used, then be sure cross sectional area will result in no less than 200 CMA at maximum load.

Wire Parameters					
Total number of layers			1.67		Total number of layers for chosen toroid
IRMS_MAIN			15.1	A	RMS current through main inductor windings
IRMS_AUX			15.2	A	RMS current through aux winding
AWG_MAIN			17.0	AWG	Main inductor winding wire gauge
OD_MAIN			1.2	mm	Main winding wire gauge outer diameter
FILAR_MAIN			2.0		Number of parallel strands for main output
RDC_MAIN			6.9	mohm	Reisistance of wire for main inductor winding
AC Resistance Ratio (Main)			4.0		Ratio of total resistance (AC + DC) to the DC resistance (using Dowell curves)
CMA_MAIN			273.1	CMA	Cir mils per amp for main inductor winding
J_MAIN			12.8	A/mm^2	Current density in main inductor winding
AWG_AUX			17.0	AWG	Aux winding wire gauge
OD_MAIN			1.2	mm	Auxilliary winding wire gauge outer diameter
FILAR_AUX			2.0		Number of parallel strands for aux output
RDC_AUX			3.0	mohm	Reisistance of wire for aux inductor winding
AC Resistance Ratio (Aux)			1.31		Ratio of total resistance (AC + DC) to the DC resistance (using Dowell curves)
CMA_AUX			273.1	CMA	Cir mils per amp for main inductor winding
J_AUX			13.0	A/mm^2	Current density in auxilliary winding

Figure 21. Output Coupled Inductor RMS Currents.

- This section provides inductor core and winding losses estimates at maximum output power.

Estimated Power Loss					
PCOPPER_MAIN			1.6	W	Copper loss in main inductor winding
PCOPPER_AUX			0.7	W	Copper loss in aux inductor windings
PCORE			0.4	W	Total core loss
PTOTAL			2.6	W	Total losses in output choke

Figure 22. Estimated Coupled Inductor Losses.

- This section gives information concerning maximum voltage and current stress for output rectifiers. Look here to determine the minimum acceptable output diode voltage rating.

SECONDARY OUTPUT PARAMETERS					
ISFWRMS			11.47	A	Max. fwd sec. RMS current (at DVNOM)
ISFWD2RMS			11.47	A	Max. fwd sec. RMS current (at DVNOM)
ISCATCHRMS			12.66	A	Max. catch sec. RMS current (at DVNOM)
ISCATCH2RMS			12.66	A	Max. catch sec. RMS current (at DVNOM)
IDAVMAINF			8.59	A	Maximum average current, Main rectifier (single device rating)
IDAVMAINC			8.89	A	Maximum average current, Main rectifier (single device rating)
IDAVOUT2F			8.59	A	Maximum average current, Main rectifier (single device rating)
IDAVOUT2C			8.89	A	Maximum average current, Main rectifier (single device rating)
IRMSMAIN			1.20	A	Maximum RMS current, Main output capacitor
IRMSOUT2			1.20	A	Maximum RMS current, Out2 output capacitor
		% Derating			
VPIVMAINF		100%	44.8	V	Main Forward Diode peak-inverse voltage (at VDSOP)
VPIVMAINC		100%	33.0	V	Main Catch Diode peak-inverse voltage (at VOVOFF_MAX)
VPIVOUT2F		100%	19.2	V	Output2 Forward Diode peak-inverse voltage (at VDSOP)
VPIVOUT2C		100%	14.2	V	Output2 Catch Diode peak-inverse voltage (at VOVOFF_MAX)
VPIVB		100%	32.0	V	Bias output rectifier peak-inverse voltage (at VDSOP)

Figure 23. Secondary RMS Currents and Output Diode Voltage Ratings.

Standby Section

The standby section of HiperTFS is essentially a TinySwitch device and follows the design procedure for TinySwitch-III with a few exceptions:

1. I_{LIM} selection is implemented by selecting a value of pull-up resistor from the enable pin to the bypass pin (rather than selection of bypass capacitor value as is done for TinySwitch-III).
2. UV lockout is sensed through LINE-SENSE pin rather than through ENABLE pin
3. Reset of OV latch is done through pulling LINE-SENSE pin low or when L pin current falls below 10 μ A.

4. The standby converter in HiperTFS has input line voltage compensation added to overpower threshold which keeps output overpower limit threshold relatively constant with respect to line.

Step 1 – AC Input and Output Voltage and Current

- Enter input voltage range $[VAC_{MIN}]$ and $[VAC_{MAX}]$.
- Enter output voltage $[VO_{SB}]$ and output current $[IO_{SB}]$.
- Enter peak output current $[IO_{(SB)(PK)}]$.
- Enter expected efficiency $[\eta]$.
- Inputs $[Z]$ and $[t_c]$ are usually left to the default values.

HiperTFS STANDBY SECTION (FLYBACK STAGE)					
ENTER APPLICATION VARIABLES					
VACMIN	85			V	Minimum AC Input Voltage
VACMAX	265			V	Maximum AC Input Voltage
fL	50			Hz	AC Mains Frequency
VO_SB	5.00			V	Output Voltage (at continuous power)
IO_SB	2.00			A	Power Supply Output Current (corresponding to peak power)
IO_SB_PK	3.50				
POUT_SB			10	W	Continuous Output Power
POUT_SB_TOTAL			10.32	W	Total Standby power (Includes Bias winding power)
POUT_SB_PK			17.5	W	Peak Standby Output Power
η	0.70				Efficiency Estimate at output terminals. Under 0.7 if no better data available
Z	0.50				Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC	3.00			ms	Bridge Rectifier Conduction Time Estimate

Figure 24. Standby Supply Design Parameters.

Step 2 – Selecting Current Limit, V_{OR} and Bias Winding

- Depending on output power select one of four current limit options LOW, RED, STD, INC. Once current limit has been selected I_{LIM} value are displayed.
- Select V_{OR} . 90 V is default setting which is usually the most efficient design. Selecting a higher value of V_{OR} can cause higher clamp losses. A V_{OR} lower than 90 V will increase the peak reverse voltage across output rectifier.
- Note that the standby converter is switching at twice the frequency of the main converter. (i.e. $f_{SB} = 132$ kHz).
- The standby transformer bias winding [V_B] is used to operate a primary side auxiliary supply. This feeds a +12 V regulator that supplies a number of primary side circuits including typically providing operating current to the PFS boost stage. The default value of +16 V gives adequate headroom for +12 V bias regulator.
- UVLO section shows expected turn on threshold for standby [$V_{(UV)(ACTUAL)}$] for the given line sense resistor value [R_{LS}].

ENTER HiperTFS STANDBY VARIABLES					
Select Current Limit	INC		Increased Current Limit		Enter "LOW" for low current limit, "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIM_MIN			0.698	A	Minimum Current Limit
ILIM_TYP			0.750	A	Typical Current Limit
ILIM_MAX			0.803	A	Maximum Current Limit
R(EN)			137.0	k-ohms	Enable pin resistor
fSmin			124000	Hz	Minimum Device Switching Frequency
I ² fmin			66.83	A ² kHz	I ² f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR			90	V	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10	V	HiperTFS Standby On State Drain to Source Voltage
VD_SB			0.5	V	Output Winding Diode Forward Voltage Drop
KP			0.65		Ripple to Peak Current Ratio (KP < 6)
KP_TRANSIENT			0.33		Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25

Figure 25. HiperTFS Standby Current Limit and Reflected Voltage.

ENTER BIAS WINDING VARIABLES					
VB			16.00	V	Bias Winding Voltage
IB			20.00	mA	Bias winding Load current
PB			0.32	W	Bias winding power
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
NB			12.15		Bias Winding Number of Turns
VZOV			22.00	V	Over Voltage Protection zener diode voltage.
UVLO VARIABLES					
RLS			4.03	M-Ohms	Line sense resistor (from Main converter section)
V_UV_ACTUAL			103	V	Typical DC start-up voltage

Figure 26. Standby Bias Winding Voltage and Input Undervoltage.

Step 3 – Standby Transformer Design

- Select desired core [Core Type] from drop down menu. The default core is EE25 (EI25) which is adequate for up to 20 W. EE19, EEL19, EE22 are also commonly used for lower power.
- Select secondary turns [N_s]. Four turns trifilar wound gives best efficiency for +5 V output.
- If desired core is not in drop down list then enter core and bobbin parameters directly into [A_E] [L_E] [A_L] [BW].

Transformer Design Parameters

Key parameters to check are:

- [L_{SB}] Primary inductance is a key parameter in determining output power.
- [B_M] Maximum flux density should be below 3000 Gauss.
- [CMA] Current density of windings at max continuous output power should be above 200 CMA to avoid excessive thermal rise of transformer.

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EE25	EE25	EE25		Enter Transformer Core
Core		EE25		P/N:	PC40EE25-Z
Bobbin		EE25_BOBBIN		P/N:	EE25_BOBBIN
AE			0.404	cm ²	Core Effective Cross Sectional Area
LE			7.34	cm	Core Effective Path Length
AL			1420	nH/T ²	Ungapped Core Effective Inductance
BW			10.2	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			2		Number of Primary Layers
NS_SB			4		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN_SB			114.52	V	Minimum DC Input Voltage
VMAX_SB			374.77	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX_SB			0.46		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.24	A	Average Primary Current
IP_SB			0.70	A	Minimum Peak Primary Current
IR_SB			0.45	A	Primary Ripple Current
IRMS_SB			0.38	A	Primary RMS Current

Figure 27. Standby Transformer Selection.

TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP_SB			799.10	uH	Typical Primary Inductance. +/- 10% to ensure a minimum primary inductance of 726 uH
LP_TOLERANCE			10	%	Primary inductance tolerance
NP_SB			65		Primary Winding Number of Turns
ALG			187	nH/T ²	Gapped Core Effective Inductance
BM			2425	Gauss	Maximum Operating Flux Density. BM<3000 is recommended
BAC			785	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			2053		Relative Permeability of Ungapped Core
LG			0.24	mm	Gap Length (Lg > 0.1 mm)
BWE			20.4	mm	Effective Bobbin Width
OD			0.31	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.26	mm	Bare conductor diameter
AWG			30	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			102	Cmils	Bare conductor effective area in circular mils
CMA			265	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			11.41	A	Peak Secondary Current
ISRMS			6.76	A	Secondary RMS Current
IRIPPLE			6.45	A	Output Capacitor RMS Ripple Current
CMS			1351	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			18	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			584	V	Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance)
PIVS			28	V	Output Rectifier Maximum Peak Inverse Voltage

Figure 28. Standby Transformer Parameter.

	Output Power Range (W)	Core Size	Core Material	Source
Main Transformer	150-300	EER28	Ferrite	TDK, Mag Inc.
	150-300	EDT34	Ferrite	TDK, Mag Inc.
	300-450	EER35	Ferrite	TDK, Mag Inc.
Standby Transformer	4-8	EE16	Ferrite	TDK, Mag Inc.
	8-15	EE19	Ferrite	TDK, Mag Inc.
	12-20	EI22	Ferrite	TDK, Mag Inc.
Coupled Output Inductor	150-300	27.7 (OD)	Sendust, Koolmu	Mag Inc. CSC
	300-450	33.8 (OD)	Sendust, Koolmu	Mag Inc. CSC
	150-300	33.0 (OD) (T130-52)	Powdered Iron	Micrometals
	300-450	38.4 (OD) (T150-52)	Powdered Iron	

Table 2. Common Cores Sizes and Sources.

External Circuit Design and Circuit Options for HiperTFS

Remote-On and Standby Bias

When the standby converter turns on and achieves regulation it provides an auxiliary bias $[V_{BIAS}]$ for primary side control circuits. The primary bias is the source for the remote-on output (V_{ON}) which is a +12 V regulated output. The external circuit configuration is shown below in Figure 29.

Design and Operation

The initial application of AC will provide a DC input to both main and standby converters. The HiperTFS high-voltage internal current source tab will then charge the BYPASS (BP) pin to 5.8 V and the standby converter will start to switch. When input reaches $[V_{UV}]$ the standby supply will power up while the main converter remains off. When the standby output reaches regulation there will also be a bias $[V_{BIAS}]$ available from the

standby converter. $[V_{AUX}]$ will then provide bias to the BYPASS pin through R2 which will bring the BP voltage up to 6 V and turn off the internal high voltage current source which allows the standby converter to operate more efficiently. When the standby converter is on and in regulation, a remote-on (power-on) command can be made from the secondary side by turning the opto LED (REM) on which turns on Q1. The emitter of Q1 then provides 12.6 V which is sufficient to cause 5 mA to flow into the BYPASS pin. This BYPASS pin current is sensed internally by HiperTFS and triggers the main converter to start its turn-on sequence. Details of turn on sequence will be described in high-side driver section.

Note: V_{ON} voltage can be adjusted by modifying V_{ZENER} (typically 13 V).

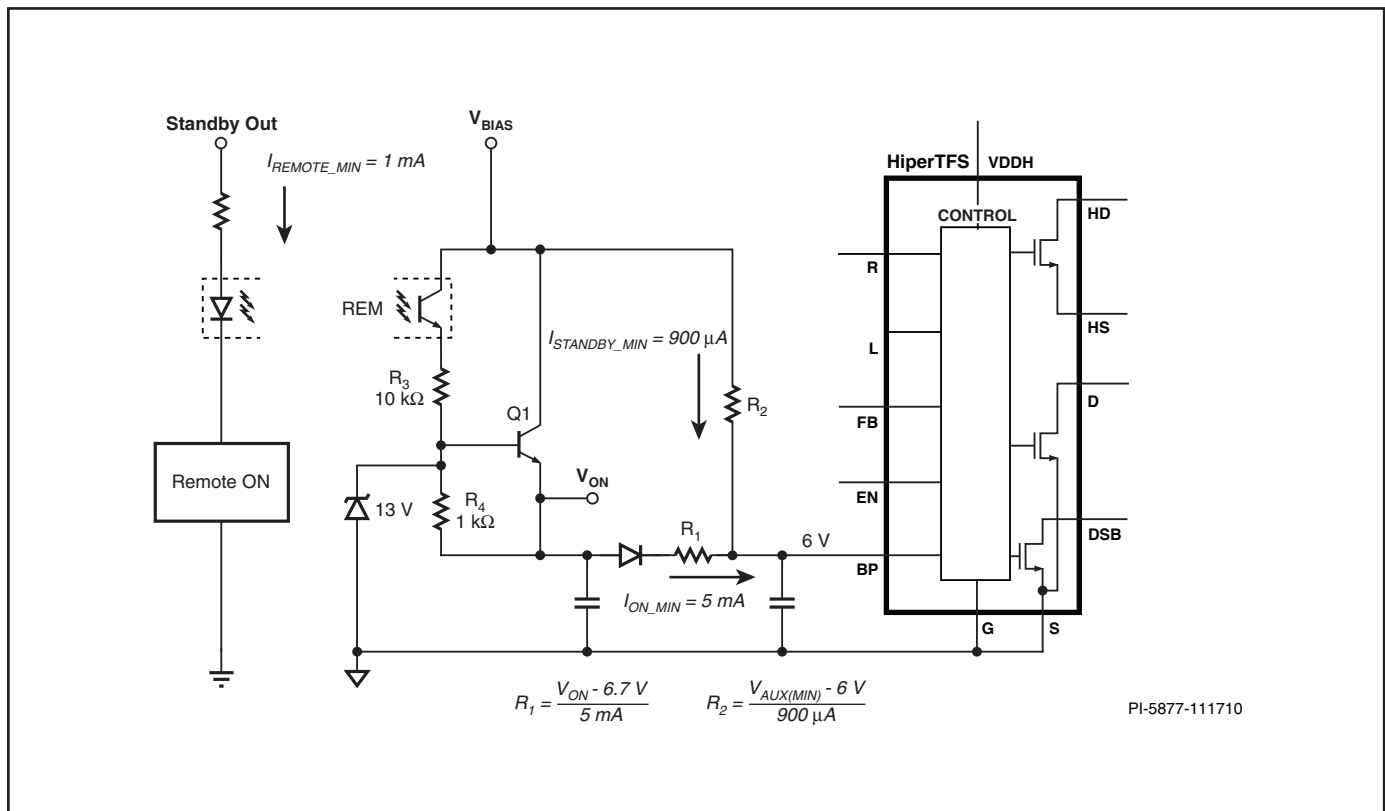


Figure 29. Remote-ON and Standby Bias.

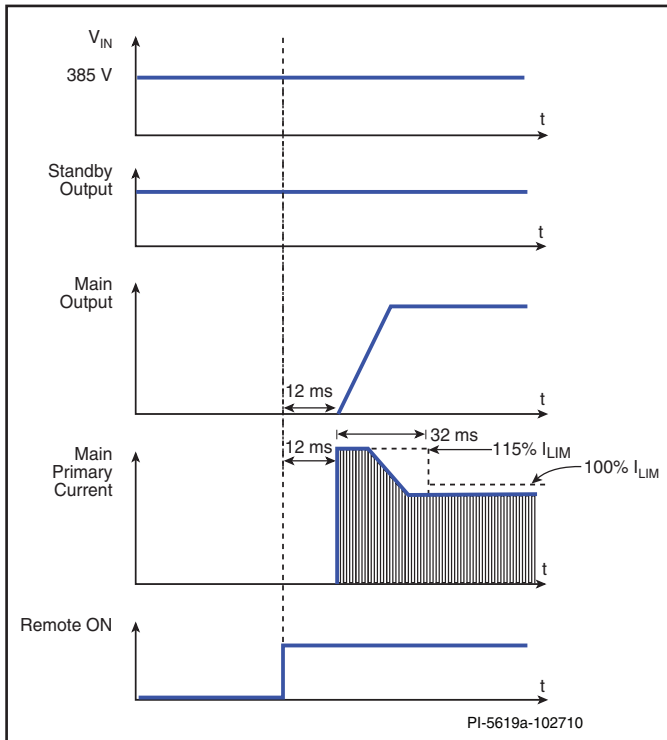


Figure 30. Supply Start-Up Sequence by Remote-ON

High-Side Drive Operation and Bias

As described in the previous section, when there is an initial Remote-on command, 12 V power is applied to the HiperTFS BYPASS pin, allowing the main converter to turn on. It does so in a series of steps. Referring to Figure 31, first the MAIN DRAIN pin of the bottom MOSFET is pulled low for 12 ms. This allows sufficient time for C1 to be bootstrap charged from the standby bias output through CR1. The voltage across C1 feeds the high-side driver bias voltage into C2 through R1 which is shunt regulated to +12 V by high-side operating voltage (VDDH) pin internal shunt regulator. The main converter will then start high-side and low-side switching 12 ms after receiving the remote-on command. Output voltages will rise at a rate determined by the built in duty cycle soft-start until the secondary main feedback regulator controls the duty cycle via the FEEDBACK pin of the HiperTFS. Once switching begins the external bias source for main high-side operating voltage pin (VDDH) is derived from a forward phased winding of the main transformer.

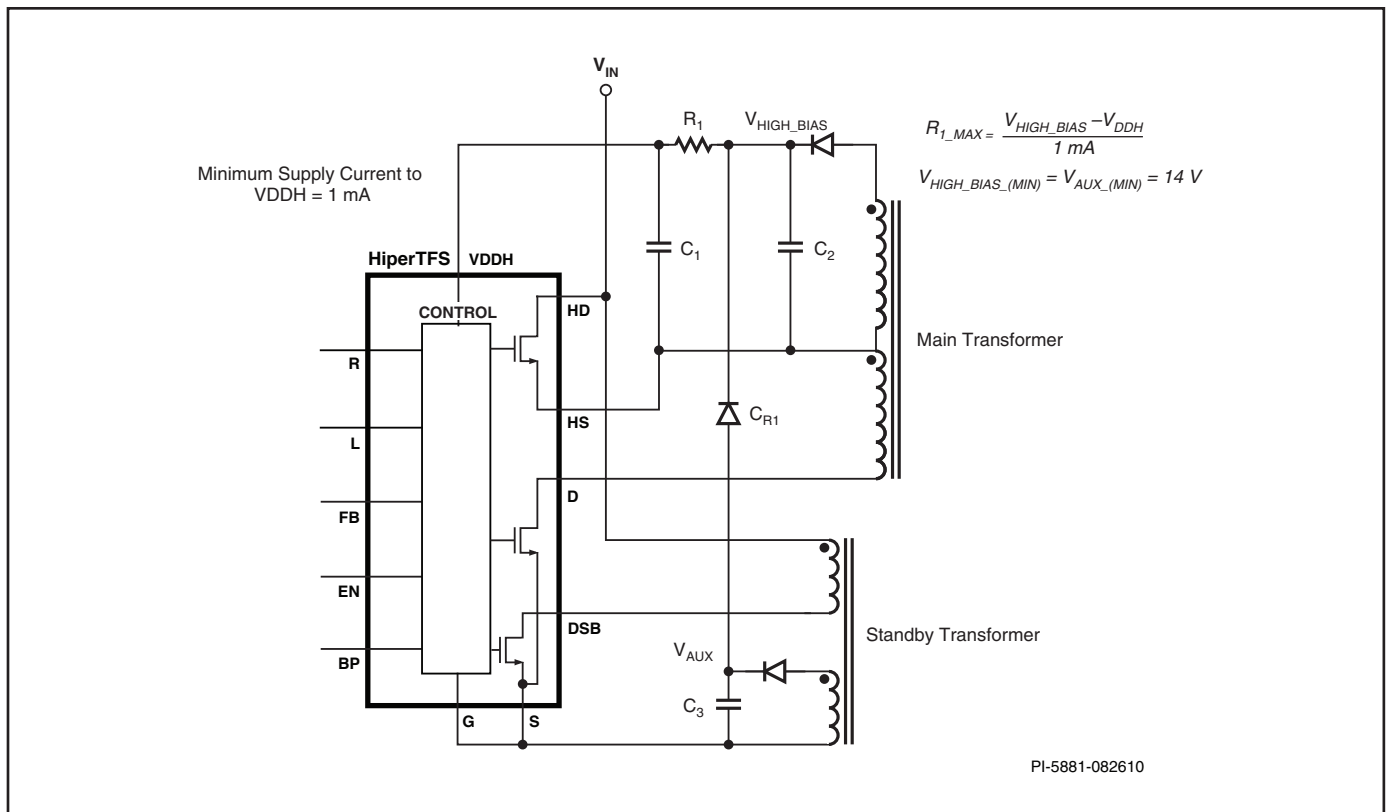


Figure 31. High-Side Bias.

Primary Clamp Circuit

The diagram below shows the standard clamp-to-rail configuration. The clamp energy of both the primary main winding magnetizing and leakage inductance and standby primary winding leakage inductance are routed through CR2 and CR3 to Zener clamp VZ1 and C1.

R1, R2, and R3 are damping resistors. Diodes CR2 and CR3 are standard slow recovery diodes such as 1N4007G which allow recycling of the leakage and magnetizing energy from C1.

Diode CR1 is an ultra fast recovery diode such as UF4006. The clamp circuit is quite efficient and commonly total dissipation in the clamp for a 300 W design is less than 0.3 W. The main converter operation uses both the VZ1 (150 V) and the input bus voltage (385 V) to reset the transformer so only a portion of the reset voltage is actually across VZ1 for reset of the main primary.

Zener diode VZ1 when referenced to the DC rail gives the benefit of the widest possible duty factor for the main transformer and also provides a shared clamp circuit above the rail for the standby flyback converter.

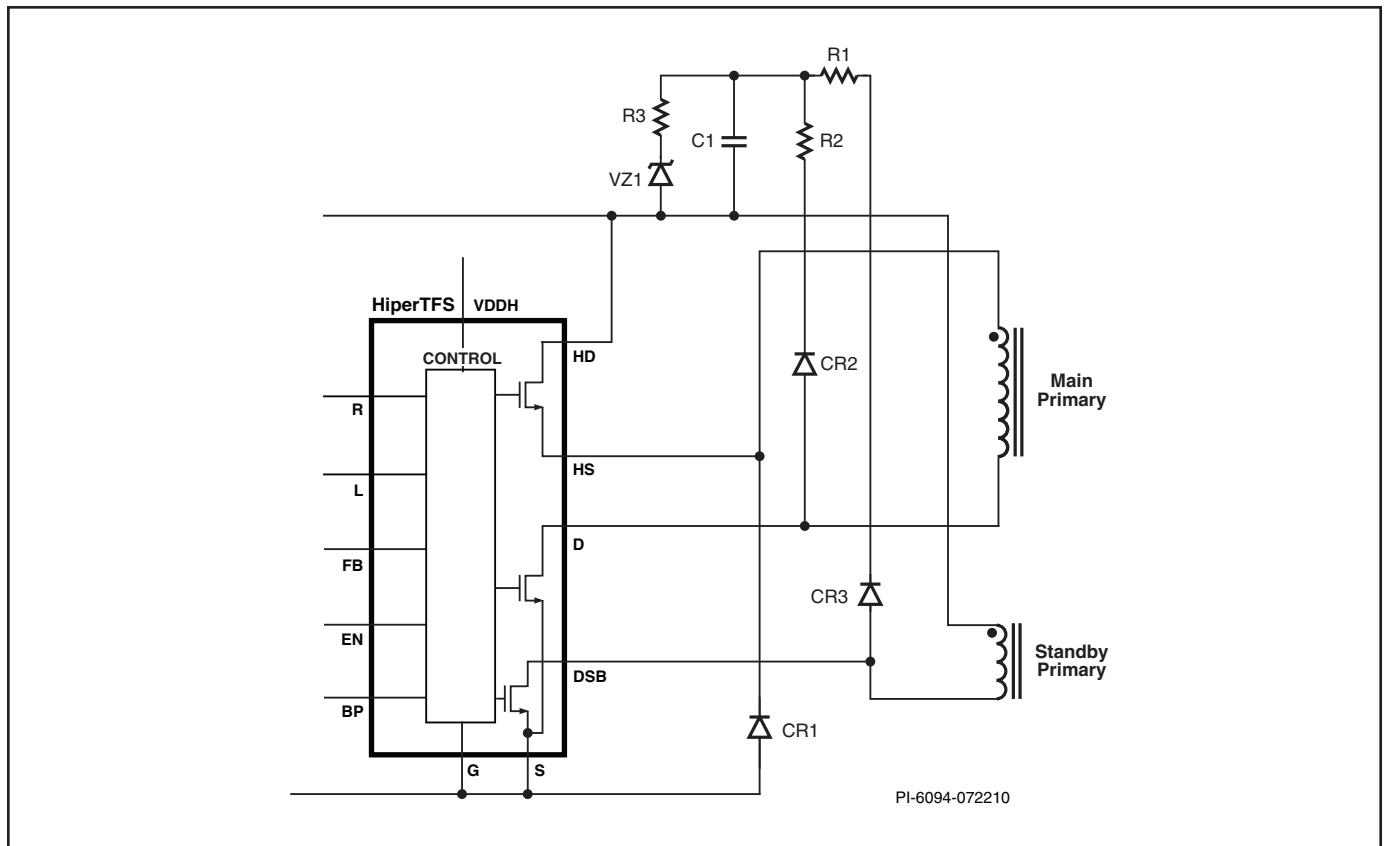


Figure 32. Primary Clamp Circuits (using Zener Clamp-to-Rail Network).

Figure 33 shows the switching voltage and current relationship between the upper switching MOSFET (V_{HS}) and lower switching MOSFET of the two-switch converter. Note that the peak drain to source voltage (V_{DS}) of high-side MOSFET is essentially equal to the input bus (385 V) while the peak drain to source voltage across the low-side MOSFET is significantly higher. The (V_{DS}) of the low-side MOSFET is equal to the sum of the input bus voltage (V_{IN}), Zener clamp VZ1 and forward recovery spike of CR2. The higher voltage across the bottom MOSFET effectively increases the reset voltage across the primary which allows for a wider operating duty cycle as compared to a conventional two-switch forward where the bottom MOSFET drain is clamped to the input bus. This enables maximum operating duty cycles in excess of 50% with associated reduction in primary and secondary RMS current and reduced voltage stress on the output catch diodes.

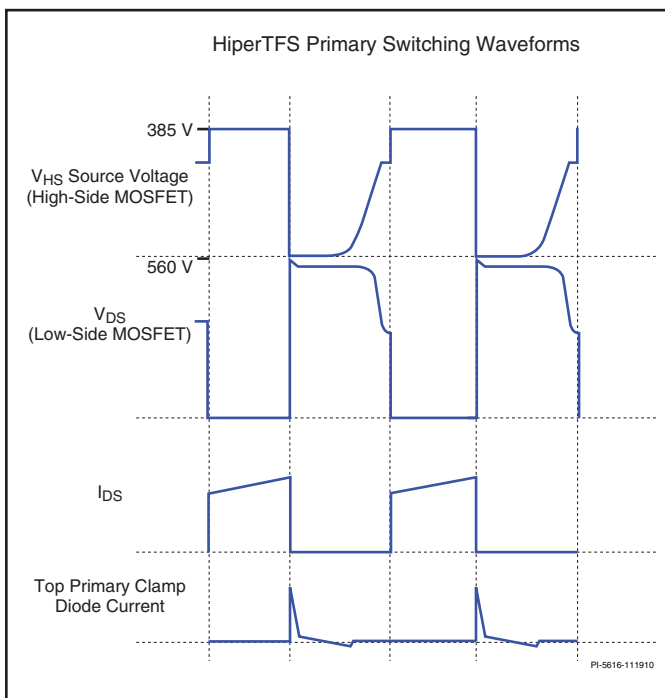


Figure 33. HiperTFS Primary Switching Waveform.

Standby and Main Feedback

The FEEDBACK pin (FB) is the voltage mode PWM control input for the main two-switch forward converter. The duty cycle of the main converter primary on-time is controlled by the feedback sink current of Opto1. Figure 35 shows the transfer relationship between the external feedback sink current and the resultant duty cycle.

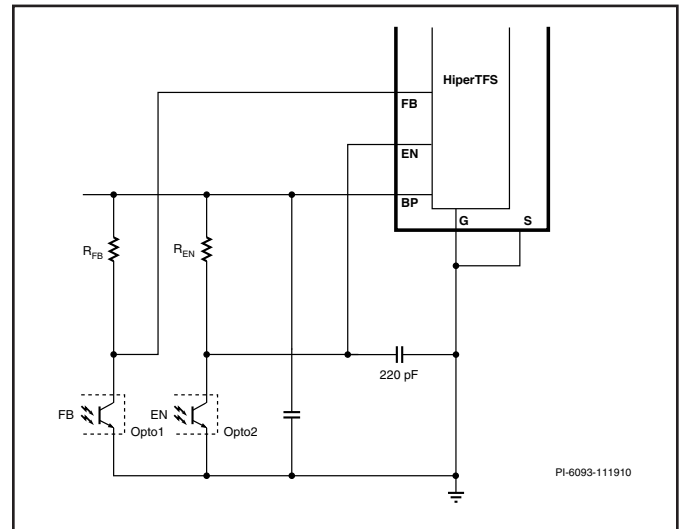


Figure 34. Main Converter FEEDBACK Pin Duty Cycle Control.

The standby converter uses the ENABLE (EN) pin for feedback via ON/OFF current mode control in the same manner as TinySwitch-III. Figure 36 shows the relationship between ENABLE pin sink current and output response.

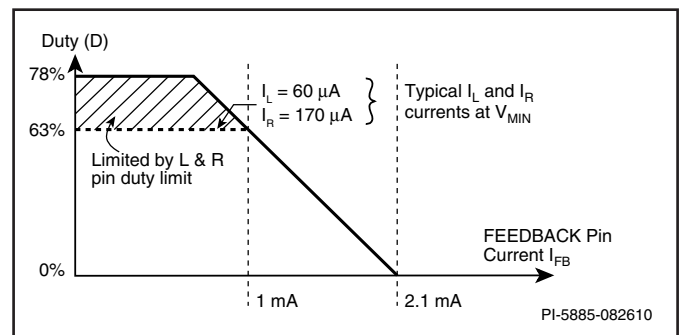


Figure 35. Main Converter FEEDBACK Pin Duty Cycle Control.

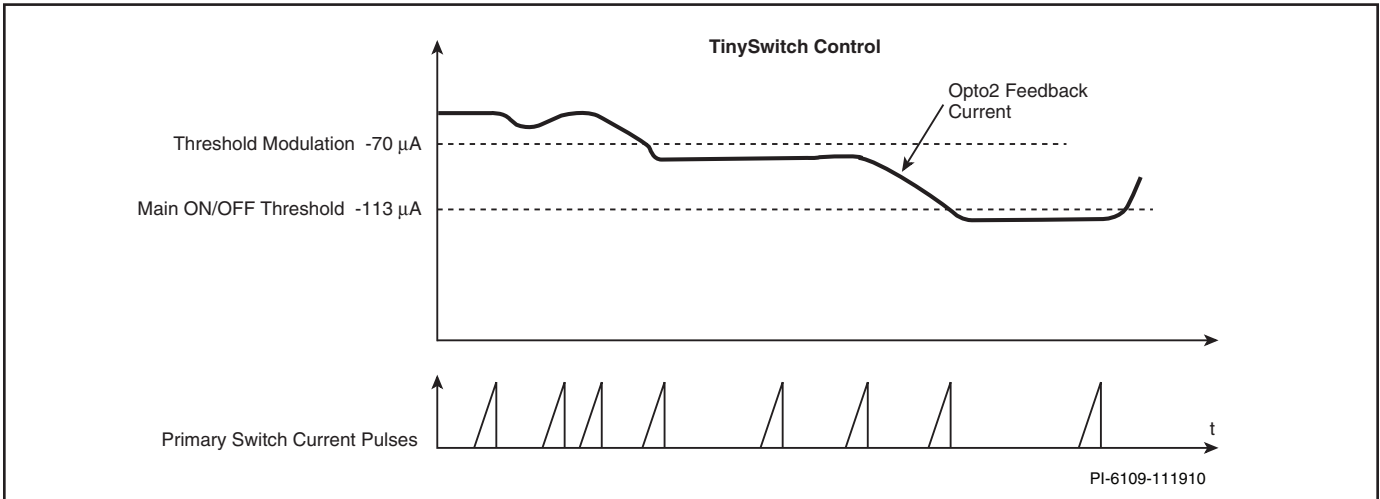


Figure 36. TinySwitch Control Illustrating ENABLE Pin Threshold Modulation.

Standby Output OVP

The BYPASS pin has the added function of latching off both standby and main converters when more than 15 mA is sourced into the BYPASS pin. This offers a very convenient way to implement standby output OVP latching protection. The diagram below shows a simple output OVP circuit using the BYPASS pin feature. When the standby output voltage exceeds

the sum of the Zener voltage of V1 and the diode drop of the LED input to IC1, current will flow into the BYPASS pin from the output transistor of IC1 into the BYPASS pin causing both converters to latch off into shutdown state. The latch can be reset by reducing the LINE-SENSE pin current below the ULVO threshold (10 μA).

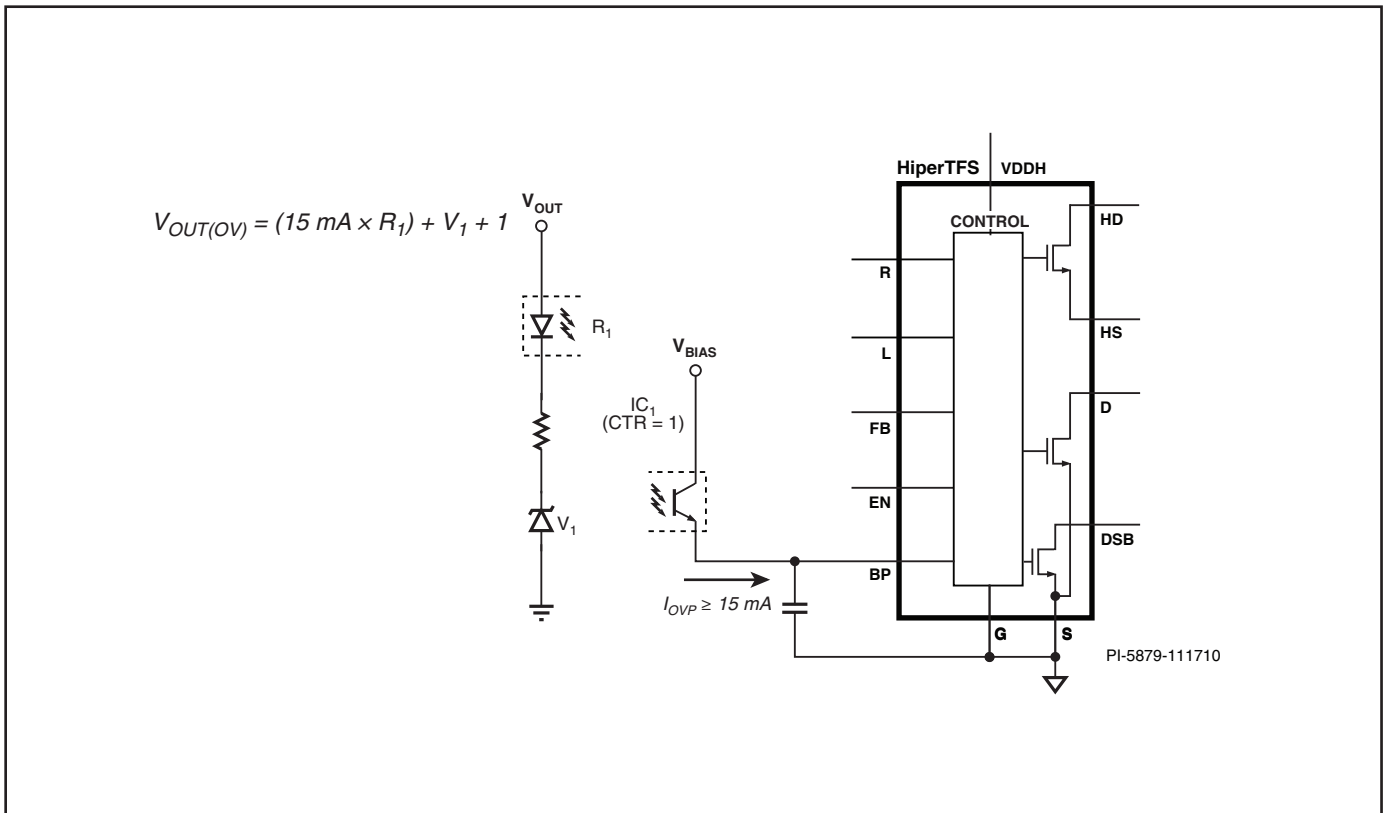


Figure 37. Latching Standby Output OVP (see Figure 42 for Quick AC Latch Reset).

Non-Latching Standby Output OVP

The diagram below is a non-latching option for standby output OVP. Instead of using the BYPASS pin latch off function, this circuit instead uses the LINE-SENSE pin OV threshold, which is non-latching

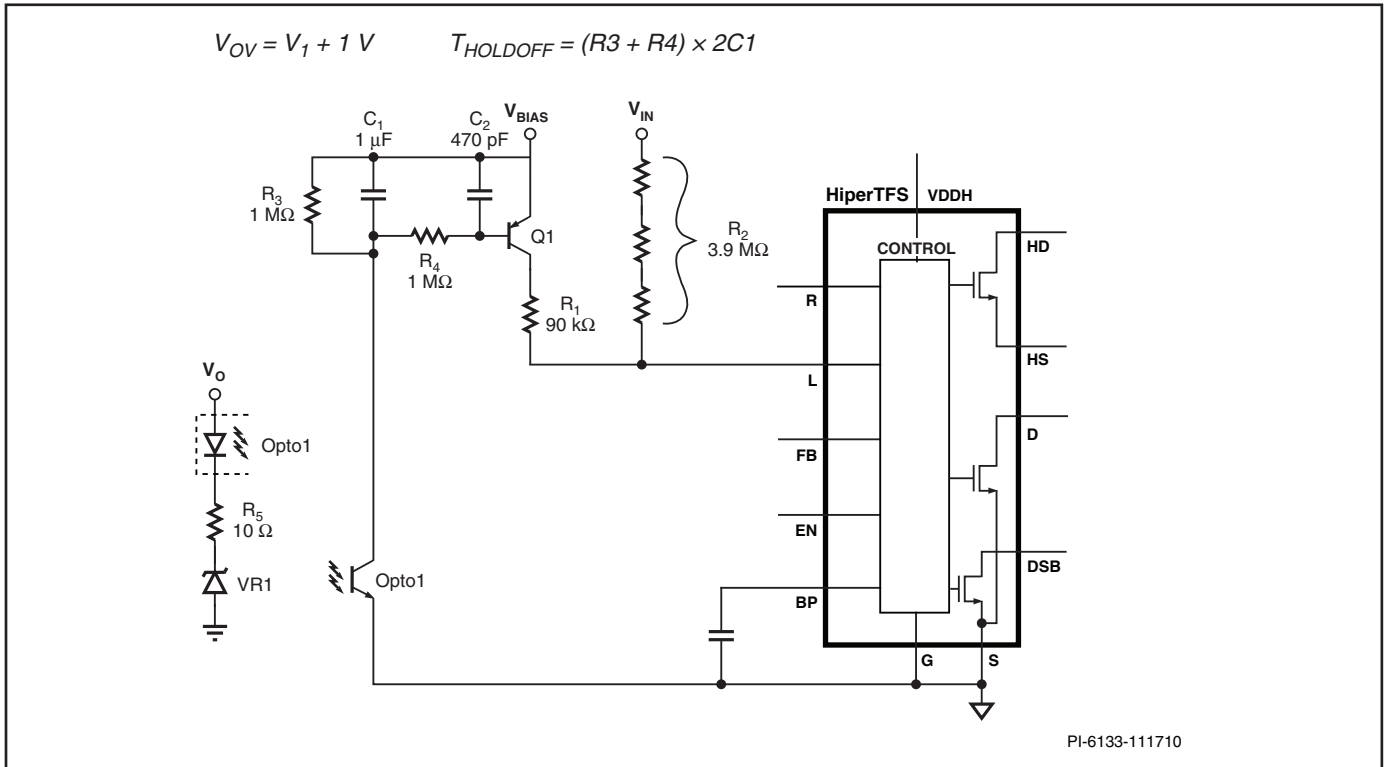


Figure 38. Standby OVP With 1-Second Shutdown of Main and Standby Followed by Retry (Auto-Restart)

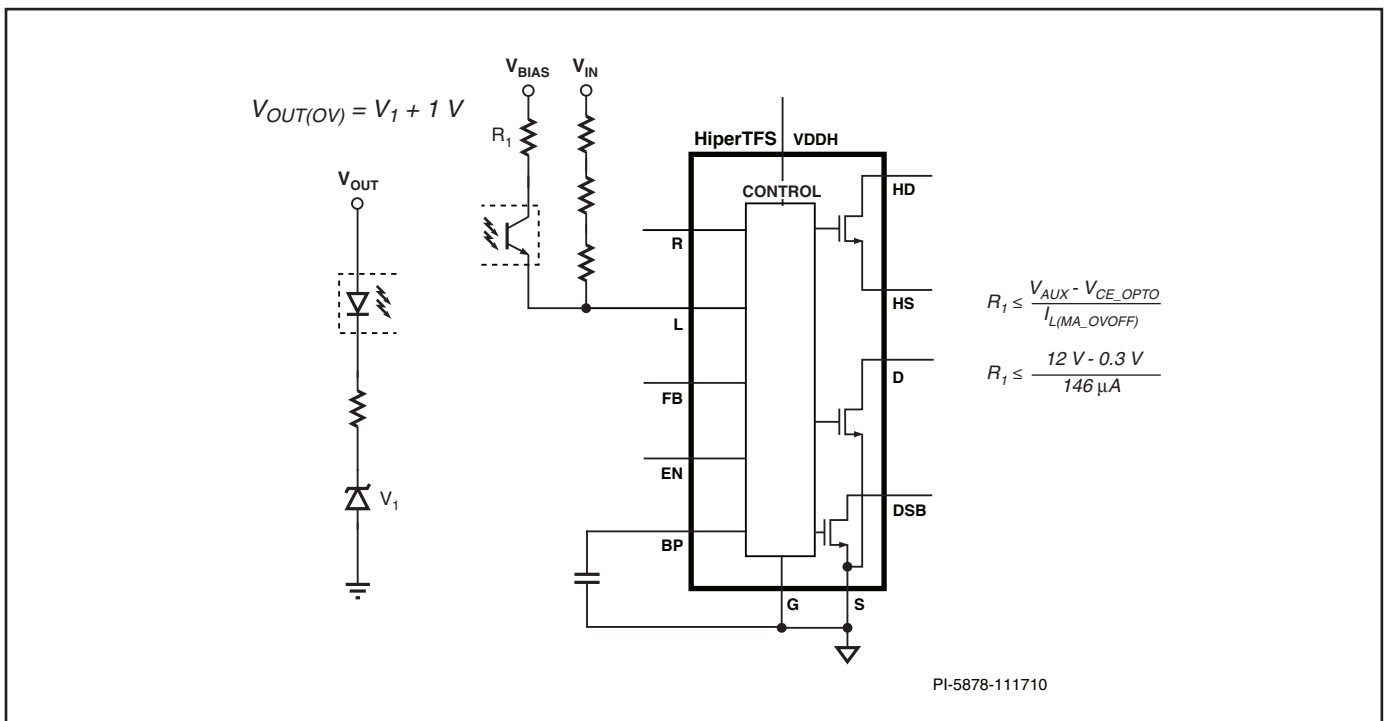


Figure 39. Non-Latching Standby Output OVP.

Independently Programmed (Non-Latching) Input OVP

The input overvoltage threshold is by default a fixed ratio with respect to the input overvoltage thresholds. However it is possible to independently program the input overvoltage threshold. This circuit senses the input voltage through the resistor divider formed by R2 (composite) and R1. This input sense voltage is compared to the Zener voltage VR1.

When the sense voltage reaches the OV threshold Q2 will conduct and the LINE-SENSE pin will be pulled high causing both the main and standby converters to shut down. Once the input (V_{IN}) OV condition is removed the supply will initiate at start-up sequence provided the remote-on command is present.

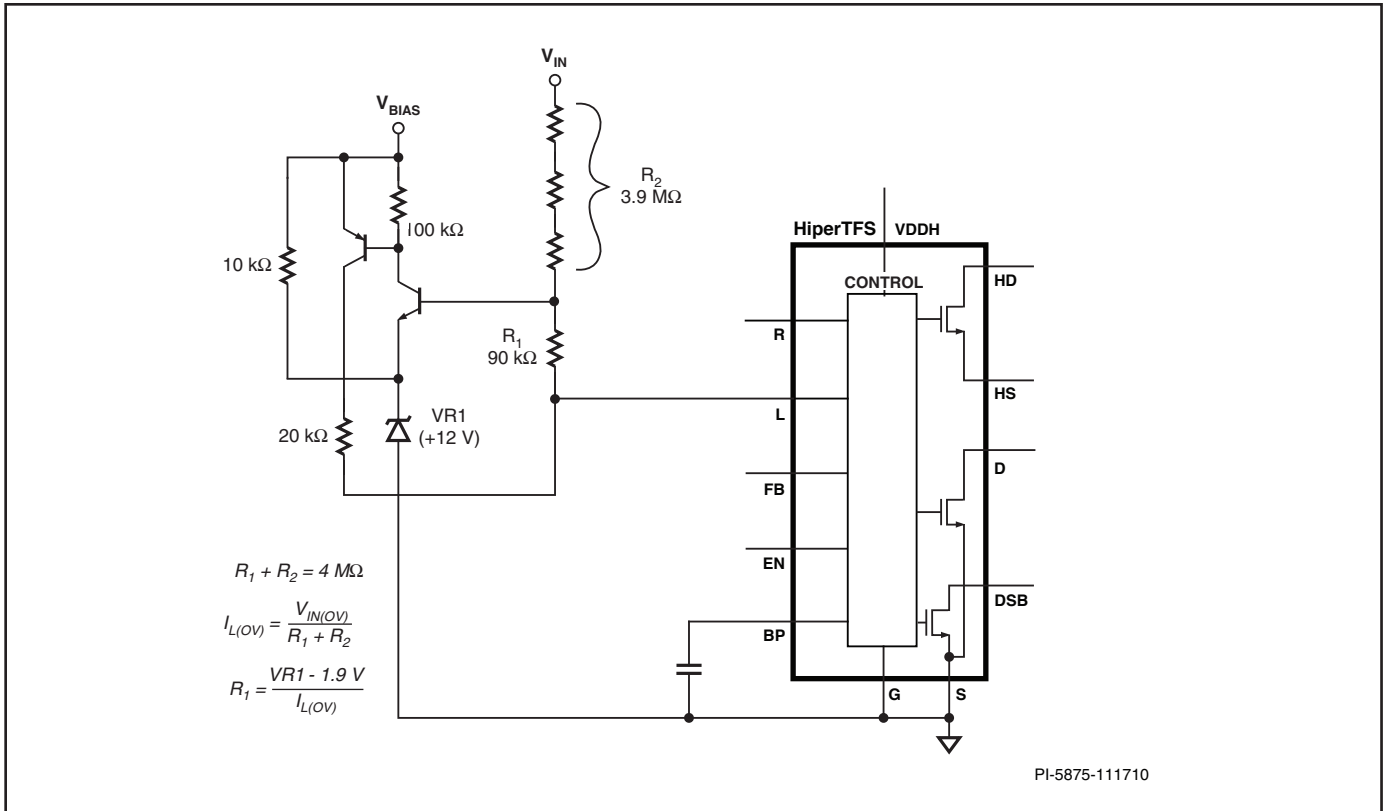


Figure 40. Non-Latching Input OVP.

Independently Programmed (Latching) Input OVP

The circuit below is the same as the non-latching input OVP circuit previously described with the exception that the output of Q1 drives the BYPASS pin, which causes the OV condition to

latch the both main and standby converters off. The latch is reset when the LINE-SENSE pin current goes below the UVLO (standby) threshold of 10 μ A.

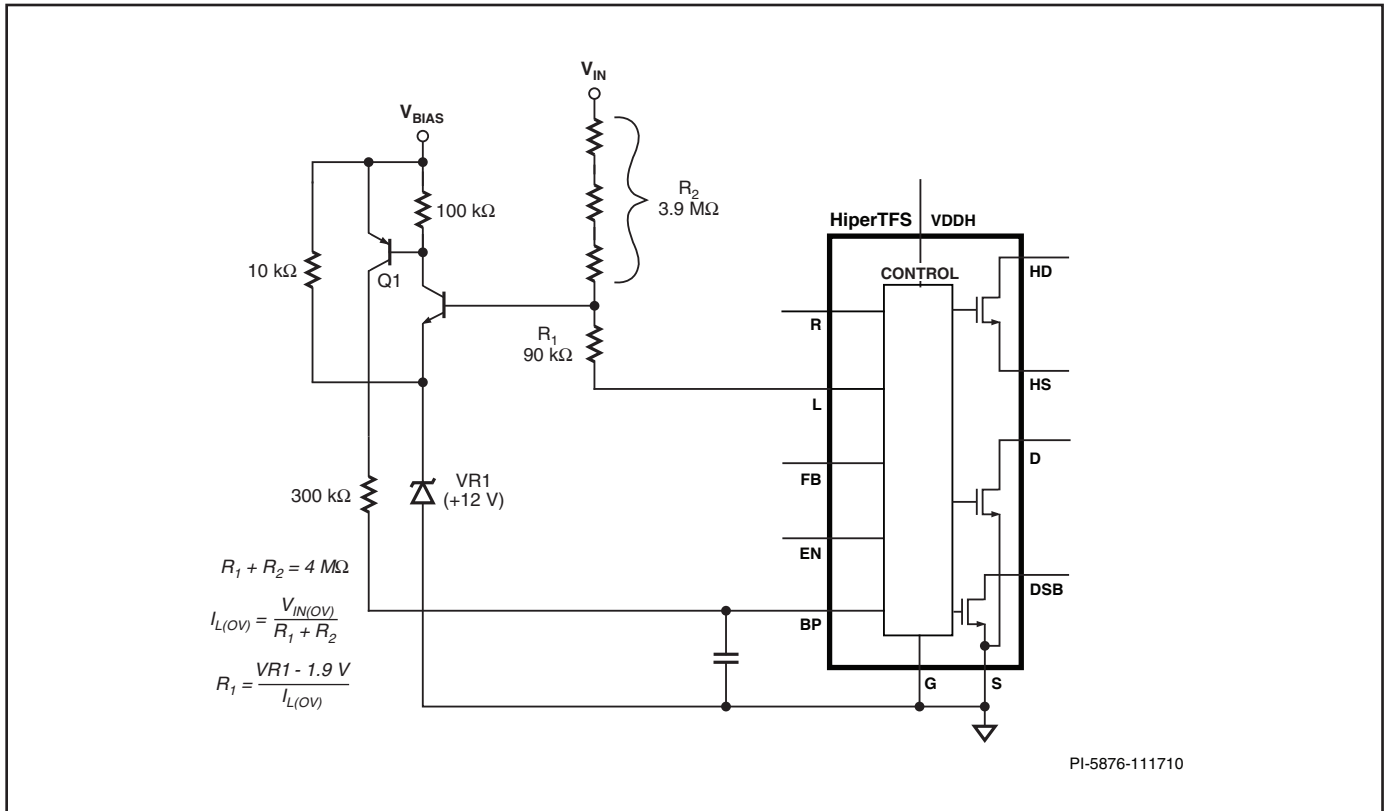


Figure 41. Latching Input OVP.

Fast AC (Off) Reset of OVP Latch from BYPASS Pin

The circuit below allows quick reset of the BYPASS pin latch which shuts off both main and standby converters. When AC is present, this turns on Q1 and thus holds Q2 in the off state. When AC input is not present, the voltage on C1 starts to decay. After a delay of 50 ms to 200 ms Q1 will turn off and

allow Q2 to turn on, biased through R3. This pulls the LINE-SENSE pin to ground and resets the latch. Application of AC after reset allows the converter to initiate normal start-up sequence.

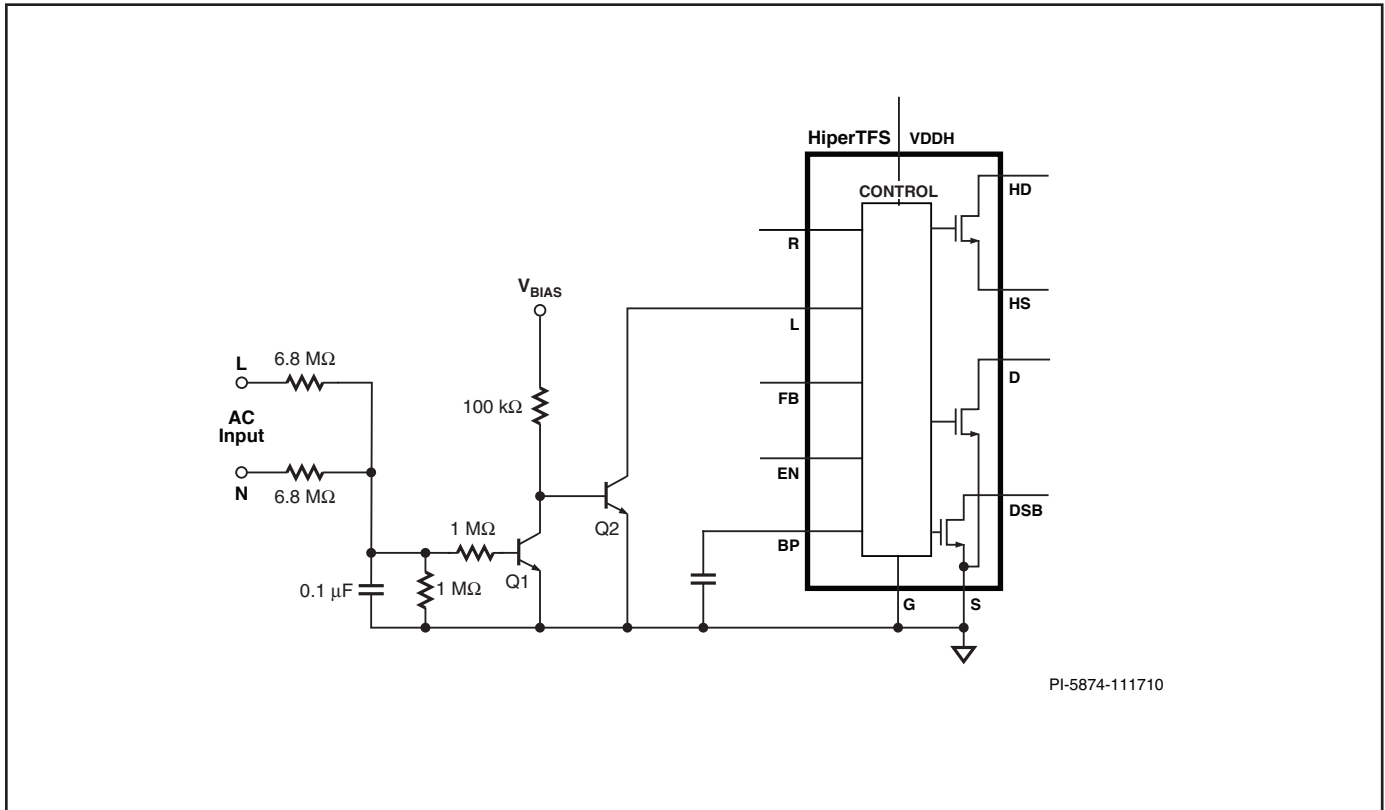


Figure 42. Quick AC Reset of BP Latch (see Figure 37 BYPASS Pin Latch).

Design Example Using HiperTFS (RDK-249)

The schematic below shows a 300 W DC input power supply with a single +12 V output and a 17 W +5 V standby using TFS762HG. The main output is guaranteed to maintain regulation from 300 VDC to the nominal of 385 V and has a minimum efficiency of 90% at full load (25 A). The standby converter has a guaranteed minimum input regulation of 100 VDC at full load, and a minimum efficiency of 75% at full load.

Some of the previously described external interface/support circuits are used, including:

- Remote-ON/OFF
- Primary clamp-to-rail
- High-side driver bias
- Latching secondary and standby output OV protection
- LINE-SENSE pin and RESET pin sensing

This power supply example uses main transformer (EER35), standby transformer (EI25) and output inductor (TH130-52) that were designed using the Power Integrations HiperTFS design spreadsheet.

Both the main +12 V output and standby +5 V output use separate TL431 error amplifiers for sensing and providing a feedback coupled to the HiperTFS via optocouplers. Standby and main output OV protection sensing is accomplished with VR3 and VR4 which drive optocoupler U2A when there is a fault. For more detail refer to RDK-249 reference design report.

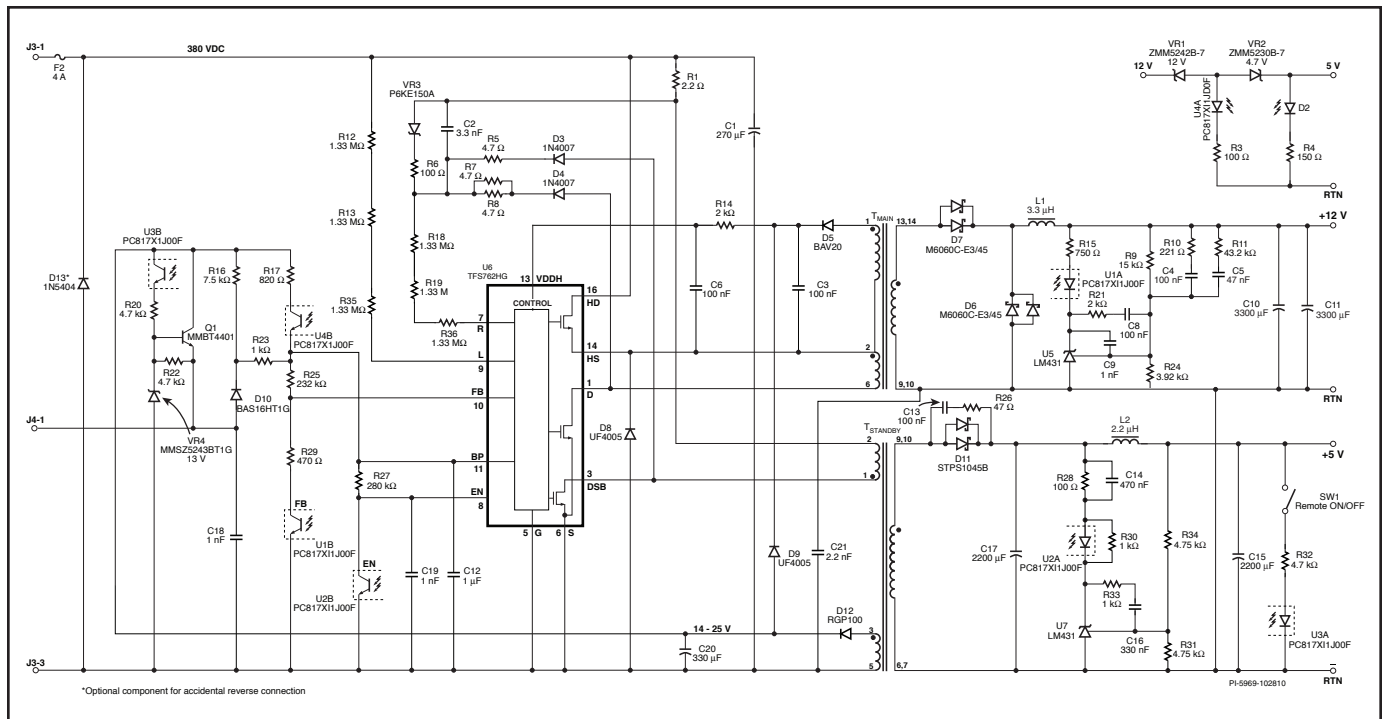


Figure 43. Schematic of 300 W Power Supply.

RDk-249 PCB Layout Guidelines

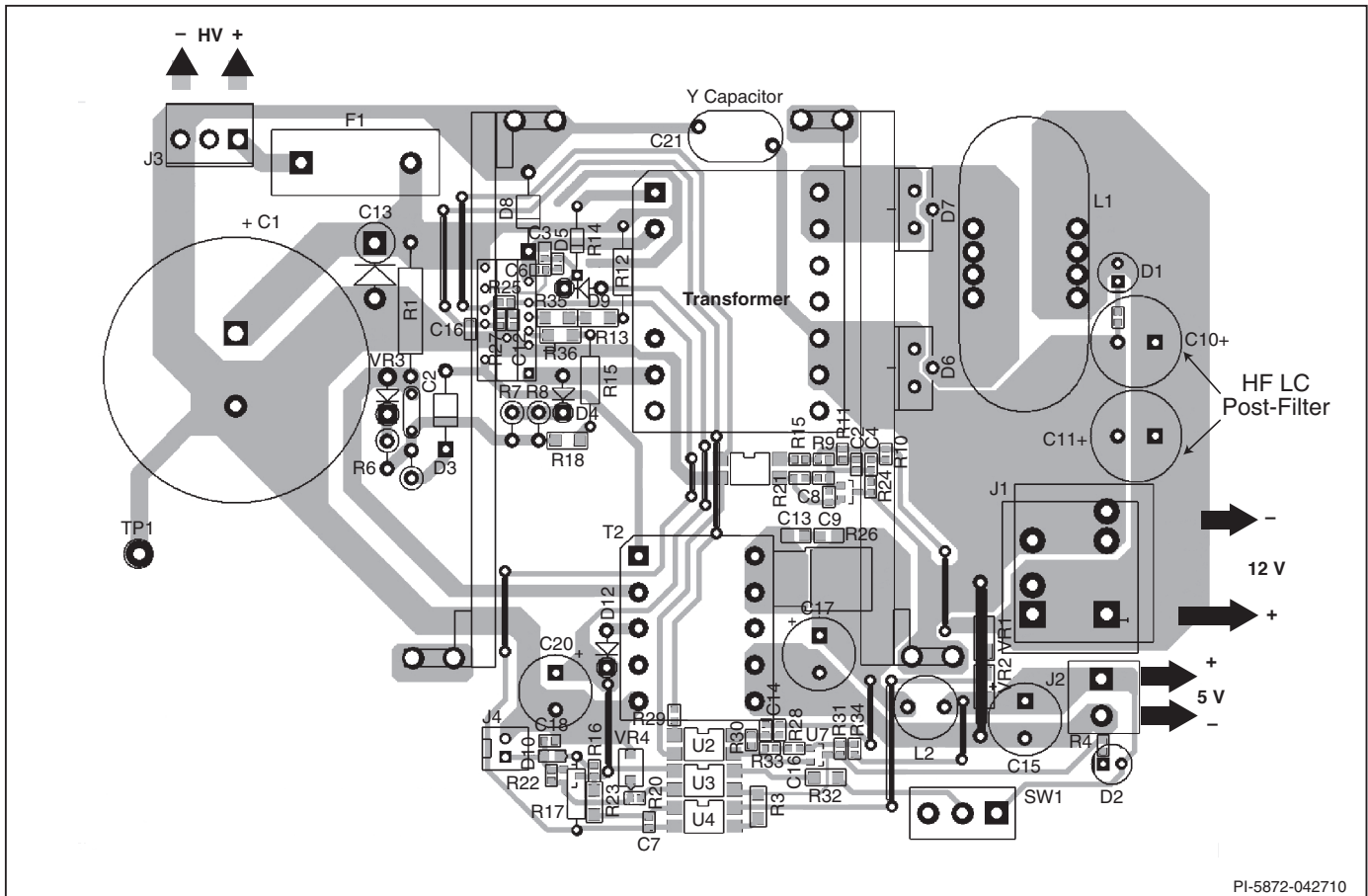
As is true with any switch mode power supply design it is critical to have a good layout. Since HiperTFS has both sensitive small signal control functions and high power (high-voltage and current) switching pins it is even more important that good layout practices be maintained. The RDk-249 is a good example of how to layout a main and standby converter design using HiperTFS. The following guidelines assure stable and clean operation of both the main and standby supplies. Since the RESET, LINE-SENSE, FEEDBACK and ENABLE pins are in close proximity to high power switching nodes, care should be taken to route high-voltage and currents traces away from these pins as much as possible to prevent interference.

The layout below shows several layout techniques that were used to keep small signal sensitive pin functions isolated from high-voltage and high current noise. High current related noise can be avoided by routing the feedback optocoupler emitters of U1B and U2B to a single point ground at the GROUND pin of HiperTFS. The return of the auxiliary capacitor C20 is routed to the return of the input bulk capacitor. The GROUND pin is locally tied to the SOURCE pin and the high current path is routed to the bulk capacitor return. These measures avoid having any high current flowing in the feedback return traces. The LINE-SENSE pin and RESET pin sense current through high impedance resistors that can pick up switching noise

unless attention is taken with the layout of these sense resistors. The layout example below is an example of how to keep the L and R sense function clean. The RESET pin sense resistor is broken up into 3 discrete resistors to distribute voltage stress. The first resistor is an SMD type and is located at the sense point from the high-voltage clamp. The second resistor is an axial leaded part used as a jumper over high-voltage switching nodes. The third resistor is SMD type and is located near the RESET pin connection for minimal noise pickup. The LINE-SENSE pin sense resistor chain uses an axial resistor as the first resistor, used as a jumper over a noisy region. The other two LINE-SENSE pin resistors R12 and R13 are very close to the LINE-SENSE pin to minimize noise pickup.

A second technique to keep the RESET pin and LINE-SENSE pin quiet is to place low impedance quiet traces adjacent to the pin. These traces act as a virtual Farady shield. In this case the final resistors R13, R35 and R36 are sandwiched between the bypass pin trace and the return trace of the HiperTFS, which are both quiet traces with low AC noise.

Another important technique is to place high-voltage switching related circuits away from the sensitive circuit regions. In particular, the high-voltage primary and standby clamp and associated circuits should be located away from sensitive pin



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Figure 44. Layout of High-Efficiency +12 V, 25 A Main Output and +5 V, 2.5 A Standby Power Supply.

circuits. The boot-strap diode D9 is close to the high-side operating voltage pin to minimize the length of the cathode trace, which has high-voltage switching. Finally, the main transformer is close to the HiperTFS device to keep high voltage switching traces short.

Retrofit 300 W PC Main and PC Standby Using HiperPFS and HiperTFS Meeting 80 PLUS Bronze Efficiency

The design in Figure 46 is an example of a complete 300 W PC power supply with power factor corrected front end using

HiperPFS providing 385 VDC to a DC-DC converter stage using HiperTFS. The design was built by removing the primary side circuitry of an existing ATX power supply and grafting on a new primary section incorporating the HiperTFS and HiperPFC converter circuits. The layout for the primary side is included below. The secondary schematic (Figure 47) shows the power and feedback circuits of original design. The original enclosure, output diodes, fan and heat sinks were used. The output choke was designed using HiperTFS spreadsheet. The table below shows performance specifications that this design meets.

Description	Symbol	Minimum	Typical	Maximum	Units	Comment
Input						
Voltage	V_{IN}		385		VDC	
Undervoltage	$V_{IN(UV)}$		290		VDC	
Overshoot	$V_{IN(OV)}$		430		VDC	
Main Output						
Output Voltage 1	V_{OUT1}	11.6	12	12.6	V	±5%
Output Ripple Voltage 1	$V_{RIPPLE1}$			120	mVp-p	20 MHz bandwidth
Output Current 1	I_{OUT1}	0.5	15.64	10	A	
Output Voltage 2	V_{OUT2}	11.6	12	12.6	V	±5%
Output Ripple Voltage 2	$V_{RIPPLE2}$			120	mVp-p	20 MHz bandwidth
Output Current 2	I_{OUT2}	0.5	15.64	7.5	A	
Output Voltage 3	V_{OUT3}	4.75	5	5.25	V	±5%
Output Ripple Voltage 3	$V_{RIPPLE3}$			50	mVp-p	20 MHz bandwidth
Output Current 3	I_{OUT3}	0	13.2	10.6	A	
Output Voltage 4	V_{OUT4}	3.15	3.3	3.4	V	±5%
Output Ripple Voltage 4	$V_{RIPPLE4}$			50	mVp-p	20 MHz bandwidth
Output Current 4	I_{OUT4}	0.5	11.12	7.6	A	
Output Voltage 5	V_{OUT5}	-11.4	-12	-13	V	±5%
Output Ripple Voltage 5	$V_{RIPPLE5}$			120	mVp-p	20 MHz bandwidth
Output Current 5	I_{OUT5}	0.1	0.1	0.2	A	
Standby Output						
Output Voltage	$V_{OUT(SB)}$	4.75	5	5.25	V	±5%
Output Ripple Voltage	$V_{RIPPLE(SB)}$			50	mVp-p	20 MHz bandwidth
Output Current	$I_{OUT(SB)}$	0	1.39	1.6	A	
Power and Efficiency						
Average Main Power	$P_{OUT(MAIN)}$		290		W	Main
Average Standby Power	$P_{OUT(SB)}$		10		W	Standby
Standby No-Load Power	P_{STDBY}			200	mW	Measured at 230 VAC
Average Total Power	$P_{OUT(TOTAL)}$		300		W	Total
Peak Power	$P_{OUT(PEAK)}$		380		W	Total
Efficiency at 20% & 100% Load	η	82			%	Overall power supply efficiency
Efficiency at 50% Load	η	85			%	Overall power supply efficiency
Hold-up Time at Maximum Load	T_{HOLDUP}	16 ms			ms	With $C_{IN} = 270 \mu F$
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Ambient Temperature	T_{AMB}	0		50	°C	Forced airflow

Table 3. 300 W Retrofit Performance Specifications.

The schematic below shows the primary side retrofit circuit using HiperTFS and HiperPFS. The primary schematic is broken into four main regions:

- AC input
- PFC preregulator
- Main forward converter
- Standby flyback converter

For detailed information on AC input and PFC regulator please refer to HiperPFS Application Note AN-52. Areas such as circuit design, layout considerations, inrush, EMI, efficiency, thermal considerations for HiperPFS are covered in AN-53.

Operation and Function of Primary Stages

The rectified AC input provides DC input to the standby and main converter when AC is first applied and the DC is above the standby undervoltage (UVSB) threshold (typically 100 VDC), the standby converter will begin switching. Once the standby is in regulation and a remote-on command is made from the secondary controller, a +12 V primary bias VCC_PFC is provided to the HiperPFS device which allows the HiperPFS to start switching, boosting the DC bulk cap voltage to 385 VDC. The remote-on command also initiates switching on the HiperTFS DC-DC forward converter once the DC input bulk capacitor C12 reaches the converter undervoltage threshold (UVMA typically 320 V). The functions of external support circuits are identical to the circuits used in RDK-249.

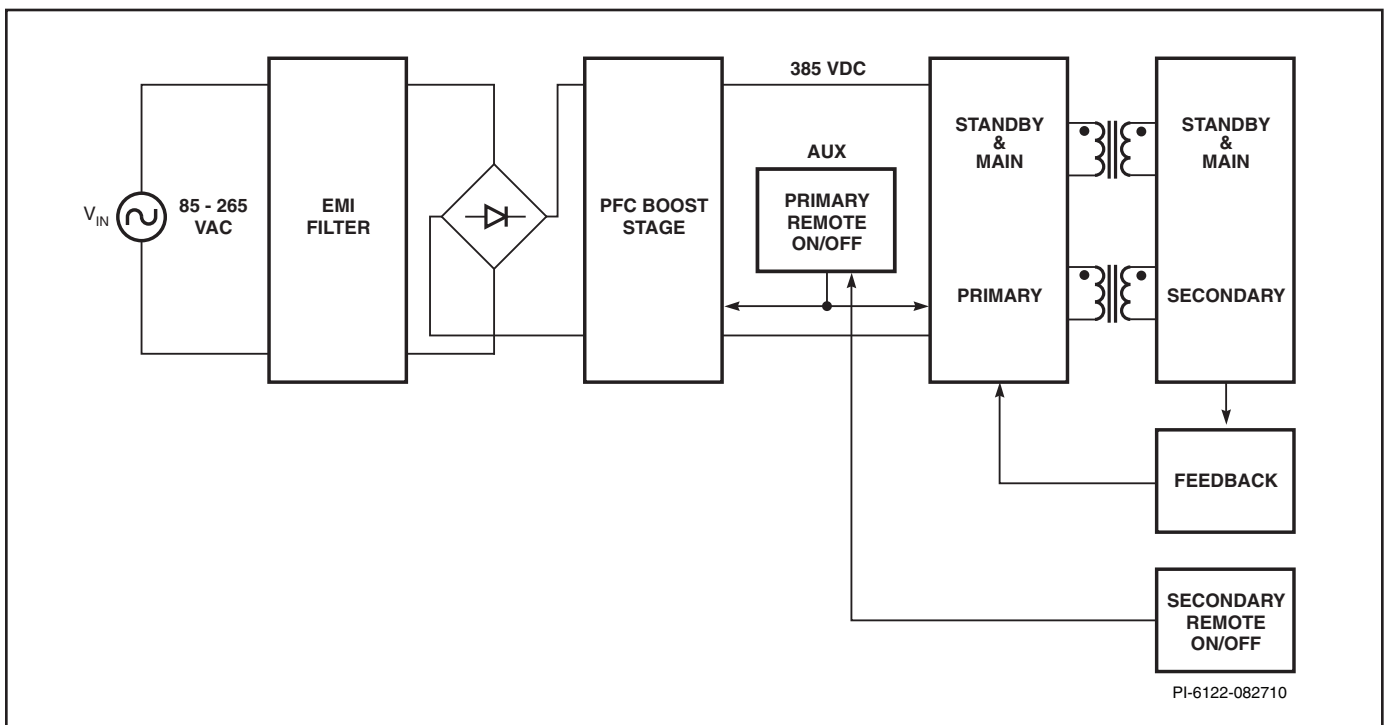


Figure 45. Power System Block Diagram.

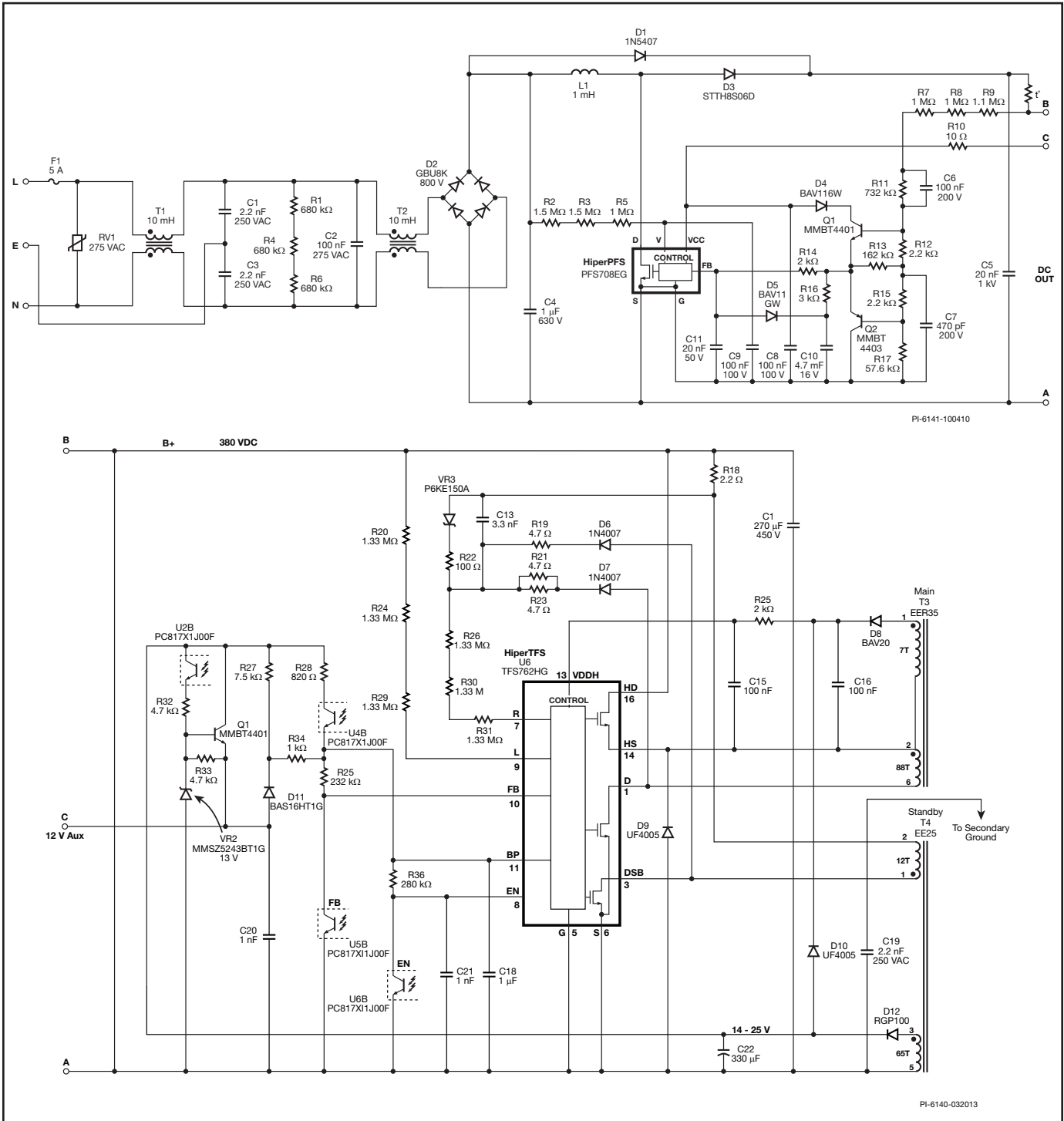


Figure 46. 300 W PC-ATX Supply Primary-Side Schematic.

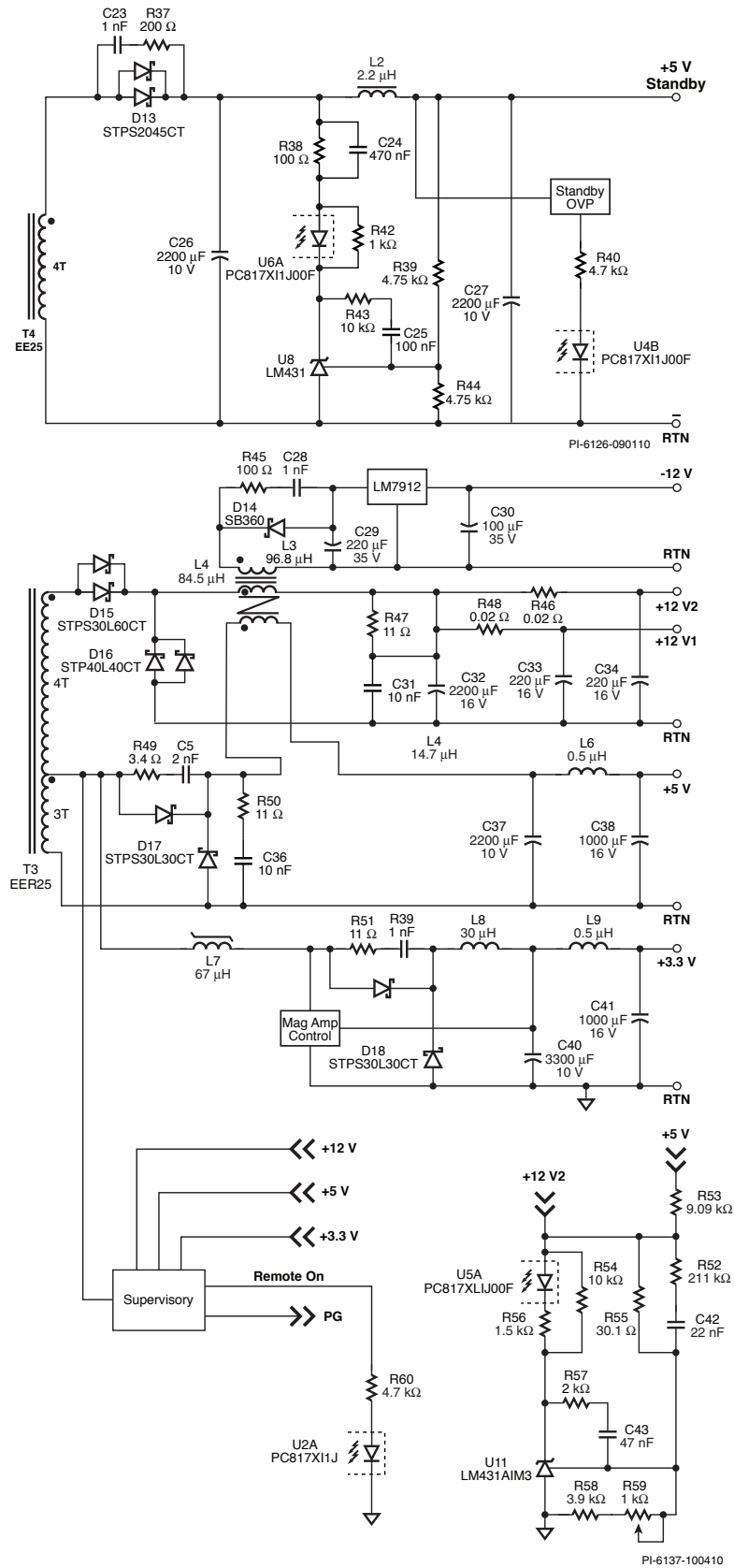


Figure 47. 300 W PC-ATX Supply Secondary-Side Schematic.

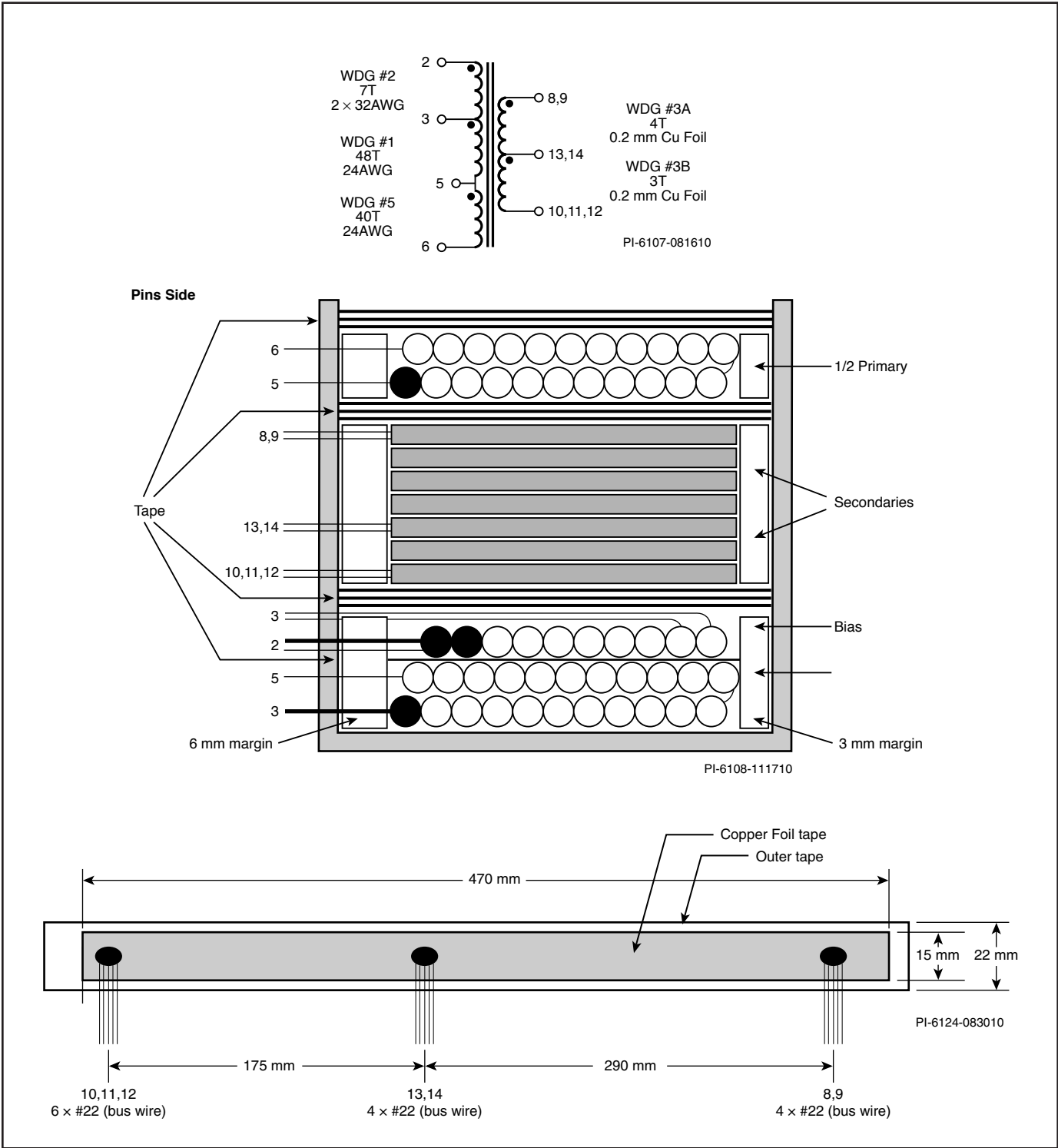


Figure 48. 300 W Main Transformer Schematic and Construction.

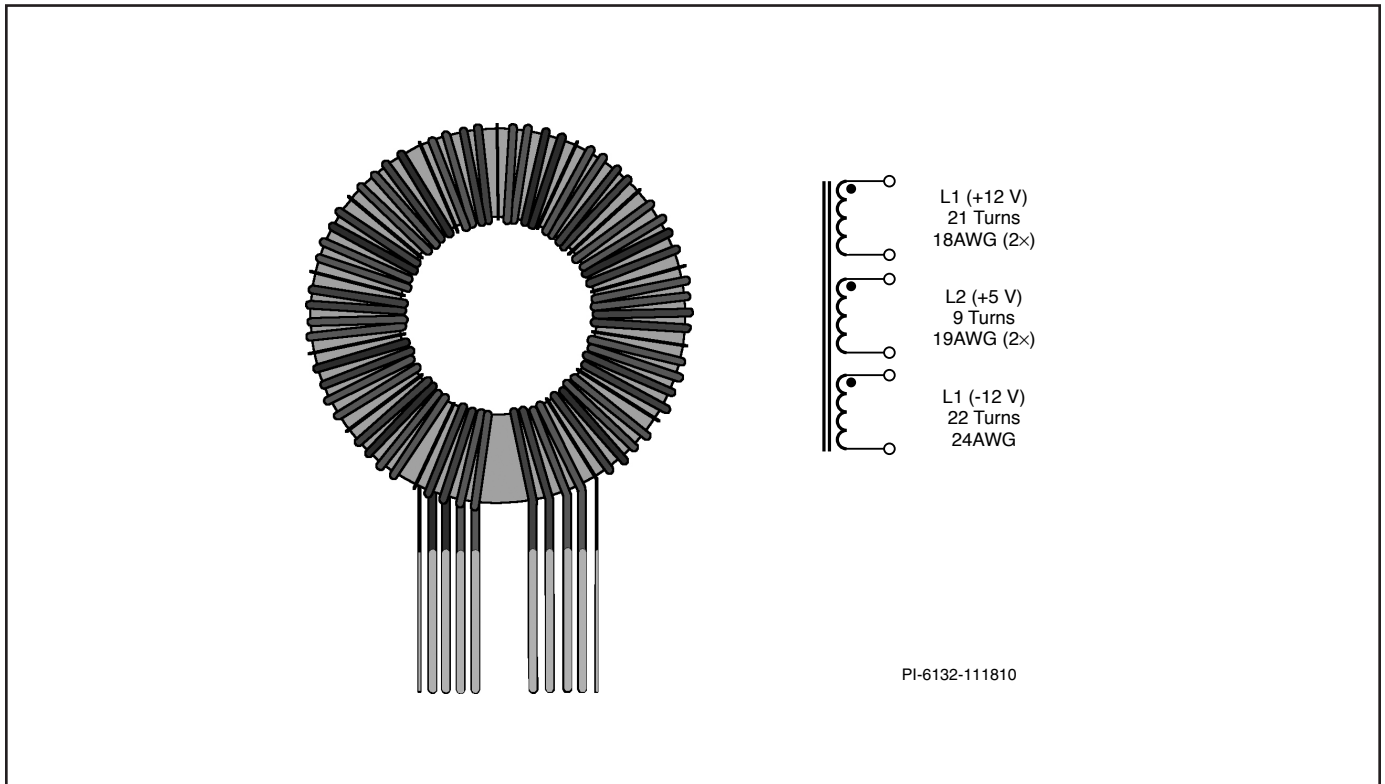


Figure 49. 300 W Main Coupled Inductor for +5 V, +12 V, -12 V Main.

Layout Considerations

For any switching power supply, layout is a critical aspect of a good design. Layout can effect stability, thermal rise of power components, EMI, and safety compliance. The key areas to consider for stable clean operation using HiperTFS have already been discussed in the RDK-249 section of the Application Note.

The key physical regions of the layout for this supply are:

- AC input bridge
- HiperPFS and boost diode heat sink
- HiperTFS heat sink
- Main transformer
- Standby transformer
- Secondary heat sink
- Coupled inductor
- Output capacitors

Layout: Electrical

The basic circuit regions described above should connect in a logical and clean manner to minimize interference between the stages. As can be seen in the layout example in Figure 50, the AC input starts at the lower right hand corner of the layout followed by the PFC stage which flows toward the upper left hand side. The main and standby stages move right toward the secondary. This is a very typical main wrap-around configuration. The AC input and line filter are located in a very quiet region to minimize EMI pickup from the noisier boost and DC converter stages. The grounding of the PFC stage is separate from the HiperTFS stage to avoid interaction. To avoid creating a high frequency ground loop, the bias capacitor, C23, is referenced to the HiperPFS device. The HiperPFS heat sink should always be grounded near its SOURCE pin to reduce conducted and radiated noise.

Layout: Thermal

The appropriate layout for HiperTFS includes proper airflow from the fan and a well designed heat sink. Most fans for PC supplies are exhaust type and it is important to direct sufficient airflow through the supply.

When considering any layout proposal, the impact on heat sink and main transformer thermal performance is especially important to keep foremost in mind. The HiperTFS heat sink should have enough area and access to airflow to allow no more than 4 °C/W heat sink to internal enclosure ambient as measured on the heat sink right behind the mounted HiperTFS device. These guidelines should keep the heat sink behind HiperTFS device below the 95 °C at maximum output power and 50 °C ambient. A heat sink temperature of 95 °C is the maximum advised behind the HiperTFS package in order to have sufficient margin below the internal thermal shutdown threshold of the device. Often heat sink arrangements can cause blockage of airflow across the magnetic components and at times, given layout constraints, airflow may need to be specifically channeled to the main transformer and coupled inductor regions by means of an air baffle. A baffle can be constructed of relatively inexpensive material such as plastic or “fish” paper.

The control circuits for HiperPFS are star ground to the GROUND pin. The optocoupler outputs for FEEDBACK pin and ENABLE pin of HiperTFS are star grounded to GROUND pin of HiperTFS.

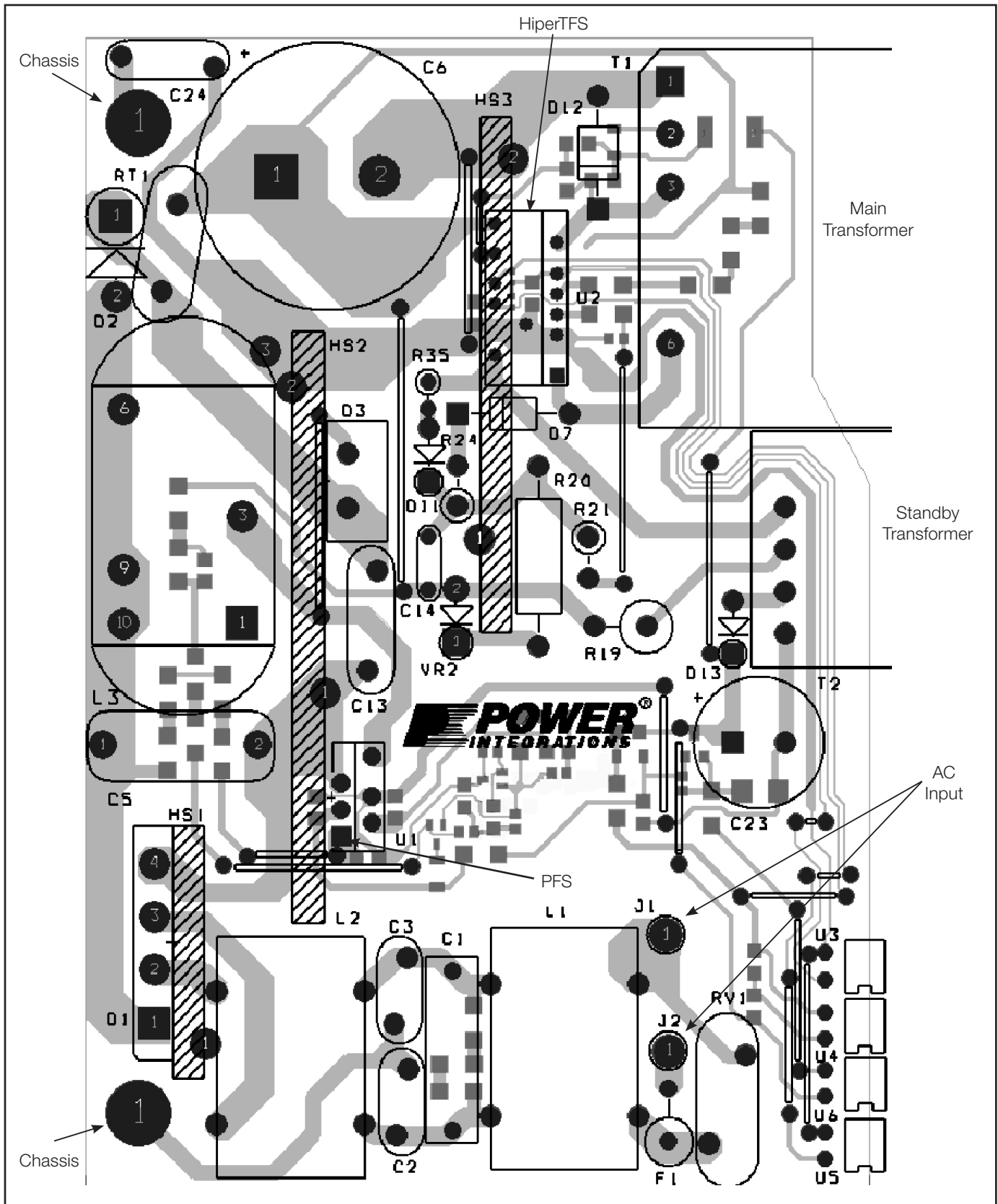


Figure 50. 300 W PC-ATX Primary-Side Layout.

The HiperTFS package is an eSIP-16B as shown in Figure 52. The exposed metal pad on the back of the package provides low thermal impedance for both the standby MOSFET and the bottom MOSFET for the main forward converter. There is also an over molded electrically isolated section at the package backside that provides a heat sink connection for the high-side MOSFET of the main forward converter. Thermal compound and a mounting clip that provides a force of ~50 Newtons are required for optimum thermal performance. Note there is no

need for an insulation (SIL) pad since the exposed pad of the device is referenced to SOURCE pin and hence electrically zero potential. The heat sink temperature behind the device should not exceed 95 °C to have adequate margin below the thermal shutdown threshold of the HiperTFS. Since some of the pins of the HiperTFS straddle under the heat sink there should a minimum vertical clearance of 0.078 inches between the heat sink and PC board.

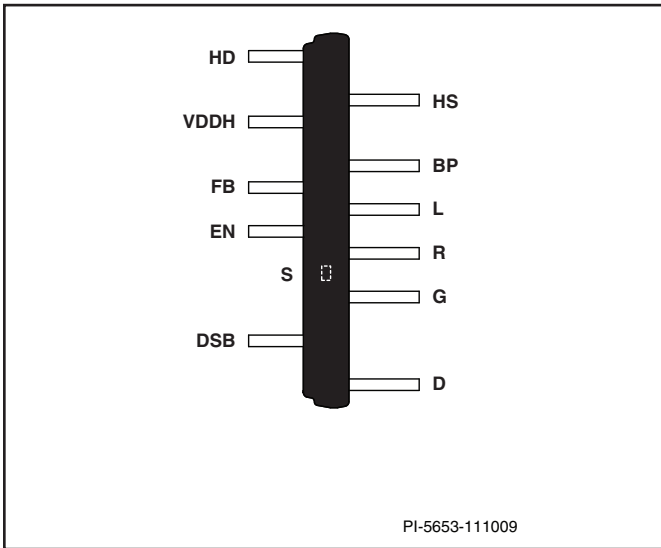


Figure 51. HiperTFS Pin Out.

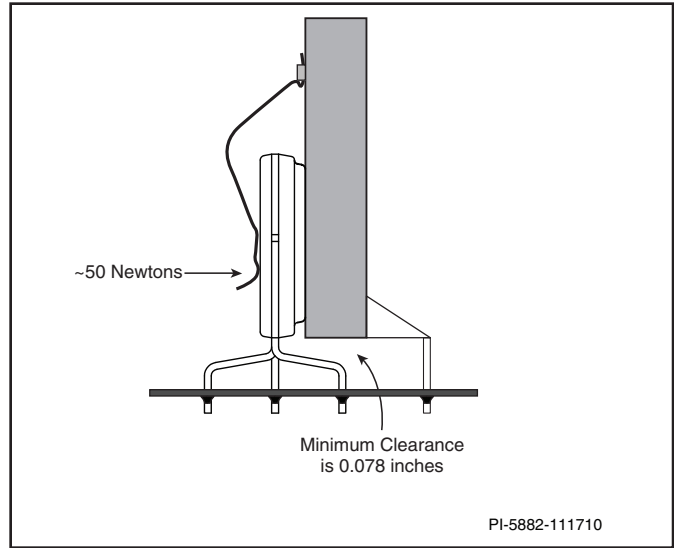


Figure 52. HiperTFS Heat Sink Mounting.

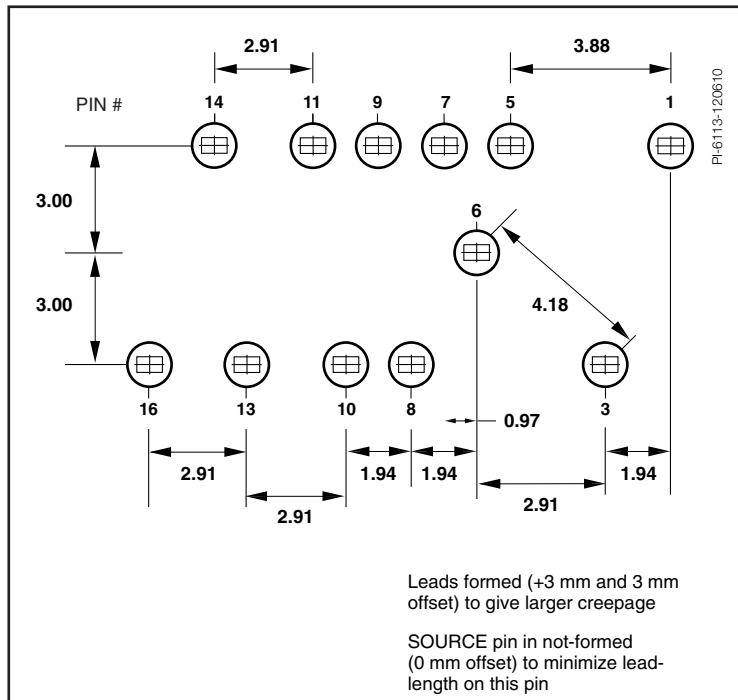


Figure 53. PCB Footprint.

Revision	Notes	Date
A	Initial Release.	11/09/10
A	Updated Figure 46.	03/20/13

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