InterFET Corporation

Semiconductor Databook


Revised January, 2000

InterFET Corporation
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Semiconductor Databook

Volume 4, Number 6

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InterFET Corporation
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InterFET Corporation

InterFET was founded in 1982 to design and manufacture Field-Effect Transistors. Having only one product has a way of focusing one's attention. "Good enough" isn't good enough. "Close" isn't close at all. That focus has worked for us. Every year we have grown, and every year we have improved our plant, our engineering, our processes, our quality, and our services. We are still focused on Field-Effect Transistors and related devices.

InterFET is big enough to competitively supply over 400 standard JFET types. Small enough to craft JFETs to your exact specifications. Big enough to supply national and international leading-edge electronic manufacturers and laboratories. Small enough for you to talk directly with the people that engineer and manufacture the product.

Every business has a culture, a way of doing business. Ours is… How we serve each customer is more important than how many customers we serve.

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Minimum Orders	$250 per line item (standard product).
Cancellation or Rescheduling	Standard product (databook) orders may be cancelled or rescheduled prior to 30 days of ship date without penalty. No cancellation or rescheduling will be accepted within 30 days of scheduled ship date.
Terms & Conditions	Net 30 days on approved credit.
Freight Charges	Prepaid and added to the invoice unless otherwise specified.
Shipping	F.O.B. Garland, Texas, via any carrier you wish, including UPS and Federal Express.
Specifications	InterFET device types are based on JEDEC or EIA registered data or InterFET datasheet specifications. Customer source-control drawings will be assigned special part numbers proprietary to the customer. Many combinations of selected electrical, process flow, and package configurations may be sourced from standard InterFET products.

InterFET Corporation makes no warranty regarding information furnished and reserves the right to make changes to standard products at any time and without notice. InterFET Corporation does not assume any liability arising from the application or use of InterFET data or products.

InterFET Corporation does not participate in life support system designs, nor knowingly sell products for life-support equipment. InterFET Corporation reserves the right to make changes in any product specifications any time without notice.

We have diligently checked and cross-checked the data in this book to coincide with published charts and drawings. Abbreviations have been updated and obvious errors corrected. When there were conflicts, logic was the prime guide, followed by experience. Printing and typography was accommodated in the interest of readability.

We suggest that, when ordering from InterFET, you also advise us of your specifications. Often, there are alternative solutions. If so, we want you to know the choices. And that, surely, is to your advantage.

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High-Reliability Process Flows

InterFET Corporation has served the military and industrial high-reliability junction field effect transistor market since 1984. There are standard high-reliability processing options available on most packaged and die products and are typically less costly than products supplied to source control drawing requirements.

Option-1 process flow provides most of the 100% screening steps for a MIL-STD-883, Method 5008 Class B die product.

Option-2 process flow provides most of the 100% screening steps for a JANTXV type device as defined by MIL-S-19500 requirements.

Option-3 process flow provides many of the 100% screening steps for a JANS type device as defined by MIL-S-19500 requirements.

Should Option-1, Option-2, or Option-3 process flows not meet your requirements, InterFET Corporation can provide processing based on your source control drawings and detail specifications. All MIL-S-19500/MIL-STD-750 requirements through JANS-level type processing can be provided. Manufacturing baseline control can be offered as an option.

We have earned a reputation in the industry for manufacturing High-Reliability products for a wide range of military and industrial users and would be pleased to work with you.

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Option 1 Process Flow Evaluation for High-Reliability Un-Encapsulated JFET Die

Screen	MIL-STD Method	Condition
Pre–Cap Visual	750-2072	100% @ 100X minimum Per InterFET PB-IN-GN04
Seal		Per InterFET PB-CW-MC01
Initial Electrical		Per InterFET PB-TS-EL00
Temperature Cycle	750-1051	Condition D, 20 cycles, –65° to +200°C, 15 minutes at extremes, minimum
Final Electrical		Per InterFET PB-FT-0000
Wire Bond Evaluation	883-2011	
Quality Conformance		Per InterFET QB-IN-GN04

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Option 2 Process Flow for High-Reliability Metal Case JFETs

Screen	MIL-STD Method	Condition
Pre–Cap Visual	750-2072	100% @ 100X minumum Per InterFET PB-IN-GN04
Seal		Per InterFET PB-CW-MC01
Initial Electrical		Per InterFET PB-TS-EL00
Stabilization Bake	750-1031	200°C for 24 hours
Temperature Cycle	750-1051	Condition D, 20 cycles, –65° to +200°C, 15 minutes at extremes, minimum
Constant Acceleration	750-2006	Y1 axis only, 20,000g
Fine Leak	750-1071	Condition G or H, 5E–8 atm/cc–sec maximum
Gross Leak	750-1071	Condition C
Pre–HTRB Electrical		Per InterFET PB-TS-EL01
HTRB–Conditioning	750-1039	Condition A, 150°C for 168 hours, minimum
Post–HTRB End Point Electrical		Per InterFET PB-FT-0000 within 24 hours
Final Electrical		Per InterFET PB-FT-0000 Optional if all customer required electrical parameters are included in Post-HTRBTest
Quality Conformance		Per InterFET QB-IN-GN04

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Option 3 Process Flow for Class S High-Reliability Metal Case JFETs

Screen	MIL-STD Method	Condition
Pre–Cap Visual	750-2072	100% @ 100X minimum Per InterFET PB-IN-GN04
Seal		Per InterFET PB-CW-MC01
Initial Electrical		Per InterFET PB-TS-EL00
Stabilization Bake	750-1031	200°C for 24 hours
Temperature Cycle	750-1051	Condition D, 20 cycles, -65° to +200°C, 15 minutes at extremes, minimum
Constant Acceleration	750-2006	Y1 axis only, 20,000g
PIND	883-2020	Condition A
Fine Leak	750-1071	Condition G or H, 5E–8 atm/cc–sec, max
Gross Leak	750-1071	Condition C
Pre–HTRB Electrical		Per InterFET PB-TS-EL01
HTRB–Conditioning	750-1039	Condition A, 150°C for 168 hours, minimum
Post–HTRB End Point Electrical		Per InterFET PB-FT-0000 within 24 hours
Radiography	750-2076	X1 & Y1 Directions
External Visual	750-2071	
Final Electrical		Per InterFET PB-FT-0000 Optional if all customer required electrical parameters are included in Post-HTRB Test
Quality Conformance		Per InterFET QB-IN-GN04

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InterFET Scientific

InterFET Scientific has been created to address the specialized needs of scientists, engineers and designers.

We are told that there are few other JFET manufacturers with our research data bank and our willingness to work in the scientific areas.

To some, JFETs are a commodity. To InterFET, JFETs are an emerging technology—ready to contribute to the applications of today and tomorrow.

We would be pleased to discuss your specific project or to send you an overview of our capabilities.

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InterFET Scientific

JFET and IC Research

InterFET and InterFET Scientific have participated in government laboratory projects at Brookhaven National Laboratory, Lawrence Berkeley Laboratories, INFN (Italian Nuclear Physics Institute) and others... plus grants from DOE/SBIR and the Texas Advanced Research Program.

InterFET Scientific has substantial experience partnering research and development with scientific and commercial customers that need very low noise, radiation tolerance, cryogenic operation or other special requirements.

New Process JFET Integrated Circuit Technology

JFET ICs are very specialized products, capable of meeting performance needs that no other IC technology can satisfy. Applications demanding extremely low-noise charge or signal amplification, or needing high tolerance to radiation or ESD are well suited to this new technology.

InterFET Scientific has developed this custom integrated circuit capability using exclusively n-channel JFET active components and on-board MOS capacitors and diffused resistors. This process uses P-well isolation and the same epitaxially formed channels which provide discrete JFETs their excellent low-noise and radiation-tolerant characteristics. Overall performance of sensitive preamplifier and amplifier applications is improved over hybrids using discrete JFETs due to reduction of chip and wire parasitics.

InterFET is capable of delivering a turnkey product, or, if you provide CAD layout, InterFET will work with you by providing the foundry work.

Custom Discrete JFET Designs

- Discrete JFETs with high gain (gm) and high gm/Cin ratio using tetrode (or dual gate) designs to allow minimum capacitance on the input gate.
- High performance discrete JFET designs to increase radiation tolerance using very small and tight design rules.
- Unusual discrete JFET designs, such as very large, high voltage, or other special design considerations.

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IFPA300, IFPA301

Monolithic JFET Preamplifier

Description & Features

The IFPA300 series is an inverting transimpedance amplifier featuring extremely low noise and a wide gain-bandwidth suitable as a charge-sensitive pre-amplifier for a broad range of applications.

The monolithic IFPA300 series contain 8 n-channel epitaxial-channel diffused-gate JFETs to achieve optimally low 1/f noise performance over a wide temperature range (120K-300K).

DC open loop gain	85 dB
GBW	200 MHz
$\bar{e}_N$ @ 10 Hz	3.0 nV/√Hz

General Specifications

Power Dissipation at VDD = 12 V	<100 mW
Input Leakage Current (T = 300 K)	10 pA
Input-Referred Noise Voltage (f = 10 kHz)	0.6 nV/√Hz
Input-Referred Noise Voltage (f = 10 Hz)	3.0 nV/√Hz
Output Range at VDD = 12 V	4.0 V (5.0 V Max)

Designed to drive 50Ω load.

Charge Sensitive Preamplifier Specifications

The IFPA300 Series is actually tailored to detector capacitance in the 100 – 1000 pF range.

Input Open-Loop Capacitance	60 pF
Rise Time (CD = 500 pF, Cf = 33 pF)	20 ns

Equivalent Noise Charge

(Measured with semigaussian shaping, peaking time = t_p)

4200 e– rms at CD @ 500 pF, t_p = 0.2 µm

3200 e– rms at CD @ 500 pF, t_p = 1.0 µm

4200 e– rms at CD @ 500 pF, t_p = 4.0 µm

Absolute maximum ratings at TA = 25°C

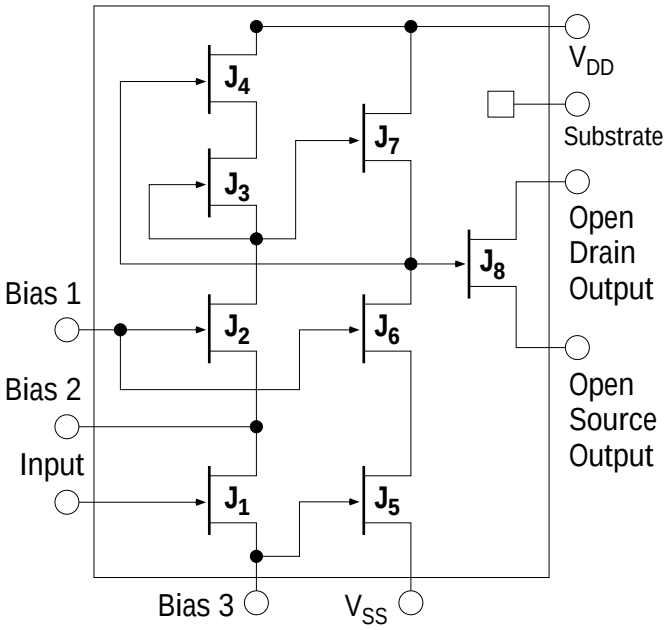
All pins (except Input) referenced to Bias 3	85 dB
Input to Bias 3	Ø V
Power Dissipation	225 mW
Derating Factor	1.8 mW/°C
Operating Temperature	150°C

At this time, there are two units in this family.

The 300/301 Series gives more flexibility with respect to output transistor drain.

The 310/311 Series ties the output transistor drain to the V_{DD} line.

Simplified Schematic Circuit



Packages & Test Circuit Overside

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IFPA300, IFPA301

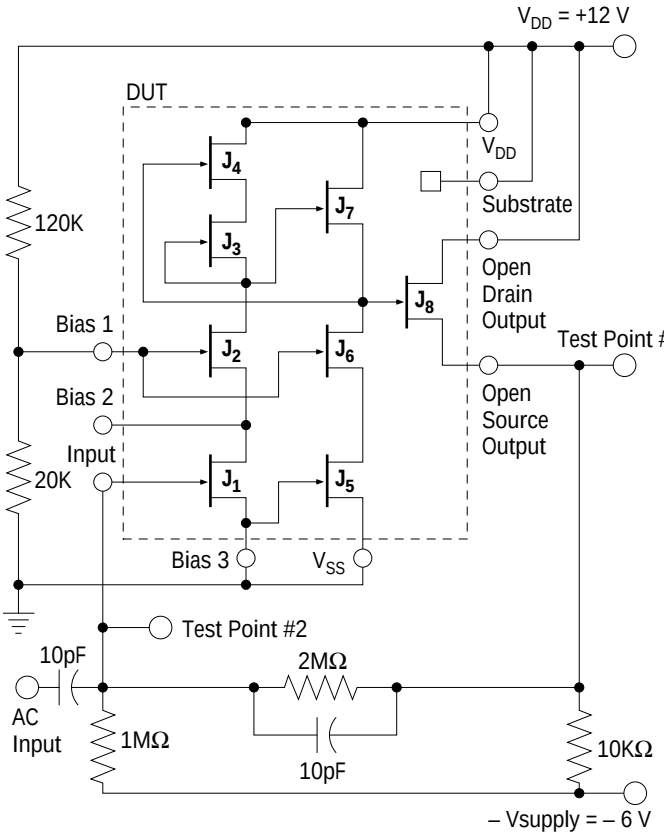
Monolithic JFET Preamplifier

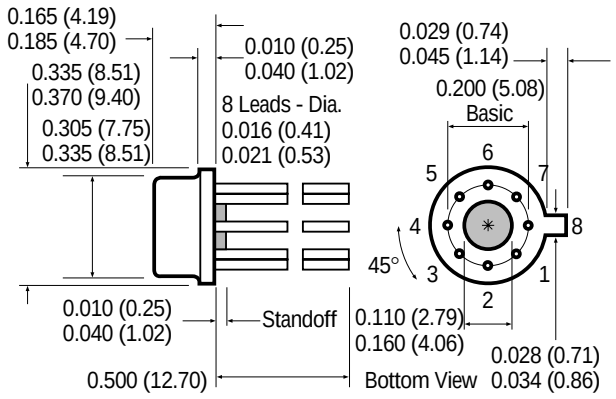
Input FET J1 selected to the following elecrical parameters.

Parameter	Conditions	Min	Max	Units
BV_{GSS}	Vds = 0, Ig = 1 µA	– 25		Volts
I_{GSS}	Vds = 0, Vgs = – 10 V		2	nA
I_{DSS}	Vds = 0, Vgs = 10 V	40	500	mA
$V_{GS(OFF)}$	Vds = 0, Id = 1 µA	1	2	Volts
G_M	Vgs = 0, Vds = 10 V	50		mM
V_{GSF}	Id = 1 µA	0.35	0.65	Volts

Test Circuit Reference

Parameter	Conditions	Min	Max	Units
VDCout	Vdd = 12 V, – VS = – 6 V Test pt #1	6	10	V
Vin	Vdd = 12 V, – VS = – 6 V Test pt #2	– 0.6	– 1.6	V
VACout	Vdd = 12 V, – VS = – 6 V t = O µsec	50		mV
VACout	Vdd = 12 V, – VS = – 6 V t = 100 µsec		20	mV



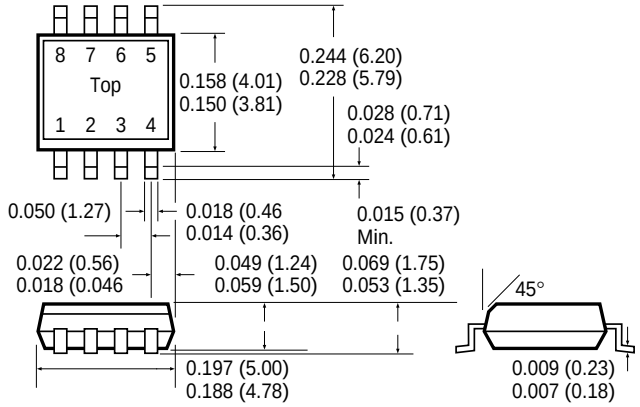


IFPA300 uses TO-99 Package

Dimensions in Inches (mm)

Pin Configuration

1 Bias 3, 2 VSS, 3 Bias 1, 4 VDD /Substrate
5 Open Drain Output, 6 Open Source Output, 7 Bias 2, 8 Input



IFPA301 uses SOIC-8 Package

Dimensions in Inches (mm)

Pin Configuration

1 Bias 2, 2 Input, 3 Bias 3, 4 VSS, 5 Bias 1, 6 VDD/Substrate
7 Open Drain Output, 8 Open Source Output

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InterFET Scientific – R&D

Problem: Low-noise amplification in hostile environment.

Solution: Integrated circuits using JFETs.

In the world of high energy physics the understanding of elementary particles and the origins of our universe has driven the need for larger and higher energy colliders. This requires a large array of radiation-hard, low-noise electronics to respond to the small input signals of the detectors which sense the results of high energy particle collisions.

The traditional way to handle this need for large calorimeter detectors is to locate small hybrid preamplifiers inside the liquified gas cryostat, near each detector segment, before the signal is sent out for further amplification and signal processing. This small hybrid circuit must operate in a high radiation environment, at temperatures approaching – 190°C! The heart of each preamplifier is a high gain JFET which offers superior noise capability and robust performance over MOSFET or bipolar technologies.

The problem with this approach is that the total power consumption and the cost of the hybrid circuits becomes a significant factor as the detector size and degree of segmentation grows. This could reach 100,000 or more channels for large equipment such as the experiments at CERN.

InterFET helped the scientists at the National Institute of Nuclear Physics in Italy (INFN) solve this problem by designing a smaller, monolithic preamplifier circuit. The manufacture of JFET integrated circuits is much more difficult than for MOSFETs due to differences in construction. Finding a way to electrically isolate individual JFET components on the circuit is the key to this success. In the beginning InterFET investigated several different types of isolation methods, until the buried layer approach was selected. The buried layer method allows a single, high quality layer of epitaxial silicon to form the channel of the JFET, the same as for discrete JFETs. It also provides for the selective placement of diffused "isolation pads" under the epitaxy layer to permit the necessary electrical isolation between circuit components. The rest of the process is the same as is used to manufacture InterFET's low-noise discrete JFETs.

The JFET integrated circuit for INFN is constructed entirely of n-channel JFETs, and consumes less space and power than the older hybrid approach. And, we were able to accomplish this without sacrificing any of the performance or radiation hardness of the discrete JFET in a hybrid circuit. InterFET Scientific has the experience and skills to provide JFET solutions—from initial design to final product in our Garland, Texas, facility. Our engineers would be happy to talk to you about your low-noise amplifier problems.

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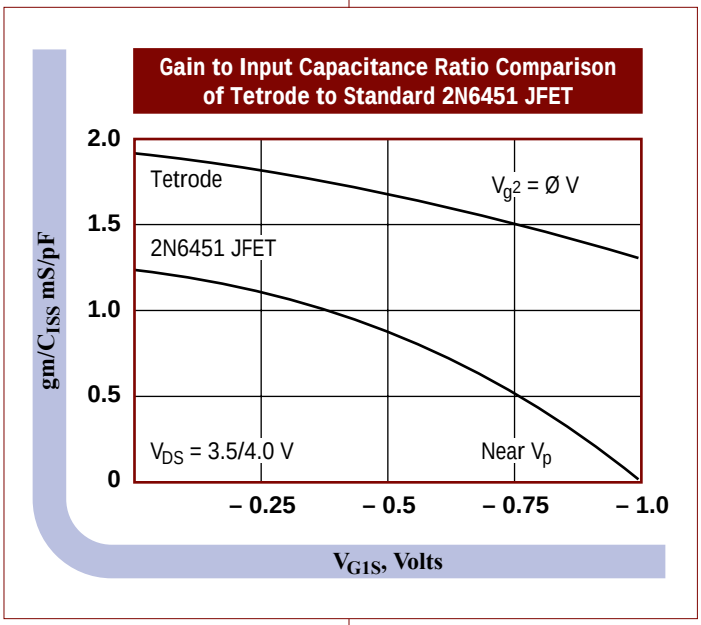
InterFET Scientific – R&D

Problem: A low-noise JFET with higher gain and less capacitance than is presently available.

Solution: InterFET Scientific Tetrodes and Circular JFETs.

The people at Lawrence Berkeley Laboratories needed to improve upon the performance of the industry standard 2N4416 JFET for their cooled X-ray detectors. They required a transistor with higher gain-to-capacitance ratio (gm/C) in order to achieve optimum performance. The industry makes a wide array of triode, (single gate) JFETs available. The problem is that a standard triode JFET comes with a lot of gate junction area which does not contribute to control of the channel current — it simply adds extra input capacitance. This reduces the high frequency cutoff of the transistor, and diminishes its low-noise performance.



InterFET Scientific worked with Lawrence Berkeley Labs to develop tetrode JFETs that separate the gate into two parts. The outer boundaries of the conduction channel are defined by the substrate gate. This requires a relatively large junction area, as is the case in triode designs. The other, top gate terminal is much smaller in area, and is located between the source and drain contacts—just enough to provide control over the channel current. By connecting only the top gate to the input signal we get maximum function control, for a minimum amount of unwanted input capacitance. InterFET Scientific designed a circular JFET, in order to reduce the size of the gate to the absolute minimum—with no end effect losses found in conventional, ladder types of JFET design. In application the substrate gate can be held at a fixed bias and the input signal is directed to the top gate.

Two different circle FETs were designed, one to replace a 2N4416 and the other for the 2N6451. The new approach has resulted in an increase in gm/C; up to 40% over the conventional JFET.

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Semiconductor Databook

Section A

Naming Convention

Selection Guide
By Application

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Semiconductor Naming Convention

JFETs, Diodes, Regulators & VCRs

Device part numbers in the InterFET Semiconductor Databook correspond to most industry standard part numbering schemes. They typically consist of a prefix containing two or more alpha-numeric characters followed by a sequence of 3 or 4 numbers.

- **IFxxxx**
- **IFNxxxx**
- **IFPxxxx**
- **SMPxxxx**

Part numbers prefixed with "I…" are unique InterFET parts which typically have no other industry source. "IFN…" and "IFP…" prefixed part numbers are normally InterFET variations of JEDEC "2N…" and Japanese "2SK…" and "2SJ…" part numbers. Examples are such as the IFN6449 which is an InterFET variation of the 2N6449 and the IFN112 which is an InterFET equivalent of the 2SK112. These equivalent parts typically perform the same function as the industry standards but may have some minor parametric variation or be offered in a different package than the registered part number.

Products in surface mount packages, SOT-23 and SOIC-8 have a "SMP…" prefix to the part number. This is normally a 3 or 4 digit number which corresponds to the standard or registered part number. An example of this is the SMP439I which is a 2N4391 equivalent device in an SOT-23 plastic surface mount package.

The "IPA..." part numbers are InterFET-specific numbers for a proprietary line of JFET integrated circuits. These manufacturer specific part numbers are also found in the databook.

- **Uxxxx**
- **Jxxxx**
- **PNxxxx**
- **PADxxxx**
- **DPADxxxx**
- **VCRxxxx**

Although the "U…" and "J…" part numbers are not JEDEC registered, they are accepted by users and manufacturers as standard industry part numbers. Several semiconductor manufacturers of JFETs include "U..." and "J…" part numbers in their data book. The "PN…" part numbers are normally TO-92 plastic encapsulated equivalents of "2N…" metal case part numbers. This is also an accepted industry practice. "PAD…" and "DPAD…" indicate that the device is a pico-Amp diode or a dual pico-Amp diode. Voltage controlled resistors will normally carry the "VCR…" prefix.

- **2Nxxxx**

JEDEC (Joint Electron Device Engineering Council) and EIA (Electronics Industry Association) standard for registered transistor part numbers specifies a "2N…" prefix. Most of the JFETs listed in the InterFET data book carry this part numbering scheme.

The numeric index has been compiled to find parts with the same number but different prefixes.

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Amplifiers

Audio

Differential

Low-Noise, High-Gain

VHF

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Semiconductor Selection Guide by Application

JFETs, Diodes, Regulators & VCRs

Choppers

Commutators

Current Limiting & Regulators

Electrometers

High Voltage

Japanese Equivalents

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Mixers

Oscillator

Pico-Ampere Diodes

Switches

Voltage-Controlled Resistors

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Semiconductor Selection Guide by Application

JFETs, Diodes, Regulators & VCRs

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Semiconductor Databook
Section B

JFET Data Sheets

These are our most called-for devices. This is certainly not the limit of our capabilities. We can and do manufacture any of the standard registered parts. We also customize any standard or proprietary device to your specifications.

Data Sheet Index

Silicon Junction Field-Effect Transistors

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2N3821, 2N3822

N-Channel Silicon Junction Field-Effect Transistor

- VHF Amplifiers
- Small Signal Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 50 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	2mW/°C

At 25°C free air temperature:		2N3821		2N3822		Process NJ32		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 50		– 50		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1		– 0.1	nA	V_{GS} = – 30V, V_{DS} = ØV	
			– 0.1		– 0.1	µA	V_{GS} = – 30V, V_{DS} = ØV	T_A = 150°C
Gate Source Voltage	V_{GS}	– 0.5	– 2			V	V_{DS} = 15V, I_D = 50 µA	
				– 1	– 4	V	V_{DS} = 15V, I_D = 200 µA	
						V	V_{DS} = 15V, I_D = 400 µA	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$		– 4		– 6	V	V_{DS} = 15V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	0.5	2.5	2	10	mA	V_{DS} = 15V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$					nA	V_{DS} = 15V, V_{GS} = – 8V	
						µA	V_{DS} = 15V, V_{GS} = – 8V	T_A = 150°C
Dynamic Electrical Characteristics								
Drain Source ON Resistance	$r_{ds(on)}$					Ω	V_{GS} = ØV, I_D = ØV	f = 1 kHz
Common Source Forward Transconductance	g_{fs}	1500	4500	3000	6500	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Forward Transmittance	$\lvert Y_{fs} \rvert$	1500		3000		µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
Common Source Output Conductance	g_{os}		10		20	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		6		6	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		2		2	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		200		200	nV/√Hz	V_{DS} = 15V, V_{GS} = ØV	f = 10 Hz
Noise Figure	NF		5		5	dB	V_{DS} = 15V, V_{GS} = ØV R_G = 1MΩ	f = 10 Hz

TO-72 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate, 4 Case

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2N3823, 2N3824

N-Channel Silicon Junction Field-Effect Transistor

- VHF Amplifiers
- Small Signal Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 50 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	2 mW/°C

At 25°C free air temperature:		2N3823		2N3824		Process NJ32		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 30		– 50		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.5		– 0.1	nA	V_{GS} = – 30V, V_{DS} = ØV	
			– 0.5		– 0.1	µA	V_{GS} = – 30V, V_{DS} = ØV	T_A = 150°C
Gate Source Voltage	V_{GS}	– 1	– 7.5			V	V_{DS} = 15V, I_D = 400 µA	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$		– 8			V	V_{DS} = 15V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	4	20			mA	V_{DS} = 15V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$				0.1	nA	V_{DS} = 15V, V_{GS} = – 8V	
					0.1	µA	V_{DS} = 15V, V_{GS} = – 8V	T_A = 150°C
Dynamic Electrical Characteristics								
Drain Source ON Resistance	$r_{ds(on)}$				250	Ω	V_{GS} = ØV, I_D = ØV	f = 1 kHz
Common Source Forward Transconductance	g_{fs}	3500	6500			µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Forward Transmittance	$\lvert Y_{fs} \rvert$	3200				µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
Common Source Output Conductance	g_{os}		35			µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		6		6	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		2		3	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		200			nV/√Hz	V_{DS} = 15V, V_{GS} = ØV	f = 10 Hz
Noise Figure	NF		6			dB	V_{DS} = 15V, V_{GS} = ØV R_G = 1MΩ	f = 10 Hz

TO-72 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate, 4 Case

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2N3954, 2N3955, 2N3956

N-Channel Dual Silicon Junction Field-Effect Transistor

- Low and Medium Frequency Differential Amplifiers
- High Input Impedance Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 50 V
Gate Current	50 mA
Total Device Power Dissipation (each side)	250 mW
@ 85°C Case Temperature (both sides)	500 mW
Power Derating (both sides)	4.3 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		2N3954		2N3955		2N3956		Process NJ16		
		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 50		– 50		– 50		V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 100		– 100		– 100	pA	V_{GS} = – 30V, V_{DS} = ØV	
			– 500		– 500		– 500	nA	V_{GS} = – 30V, V_{DS} = ØV	T_A = 125°C
Gate Operating Current	I_G		– 50		– 50		– 50	pA	V_{DS} = 20V, I_D = 200 µA	
			– 250		– 250		– 250	nA	V_{DS} = 20V, I_D = 200 µA	T_A = 125°C
Gate Source Voltage	V_{GS}		– 4.2		– 4.2		– 4.2	V	V_{DS} = 20V, I_D = 50 µA	
		– 0.5	– 4	– 0.5	– 4	– 0.5	– 4	V	V_{DS} = 20V, I_D = 200 µA	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1	– 4.5	– 1	– 4.5	– 1	– 4.5	V	V_{DS} = – 20V, I_G = 1 nA	
Gate Source Forward Voltage	$V_{GS(F)}$		2		2		2	V	V_{DS} = ØV, I_G = 1 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	0.5	5	0.5	5	0.5	5	mA	V_{DS} = 20V, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Common Source Forward Transconductance	g_{fs}	1000	3000	1000	3000	1000	3000	µS	V_{DS} = 20V, V_{GS} = ØV	f = 1 kHz
		1000		1000		1000		µS	V_{DS} = 20V, V_{GS} = ØV	f = 200 MHz
Common Source Output Capacitance	g_{os}		35		35		35	µS	V_{DS} = 20V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		4		4		4	pF	V_{DS} = 20V, V_{GS} = ØV	f = 1 MHz
Drain Gate Capacitance	C_{dgo}		1.5		1.5		1.5	pF	V_{dg} = 10V, I_S = ØA	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		1.2		1.2		1.2	pF	V_{DS} = 20V, V_{GS} = ØV	f = 1 MHz
Noise Figure	NF		0.5		0.5		0.5	dB	V_{DS} = 20V, V_{GS} = ØV, R_g = 10 MΩ	f = 100 Hz
Differential Gate Current	$\lvert I_{G1} - I_{G2} \rvert$		10		10		10	nA	V_{DS} = 20V, I_D = 200µA	T_A = 125°C
Saturation Drain Current Ratio	I_{DSS1}/I_{DSS2}	0.95	1	0.95	1	0.95	1		V_{DS} = 20V, V_{GS} = ØV	
Differential Gate Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$		5		10		15	mV	V_{DS} = 20V, I_D = 200µA	
Differential Gate Source Voltage with Temperature	$\frac{\Delta V_{GS1} - V_{GS2}}{\Delta T}$		0.8		2		4	mV/°C	V_{DS} = 20V, I_D = 200µA	T_A = 25°C to = – 55°C
			1		2.5		5	mV/°C	V_{DS} = 20V, I_D = 200µA	T_A = 25°C to = +125°C
Transconductance Ratio	g_{fs1}/g_{fs2}	0.97	1	0.97	1	0.97	1		V_{DS} = 20V, I_D = 200µA	f = 1 kHz

TO-71 Package

See Section G for Outline Dimensions

Pin Configuration

1 Source, 2 Drain, 3 Gate,
5 Source, 6 Drain, 7 Gate

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2N3957, 2N3958

N-Channel Dual Silicon Junction Field-Effect Transistor

- Low and Medium Frequency Differential Amplifiers
- High Input Impedance Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 50 V
Gate Current	50 mA
Total Device Power Dissipation (each side)	250 mW
@ 85°C Case Temperature (both sides)	500 mW
Power Derating (both sides)	4.3 mW/°C

At 25°C free air temperature:		2N3957		2N3958		Process NJ16		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 50		– 50		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 100		– 100	pA	V_{GS} = – 30 V, V_{DS} = ØV	
			– 500		– 500	nA	V_{GS} = – 30 V, V_{DS} = ØV	T_A = 125°C
Gate Operating Current	I_G		– 50		– 50	pA	V_{DS} = 20 V, I_D = 200 µA	
			– 250		– 250	nA	V_{DS} = 20 V, I_D = 200 µA	T_A = 125°C
Gate Source Voltage	V_{GS}		– 4.2		– 4.2	V	V_{DS} = 20 V, I_D = 50 µA	
		– 0.5	– 4	– 0.5	– 4	V	V_{DS} = 20 V, I_D = 200 µA	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1	– 4.5	– 1	– 4.5	V	V_{DS} = 20 V, I_D = 1 nA	
Gate Source Forward Voltage	$V_{GS(F)}$		2		2	V	V_{DS} = Ø, I_G = 1 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	0.5	5	0.5	5	mA	V_{DS} = 20 V, V_{GS} = ØV	
Dynamic Electrical Characteristics								
Common Source Forward Transconductance	g_{fs}	1000	3000	1000	3000	µS	V_{DS} = 20 V, V_{GS} = ØV	f = 1 kHz
		1000		1000		µS	V_{DS} = 20 V, V_{GS} = ØV	f = 200 MHz
Common Source Output Conductance	g_{os}		35		35	µS	V_{DS} = 20 V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		4		4	pF	V_{DS} = 20 V, V_{GS} = ØV	f = 1 MHz
Drain Gate Capacitance	C_{dgo}		1.5		1.5	pF	V_{DS} = 10 V, I_S = ØA	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		1.2		1.2	pF	V_{DS} = 20 V, V_{GS} = ØV	f = 1 MHz
Noise Figure	NF		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = ØV R_G = 10 MΩ	f = 100 Hz
Differential Gate Current	$\lvert I_{G1} - I_{G2} \rvert$		10		10	nA	V_{DS} = 20 V, I_D = 200 µA	T_A = 125°C
Saturation Drain Current Ratio	I_{DSS1} / I_{DSS2}	0.9	1	0.85	1		V_{DS} = 20 V, V_{GS} = ØV	
Differential Gate Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$		20		25	mV	V_{DS} = 20 V, I_D = 200 µA	
Differential Gate Source Voltage with Temperature	$\frac{\Delta V_{GS1} - V_{GS2}}{\Delta T}$		6		8	mV	V_{DS} = 20 V, I_D = 200 µA	T_A = 25°C to – 55°C
			7.5		10	mV	V_{DS} = 20 V, I_D = 200 µA	T_A = 25°C to 125°C
Transconductance Ratio	g_{fs1} / g_{fs2}	0.9	1	0.85	1		V_{DS} = 20 V, I_D = 200 µA	f = 1 kHz

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TO-71 Package
See Section G for Outline Dimensions

Pin Configuration
1 Source, 2 Drain, 3 Gate, 5 Source, 6 Drain, 7 Gate

2N3993, 2N3993A

P-Channel Silicon Junction Field-Effect Transistor

- Choppers
- High Speed Commutators

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	25 V
Continuous Forward Gate Current	– 10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	2.4 mW/°C

At 25°C free air temperature:		2N3993		2N3993A		Process PJ99		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	25		25		V	I_G = 1 µA, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	4	9.5	4	9.5	V	V_{DS} = – 10V, I_D = – 1 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	– 10		– 10		mA	V_{DS} = – 10V, V_{GS} = ØV	
Drain Reverse Current	I_{DGO}		– 1.2		– 1.2	nA	V_{DG} = – 15V, I_S = ØA	
			– 1.2		– 1.2	µA	V_{DG} = – 15V, I_S = ØA	T_A = 150°C
Drain Cutoff Current	$I_{D(OFF)}$		– 1.2		– 1.2	nA	V_{DS} = – 10V, V_{GS} = 10 V	
			– 1		– 1	µA	V_{DS} = – 10V, V_{GS} = 10 V	T_A = 150°C
Dynamic Electrical Characteristics								
Drain Source ON Resistance	$r_{ds(on)}$		150		150	Ω	V_{GS} = ØV, I_D = Ø A	f = 1 kHz
Common Source Forward Transmittance	$\lvert Y_{fs} \rvert$	6	12	7	12	mS	V_{DS} = – 10V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		16		12	pF	V_{DS} = – 10V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		4.5		3	pF	V_{DS} = Ø, V_{GS} = 10V	f = 1 MHz

TO-72 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Gate, 3 Drain, 4 Case

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2N3994, 2N3994A

P-Channel Silicon Junction Field-Effect Transistor

- Choppers
- High Speed Commutators

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source Voltage	25 V
Reverse Gate Drain Voltage	25 V
Continuous Forward Gate Current	– 10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	2.4 mW/°C

At 25°C free air temperature:		2N3994		2N3994A		Process PJ99		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	25		25		V	I_G = 1 µA, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	1	5.5	1	5.5	V	V_{DS} = – 10V, I_D = – 1 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	– 2		– 2		mA	V_{DS} = – 10V, V_{GS} = ØV	
Drain Reverse Current	I_{DGO}		– 1.2		– 1.2	nA	V_{DG} = – 15V, I_S = ØA	
			– 1.2		– 1.2	µA	V_{DG} = – 15V, I_S = ØA	T_A = 150°C
Drain Cutoff Current	$I_{D(OFF)}$		– 1.2		– 1.2	nA	V_{DS} = – 10V, V_{GS} = 10V	
			– 1		– 1	µA	V_{DS} = – 10V, V_{GS} = 10V	T_A = 150°C
Dynamic Electrical Characteristics								
Drain Source ON Resistance	$r_{ds(on)}$		300		300	Ω	V_{GS} = ØV, I_D = ØA	f = 1 kHz
Common Source Forward Transmittance	$\lvert Y_{fs} \rvert$	4	10	5	10	mS	V_{DS} = – 10V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		16		12	pF	V_{DS} = – 10V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		5		3.5	pF	V_{DS} = Ø, V_{GS} = 10V	f = 1 MHz

TO-72 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Gate, 3 Drain, 4 Case

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2N4117, 2N4117A, 2N4118, 2N4118A, 2N4119, 2N4119A

N-Channel Silicon Junction Field-Effect Transistor

- Audio Amplifiers
- Ultra-High Input Impedance Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 40 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	300 mW
Power Derating (to 175°C)	2 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		2N4117 2N4117A		2N4118 2N4118A		2N4119 2N4119A		Process NJ01		
		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 40		– 40		– 40		V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current 2N4117, 2N4118, 2N4119	I_{GSS}		– 10		– 10		– 10	pA	V_{GS} = – 20V, V_{DS} = ØV	
2N4117A, 2N4118A, 2N4119A			– 1		– 1		– 1	pA	V_{GS} = – 20V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.6	– 1.8	– 1	– 3	– 2	– 6	V	V_{DS} = 10V, I_D = 1 nA	
Drain Saturation Current (Pulsed) 2N4117, 2N4118, 2N4119	I_{GSS}	0.03	0.09	0.08	0.24	0.2	0.6	mA	V_{DS} = 10V, V_{GS} = ØV	
2N4117A, 2N4118A, 2N4119A		0.015	0.09	0.08	0.24	0.2	0.6	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Common Source Forward Transconductance	g_{fs}	70	210	80	250	100	330	µS	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Common Source Output Conductance	g_{os}		3		5		10	µS	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		3		3		3	pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		1.5		1.5		1.5	pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 MHz

TO-72 Package

Dimensions in Inches (mm)

Pin Configuration

1 Source, 2 Drain, 3 Gate, 4 Case

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2N4220, 2N4220A, 2N4221, 2N4221A, 2N4222, 2N4222A

N-Channel Silicon Junction Field-Effect Transistor

- Mixers
- Oscillators
- VHF Amplifiers
- Small Signal Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 30 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating (to 150 °C)	2 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		2N4220 2N4220A NJ16 Min	2N4220 2N4220A NJ16 Max	2N4221 2N4221A NJ16 Min	2N4221 2N4221A NJ16 Max	2N4222 2N4222A NJ32 Min	2N4222 2N4222A NJ32 Max	Process Unit	Process Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 30		– 30		– 30		V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1		– 0.1		– 0.1	nA	V_{GS} = – 15V, V_{DS} = ØV	
			– 0.1		– 0.1		– 0.1	µA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 150°C
Gate Source Voltage	V_{GS}	– 0.5 (50)	– 2.5 (50)	– 1 (200)	– 5 (200)	– 2 (500)	– 6 (500)	V µA	V_{DS} = 15V, I_D = ( )	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$		– 4		– 6		– 8	V	V_{DS} = 15V, I_D = 0.1 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	0.5	3	2	6	5	15	mA	V_{DS} = 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Common Source Forward Transconductance	g_{fs}	1000	4000	2000	5000	2500	6000	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Forward Transmittance	$\lvert Y_{fs} \rvert$	750		750		750		µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
Common Source Output Conductance	g_{os}		10		20		40	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		6		6		6	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		2		2		2	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Noise Figure **2N4220A, 2N4221A, 2N4222A**	NF		2.5		2.5		2.5	dB	V_{DS} = 15V, V_{GS} = ØV R_G = 1 MΩ	f = 100 MHz

TO-72 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate, 4 Case

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2N4338, 2N4339

N-Channel Silicon Junction Field-Effect Transistor

- Audio Amplifiers
- Small Signal Amplifiers
- Voltage-Controlled Resistors
- Current Limiters & Regulators

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 50 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	300 mW
Power Derating (to 175°C)	2mW/°C

At 25°C free air temperature:		2N4338		2N4339		Process NJ16		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 50		– 50		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 100		– 100	pA	V_{GS} = – 30V, V_{DS} = ØV	
			– 100		– 100	nA	V_{GS} = – 30V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.3	– 1	– 0.6	– 1.8	V	V_{DS} = 15V, I_D = 0.1 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	0.2	0.6	0.5	1.5	mA	V_{DS} = 15V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$		0.05 (– 5)		0.05 (– 5)	nA V	V_{DS} = 15V, V_{GS} = ( )	
Dynamic Electrical Characteristics								
Drain Source ON Resistance	$r_{ds(on)}$		2500		1700	Ω	V_{GS} = ØV, I_D = Ø A	f = 1 kHz
Common Source Forward Transconductance	g_{fs}	600	1800	800	2400	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Output Conductance	g_{os}		5		15	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		7		7	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		3		3	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Noise Figure	NF		1		1	dB	V_{DS} = 15V, V_{GS} = ØV R_G = 1 MΩ, BW = 200 Hz	f = 1 kHz

TO-18 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

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2N4340, 2N4341

N-Channel Silicon Junction Field-Effect Transistor

- Small Signal Amplifiers
- Current Regulators
- Voltage-Controlled Resistors

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 50 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	300 mW
Power Derating (to 175°C)	2mW/°C

At 25°C free air temperature:		2N4340		2N4341		Process NJ16		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 50		– 50		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 100		– 100	pA	V_{GS} = – 30 V, V_{DS} = ØV	
			– 100		– 100	nA	V_{GS} = – 30 V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1	– 3	– 2	– 6	V	V_{DS} = 15 V, I_D = 0.1 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	1.2	3.6	3	9	mA	V_{DS} = 15 V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$		0.05 (– 5)		0.07 (– 10)	nA V	V_{DS} = 15 V, V_{GS} = ( )	

Dynamic Electrical Characteristics

Drain Source ON Resistance	$r_{ds(on)}$		1500		800	Ω	V_{GS} = ØV, I_D = Ø A	f = 1 kHz
Common Source Forward Transconductance	g_{fs}	1300	3000	2000	4000	µS	V_{DS} = 15 V, V_{GS} = ØV	f = 1 kHz
Common Source Output Conductance	g_{os}		30		60	µS	V_{DS} = 15 V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		7		7	pF	V_{DS} = 15 V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		3		3	pF	V_{DS} = 15 V, V_{GS} = ØV	f = 1 MHz
Noise Figure	NF		1		1	dB	V_{DS} = 15 V, V_{GS} = ØV R_G = 1 MΩ, BW = 200 Hz	f = 1 kHz

TO-18 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

Surface Mount
SMP4340, SMP4341

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2N4391, 2N4392, 2N4393

N-Channel Silicon Junction Field-Effect Transistor

- Low On Resistance Analog Switches
- Choppers
- Commutators

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 40 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	1.8 W
Power Derating	12 mW/°C

At 25°C free air temperature Static Electrical Characteristics		2N4391		2N4392		2N4393		Process NJ132		
		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 40		– 40		– 40		V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 100		– 100		– 100	pA	V_{GS} = – 20V, V_{DS} = ØV	
			– 200		– 200		– 200	nA	V_{GS} = – 20V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 4	– 10	– 2	– 5	– 0.5	– 3	V	V_{DS} = – 20V, I_D = 1 nA	
Gate Source Forward Voltage	$V_{GS(F)}$		1		1		1	V	I_G = 1 mA, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	50	150	25	75	5	30	mA	V_{DS} = 20V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$						100	pA	V_{DS} = 20V, V_{GS} = – 5V	
							200	nA	V_{DS} = 20V, V_{GS} = – 5V	T_A = 150°C
					100			pA	V_{DS} = 20V, V_{GS} = – 7V	
					200			nA	V_{DS} = 20V, V_{GS} = – 7V	T_A = 150°C
			100					pA	V_{DS} = 20V, V_{GS} = – 12V	
			200					nA	V_{DS} = 20V, V_{GS} = – 12V	T_A = 150°C
Drain Source ON Voltage	$V_{DS(ON)}$						0.4	V	V_{GS} = ØV, I_D = 3 mA	
					0.4			V	V_{GS} = ØV, I_D = 6 mA	
			0.4					V	V_{GS} = ØV, I_D = 12 mA	
Static Drain Source ON Resistance	$r_{DS(ON)}$		30		60		100	Ω	V_{GS} = ØV, I_D = 1 mA	
Dynamic Electrical Characteristics										
Drain Source ON Resistance	$r_{ds(on)}$		30		60		100	Ω	V_{GS} = ØV, I_D = ØA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		14		14		14	pF	V_{DS} = 20V, V_{GS} = ØV	f = 1 kHz
Common Source Reverse Transfer Capacitance	C_{rss}						3.5	pF	V_{DS} = ØV, V_{GS} = – 5V	f = 1 kHz
					3.5			pF	V_{DS} = ØV, V_{GS} = – 7V	f = 1 kHz
			3.5					pF	V_{DS} = ØV, V_{GS} = – 12V	f = 1 kHz
Switching Characteristics										
Turn ON Delay Time	$t_{d(on)}$		15		15		15	ns	V_{DD} = 10V, $V_{GS(ON)}$ = ØV	
Rise Time	t_r		5		5		5	ns		
Turn OFF Delay Time	$t_{d(off)}$		20		35		50	ns		
Fall Time	t_f		15		20		30	ns		

	2N4391	2N4392	2N4393	
$I_{D(ON)}$	12	6	3	mA
$V_{GS(OFF)}$	– 12	– 7	– 5	V

TO-18 Package
See Section G for Outline Dimensions

Surface Mount
SMP4391, SMP4392, SMP4393

Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

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2N4416, 2N4416A

N-Channel Silicon Junction Field-Effect Transistor

- Mixers
- VHF Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	2N4416	– 30 V	2N4416A	– 35 V
Gate Current		10 mA		10 mA
Continuous Device Dissipation		300 mW		300 mW
Power Derating		2 mW°C		2 mW/°C

At 25°C free air temperature:		2N4416		2N4416A		Process NJ26		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 30		– 35		V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1		– 0.1	nA	V_{GS} = – 20V, V_{DS} = ØV	
			– 0.1		– 0.1	µA	V_{GS} = – 20V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$		– 6	– 2.5	– 6	V	V_{DS} = 15V, I_D = 1 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	5	15	5	15	mA	V_{DS} = 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics								
Common Source Forward Transconductance	g_{fs}	4500	7500	4500	7500	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
		4000		4000		µS	V_{DS} = 15V, V_{GS} = ØV	f = 400 MHz
Common Source Output Conductance	g_{os}		50		50	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
			75		75	µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
			100		100	µS	V_{DS} = 15V, V_{GS} = ØV	f = 400 MHz
Common Source Input Capacitance	C_{iss}		4		4	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Output Capacitance	C_{oss}		2		2	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		0.8		0.8	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Input Conductance	g_{is}		100		100	µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
			1000		1000	µS	V_{DS} = 15V, V_{GS} = ØV	f = 400 MHz
Common Source Input Susceptance	b_{is}		2500		2500	µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
			10000		10000	µS	V_{DS} = 15V, V_{GS} = ØV	f = 400 MHz
Common Source Output Susceptance	b_{os}		1000		1000	µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
			4000		4000	µS	V_{DS} = 15V, V_{GS} = ØV	f = 400 MHz
Common Source Power Gain	G_{ps}	18		18		dB	V_{DS} = 15V, I_D = 5mA	f = 100 MHz
		10		10		dB	V_{DS} = 15V, I_D = 5mA	f = 400 MHz
Noise Figure	NF		2		2	dB	V_{DS} = 15V, I_D = 5mA, R_G = 1kΩ	f = 100 MHz
			4		4	dB		f = 400 MHz

TO-72 Package
See Section G for Outline Dimensions

Surface Mount
SMP4416, SMP4416A

Pin Configuration
1 Source, 2 Drain, 3 Gate, 4 Case

Note: rf parameters guaranteed, but not 100% tested.

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2N4856, 2N4857, 2N4858, 2N4859, 2N4860, 2N4861

N-Channel Silicon Junction Field-Effect Transistor

- Choppers
- Commutators
- Analog Switches

Absolute maximum ratings at T_A = 25°C

	2N4856, 2N4857, 2N4858	2N4859, 2N4860, 2N4861
Reverse Gate Source Voltage	– 40 V	– 30 V
Reverse Gate Drain Voltage	– 40 V	– 30 V
Continuous Device Dissipation	1.8 W	1.8 W
Power Derating	10 mW/°C	10 mW/°C
Continuous Forward Gate Current	50 mA	50 mA

At 25°C free air temperature: Static Electrical Characteristics		2N4856 2N4859		2N4857 2N4860		2N4858 2N4861		Process NJ132		
		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage **2N4856, 2N4857, 2N4858**	$V_{(BR)GSS}$		– 40		– 40		– 40	V	I_G = – 1 µA, V_{DS} = ØV	
2N4859, 2N4860, 2N4861			– 30		– 30		– 30	V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current **2N4856, 2N4857, 2N4858**	I_{GSS}		– 250		– 250		– 250	pA	V_{GS} = – 20V, V_{DS} = ØV	
			– 500		– 500		– 500	nA	V_{GS} = – 20V, V_{DS} = ØV	T_A = 150°C
Gate Reverse Current **2N4859, 2N4860, 2N4861**	I_{GSS}		– 250		– 250		– 250	pA	V_{GS} = – 15V, V_{DS} = ØV	
			– 500		– 500		– 500	nA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 4	– 10	– 2	– 6	– 0.8	– 4	V	V_{DS} = 15V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	50		20	100	8	80	mA	V_{DS} = 15V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$		250		250		250	pA	V_{DS} = 15V, V_{GS} = – 10V	
			500		500		500	nA	V_{DS} = 15V, V_{GS} = – 10V	T_A = 150°C
Drain Source ON Voltage	$V_{DS(ON)}$		0.75 (20)		0.5 (10)		0.5 (5)	V (mA)	V_{GS} = ØV, I_D = ( )	
Dynamic Electrical Characteristics										
Common Source ON Resistance	$r_{ds(on)}$		25		40		60	Ω	V_{GS} = ØV, I_D = Ø A	f = 1 kHz
Common Source Input Capacitance	C_{iss}		18		18		18	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		8		8		8	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Switching Characteristics										
Turn ON Delay Time	$t_{d(on)}$		6 (20) [–10]		6 (10) [– 6]		10 (5) [– 4]	ns (mA) [V]	V_{DD} = 10V, V_{GS} = ØV $I_{D(ON)}$ = ( ) $V_{GS(OFF)}$ = [ ] **(2N4856, 2N4859)** R_L = 465Ω **(2N4857, 2N4860)** R_L = 953Ω **(2N4858, 2N4861)** R_L = 1910Ω	
Rise Time	t_r		3 (20) [–10]		4 (10) [– 6]		10 (5) [– 4]	ns (mA) [V]		
Turn OFF Delay Time	$t_{d(off)}$		25 (20) [–10]		50 (10) [– 6]		100 (5) [– 4]	ns (mA) [V]		

TO-18 Package
See Section G for Outline Dimensions

Pin Configuration
1 Source, 2 Drain, 3 Gate &Case

Surface Mount
SMP4856, SMP4857, SMP4858, SMP4859, SMP4860, SMP4861

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2N4856A, 2N4857A, 2N4858A, 2N4859A, 2N4860A, 2N4861A

N-Channel Silicon Junction Field-Effect Transistor

- Choppers
- Commutators
- Analog Switches

Absolute maximum ratings at T_A = 25°C

	2N4856A, 2N4857A, 2N4858A	2N4859A, 2N4860A, 2N4861A
Reverse Gate Source Voltage	– 40 V	– 30 V
Reverse Gate Drain Voltage	– 40 V	– 30 V
Continuous Device Dissipation	1.8 W	1.8 W
Continuous Forward Gate Current	50 mA	50 mA
Power Derating	10 mA/°C	10 mA/°C

At 25°C free air temperature:		2N4856A 2N4859A		2N4857A 2N4860A		2N4858A 2N4861A		Process NJ132		
Static Electrical Characteristics		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage **2N4856A, 2N4857A, 2N4858A**	$V_{(BR)GSS}$		– 40		– 40		– 40	V	I_G = – 1 µA, V_{DS} = ØV	
Gate Source Breakdown Voltage **2N4859A, 2N4860A, 2N4861A**	$V_{(BR)GSS}$		– 30		– 30		– 30	V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current **2N4856A, 2N4857A, 2N4858A**	I_{GSS}		– 250		– 250		– 250	pA	V_{GS} = – 20V, V_{DS} = ØV	
			– 500		– 500		– 500	nA	V_{GS} = – 20V, V_{DS} = ØV	T_A = 150°C
Gate Reverse Current **2N4859A, 2N4860A, 2N4861A**	I_{GSS}		– 250		– 250		– 250	pA	V_{GS} = – 15V, V_{DS} = ØV	
			– 500		– 500		– 500	nA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 4	– 10	– 2	– 6	– 0.8	– 4	V	V_{DS} = 15V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	50		20	100	8	80	mA	V_{DS} = 15V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$		250		250		250	pA	V_{DS} = 15V, V_{GS} = – 10V	
			500		500		500	nA	V_{DS} = 15V, V_{GS} = – 10V	T_A = 150°C
Drain Source ON Voltage	$V_{DS(ON)}$		0.75 (20)		0.5 (10)		0.5 (5)	V (mA)	V_{GS} = ØV, I_D = ( )	
Dynamic Electrical Characteristics										
Common Source ON Resistance	$r_{ds(on)}$		25		40		60	Ω	V_{GS} = ØV, I_D = Ø A	f = 1 kHz
Common Source Input Capacitance	C_{iss}		10		10		10	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		4		3.5		3.5	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Switching Characteristics										
Turn ON Delay Time	$t_{d(on)}$		5 (20) [–10]		6 (10) [– 6]		8 (5) [– 4]	ns (mA) [V]	V_{DD} = 10V, V_{GS} = ØV $I_{D(ON)}$ = ( ) $V_{GS(OFF)}$ = [ ] **(2N4856A, 2N4859A)** R_L = 464Ω **(2N4857A, 2N4860A)** R_L = 953Ω **(2N4858A, 2N486A1)** R_L = 1910Ω	
Rise Time	t_r		3 (20) [–10]		4 (10) [– 6]		8 (5) [– 4]	ns (mA) [V]		
Turn OFF Delay Time	$t_{d(off)}$		25 (20) [–10]		40 (10) [– 6]		80 (5) [– 4]	ns (mA) [V]		

TO-18 Package
See Section G for Outline Dimensions

Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

Surface Mount
SMP4856A, SMP4857A, SMP4858A, SMP4859A, SMP4860A, SMP4861A

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2N4867, 2N4867A, 2N4868, 2N4868A, 2N4869, 2N4869A

N-Channel Silicon Junction Field-Effect Transistor

- **Audio Amplifiers**

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 40 V
Gate Current	50 mA
Continuous Device Power Dissipation	300mW
Power Derating	1.7 mW/°C
Storage Temperature Range	– 65°C to + 200°C

At 25°C free air temperature: Static Electrical Characteristics		2N4867 2N4867A		2N4868 2N4868A		2N4869 2N4869A		Process NJ16		
		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 40		– 40		– 40		V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.25		– 0.25		– 0.25	nA	V_{GS} = – 30V, V_{DS} = ØV	
			– 0.25		– 0.25		– 0.25	µA	V_{GS} = – 30V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.7	– 2	– 1	– 3	– 1.8	– 5	V	V_{DS} = 20V, I_D = 1 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	0.4	1.2	1	3	2.5	7.5	mA	V_{DS} = 20V, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Common Source Forward Transconductance	g_{fs}	700	2000	1000	3000	1300	4000	µS	V_{DS} = 20V, V_{GS} = ØV	f = 1 kHz
Common Source Output Conductance	g_{os}		1.5		4		10	µS	V_{DS} = 20V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		25		25		25	pF	V_{DS} = 20V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		5		5		5	pF	V_{DS} = 20V, V_{GS} = ØV	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		20		20		20	nV/√HZ	V_{DS} = 10V, V_{GS} = ØV	f = 10 Hz
			10		10		10	nV/√HZ	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Noise Figure	NF		1		1		1	dB	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
									(2N4867, 68, 69) R_G = 20 kΩ **(2N4867A, 68A, 69A)** R_G = 5 kΩ	

TO-72 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate, 4 Case

Surface Mount
SMP4867, SMP4867A, SMP4868, SMP4868A, SMP4869, SMP4869A

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2N5020, 2N5021

P-Channel Silicon Junction Field-Effect Transistor

- Analog Switches

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 50 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	500 mW
Power Derating	4 mW/°C
Storage Temperature Range	– 65°C to + 200°C

At 25°C free air temperature:		2N5020		2N5021		Process PJ32		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GDO}$	25		25		V	I_G = 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		1		1	nA	V_{GS} = 15 V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	0.3	1.5	0.5	2.5	V	V_{DS} = – 15 V, I_D = 1 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	– 0.3	– 1.2	– 1	– 3.5	mA	V_{DS} = – 15 V, V_{GS} = ØV	
Dynamic Electrical Characteristics								
Common Source Forward Transconductance	g_{fs}	1	3.5	1.5	6	mS	V_{DS} = – 15 V, V_{GS} = ØV	
Common Source Output Conductance	g_{os}		20		20	µS	V_{DS} = – 15 V, V_{GS} = ØV	
Common Source Input Capacitance	C_{iss}		25		25	pF	V_{DS} = – 15 V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		7		7	pF	V_{DS} = – 15 V, V_{GS} = ØV	f = 1 MHz

TO-18 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source 1, 2 Gate & Case, 3 Drain

Surface Mount
SMP5020, SMP5021

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2N5114, 2N5115, 2N5116

P-Channel Silicon Junction Field-Effect Transistor

- Analog Switches

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 40 V
Gate Current	50 mA
Continuous Device Power Dissipation	500mW
Power Derating	3 mW/°C
Storage Temperature Range	– 65°C to + 200°C

At 25°C free air temperature: Static Electrical Characteristics		2N5114		2N5115		2N5116		Process PJ99		
		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	30		30		30		V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		500		500		500	pA	V_{GS} = 20V, V_{DS} = ØV	
			1		1		1	µA	V_{GS} = 20V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	5	10	3	6	1	4	V	V_{DS} = – 15V, I_G = – 1 nA	
Gate Source Forward Voltage	$V_{GS(F)}$		– 1		– 1		– 1	V	V_{DS} = ØV, I_G = – 1 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	– 30	– 90					mA	V_{GS} = ØV, V_{DS} = – 18V	
				– 15	– 60	– 5	– 25	mA	V_{GS} = ØV, V_{DS} = – 15V	
Drain Cutoff Current	$I_{D(OFF)}$		– 500					pA	V_{DS} = – 15V, V_{GS} = 12V	
			– 1					µA	V_{DS} = – 15V, V_{GS} = 12V	T_A = 150°C
					– 500			pA	V_{DS} = – 15V, V_{GS} = 7V	
					– 1			µA	V_{DS} = – 15V, V_{GS} = 7V	T_A = 150°C
							– 500	pA	V_{DS} = – 15V, V_{GS} = 5V	
							– 1	µA	V_{DS} = – 15V, V_{GS} = 5V	T_A = 150°C
Drain Source ON Voltage	$V_{DS(ON)}$		– 1.3					V	V_{GS} = ØV, I_D = – 15 mA	
					– 0.8			V	V_{GS} = ØV, I_D = – 7 mA	
							– 0.6	V	V_{GS} = ØV, I_D = – 3 mA	
Static Drain Source ON Resistance	$r_{DS(ON)}$		75		100		150	Ω	V_{GS} = ØV, I_D = – 1 mA	
Dynamic Electrical Characteristics										
Drain Source ON Resistance	$r_{ds(on)}$		75		100		150	Ω	V_{GS} = ØV, I_D = ØA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		25		25		27	pF	V_{DS} =– 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		7					pF	V_{DS} = ØV, V_{GS} = 12V	f = 1 MHz
					7			pF	V_{DS} = ØV, V_{GS} = 7 V	f = 1 MHz
							7	pF	V_{DS} = ØV, V_{GS} = 5V	f = 1 MHz

Switching Characteristics									2N5114	2N5115	2N5116	
Turn ON Delay Time	$t_{d(on)}$		6		10		25	ns	V_{DD}	– 10	– 6	– 6 V
Rise Time	t_r		10		20		35	ns	V_{GG}	20	12	8 V
Turn OFF Delay Time	$t_{d(off)}$		6		8		20	ns	R_L	130	910	2000 Ω
Fall Time	t_f		15		30		60	ns	R_G	100	220	390 Ω
									$I_{D(ON)}$	– 15	– 7	– 3 mA

TO-18 Package

See Section G for Outline Dimensions

Pin Configuration

1 Source 1, 2 Gate & Case, 3 Drain

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2N5397, 2N5398

N-Channel Silicon Junction Field-Effect Transistor

- Low-Noise
- High Power Gain
- High Transconductance
- Mixers
- Oscillators
- VHF Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 25 V
Drain Source Voltage	25 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	1.7 mW/°C

At 25°C free air temperature:		2N5397		2N5398		Process NJ26L		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25		– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Source Forward Voltage	$V_{GS(F)}$		1		1	V	I_G = 1 mA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1		– 0.1	nA	V_{GS} = – 15V, V_{DS} = ØV	
			– 0.1		– 0.1	µA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1	– 6	– 1	– 6	V	V_{DS} = 10V, I_D = 1 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	10	30	5	40	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics								
Common Source Forward Transconductance	g_{fs}	5.5	9	5	10	mS	V_{DG} = 10V, I_D = 10 mA	f = 450 MHz
Common Source Forward Transfer Admittance	$\lvert Y_{fs} \rvert$	6	10	5.5	10	mS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Common Source Output Conductance	$\lvert g_{os} \rvert$		0.4		0.5	mS	V_{DG} = 10V, I_D = 10 mA	f = 450 MHz
Common Source Input Admittance	$\lvert Y_{os} \rvert$		0.2		0.4	mS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Common Source Input Conductance	g_{is}		2		3	mS	V_{DG} = 10V, I_D = 10 mA	f = 450 MHz
Common Source Input Capacitance	C_{iss}		5		5.5	pF	V_{DG} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Reverse Transfer Capacitance	C_{rss}		1.2		1.3	pF	V_{DG} = 15V, V_{GS} = ØV	f = 1 kHz

TO-72 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate, 4 Case

Surface Mount
SMP5397, SMP5398

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2N5460, 2N5461, 2N5462

P-Channel Silicon Junction Field-Effect Transistor

- Audio Amplifiers
- General Purpose Amplifiers

Absolute maximum ratings at 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	40 V
Continuous Forward Gate Current	– 10 mA
Continuous Device Power Dissipation	310 mW
Power Derating	2.8 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		2N5460		2N5461		2N5462		Process PJ32		
		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	40		40		40		V	I_G = 10µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		5		5		5	nA	V_{GS} = 20V, V_{DS} = ØV	
			1		1		1	µA	V_{GS} = 20V, V_{DS} = ØV	T_A = 100°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	0.75	6	1	7.5	1.8	9	V	V_{DS} = – 15V, I_D = – 1 µA	
Gate Source Voltage	V_{GS}	0.8	4.5					V	V_{DS} = – 15V, I_D = – 100 µA	
				0.8	4.5			V	V_{DS} = – 15V, I_D = – 200 µA	
						1.5	6	V	V_{DS} = – 15V, I_D = – 400 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	– 1	– 5	– 2	– 9	– 4	– 16	mA	V_{DS} = – 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Drain Source ON Resistance	$r_{ds(on)}$		2		0.8		0.4	kΩ	V_{GS} = ØV, I_D = Ø A	f = 1 kHz
Common Source Forward Transadmittance	$\lvert Y_{fs} \rvert$	1	4	1.5	5	2	6	mS	V_{DS} = – 15V, V_{GS} = Ø V	f = 1 kHz
Common Source Output Admittance	$\lvert Y_{os} \rvert$		75		75		75	µS	V_{DS} = – 15V, V_{GS} = Ø V	f = 1 kHz
Common Source Input Capacitance	C_{iss}		7		7		7	pF	V_{DS} = – 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		2		2		2	pF	V_{DS} = – 15V, V_{GS} = ØV	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		2.5		2.5		2.5	dB	V_{DS} = – 15V, V_{GS} = ØV	f = 100 Hz, BW = 1 Hz
Noise Figure	NF		115		115		115	nV/√Hz	V_{DS} = – 15V, V_{GS} = ØV, R_G = 1MΩ	f = 100 Hz

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

Surface Mount
SMP5460, SMP5461, SMP5462

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2N5484, 2N5485, 2N5486

N-Channel Silicon Junction Field-Effect Transistor

- VHF/UHF Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source Voltage	– 25 V
Reverse Gate Drain Voltage	– 25 V
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		2N5484		2N5485		2N5486		Process NJ26		
		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25		– 25		– 25		V	I_G = 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 1		– 1		– 1	nA	V_{GS} = – 20V, V_{DS} = ØV	
			– 0.2		– 0.2		– 0.2	µA	V_{GS} = – 20V, V_{DS} = ØV	T_A = 100°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.3	– 3	– 0.5	– 4	– 2	– 6	V	V_{DS} = 15V, I_D = 10 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	1	5	4	10	8	20	mA	V_{DS} = 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Forward Transconductance	$R_{e(Yfs)}$	2500						µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
				3000		3500		µS	V_{DS} = 15V, V_{GS} = ØV	f = 400 MHz
Common Source Forward Transadmittance	Y_{fs}	3000	6000	3500	7000	4000	8000	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Input Admittance	$R_{e(Yis)}$		100					µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
					1000		1000	µS	V_{DS} = 15V, V_{GS} = ØV	f = 400 MHz
Output Conductance	$R_{e(Yos)}$		75					µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
					100		100	µS	V_{DS} = 15V, V_{GS} = ØV	f = 400 MHz
Common Source Output Admittance	Y_{os}		50		60		75	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Input Capacitance	C_{iss}		5		5		5	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		1		1		1	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Output Capacitance	C_{oss}		2		2		2	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

Surface Mount
SMP5484, SMP5485, SMP5486

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2N5911, 2N5912

Dual N-Channel Silicon Junction Field-Effect Transistor

- **Wideband Differential Amplifiers**

Absolute maximum ratings at T_A = 25°C

Continuous Forward Gate Current	50 mA
Total Device Power Dissipation	500 mW
Power Derating	4 mW°C
Storage Temperature Range	–65°C to + 200°C

At 25°C free air temperature:		2N5911		2N5912		Process NJ30L or NJ36D		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25		– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 100		– 100	pA	V_{GS} = – 15V, V_{DS} = ØV	
			– 250		– 250	nA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 150°C
Gate Operating Current	I_G		– 100		– 100	pA	V_{DG} = 10V, I_D = 5 mA	
			– 100		– 100	nA	V_{DG} = 10V, I_D = 5 mA	T_A = 125°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1	– 5	– 1	– 5	V	V_{DS} = 10V, I_D = 1 nA	
Gate Source Voltage	V_{GS}	– 0.3	– 4	– 0.3	– 4	V	V_{DS} = 10V, I_D = 5 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	7	40	7	40	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics								
Common Source Forward Transconductance	g_{fs}	5000	10000	5000	10000	µS	V_{DG} = 10V, I_D = 5 mA	f = 1 kHz
		5000	10000	5000	10000	µS	V_{DG} = 10V, I_D = 5 mA	f = 100 MHz
Common Source Output Conductance	g_{os}		100		100	µS	V_{DG} = 10V, I_D = 5 mA	f = 1 kHz
			150		150	µS	V_{DG} = 10V, I_D = 5 mA	f = 100 MHz
Common Source Input Capacitance	C_{iss}		5		5	pF	V_{DG} = 10V, I_D = 5 mA	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		1.2		1.2	pF	V_{DG} = 10V, I_D = 5 mA	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		20		20	nV/√Hz	V_{DG} = 10V, I_D = 5 mA	f = 10 kHz
Noise Figure	NF		1		1	dB	V_{DG} = 10V, I_D = 5 mA R_G = 100 KΩ	f = 10 kHz
Differential Gate Current	$I_{G1} - I_{G2}$		20		20	nA	V_{DG} = 10V, I_D = 5 mA	T_A = 125°C
Saturation Drain Current Ratio	I_{DSS1} / I_{DSS2}	0.95	1	0.95	1		V_{DG} = 20V, V_{GS} = ØV	
Differential Gate Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$		10		15	mV	V_{DG} = 10V, I_D = 5 mA	
Gate Source Voltage Differential Drift	$\frac{\Delta V_{GS1} - V_{GS2}}{\Delta T}$		20		40	mV	V_{DG} = 10V, I_D = 5 mA	T_A = 25°C, T_B = 125°C
			20		40	mV	V_{DG} = 10V, I_D = 5 mA	T_A = – 55°C, T_B = 25°C
Transconductance Ratio	g_{fs1} / g_{fs2}	0.9	1	0.85	1		V_{DG} = 10V, I_D = 5 mA	f = 1 kHz

SOIC-8 Package
See Section G for Outline Dimensions

Pin Configuration
1 Source 1, 2 Drain 1, 3 Gate 1, 4 N/C,
5 Source 2, 6 Drain 2, 7 Gate 2, 8 Omitted

TO-78 Package
See Section G for Outline Dimensions

Pin Configuration
1 Source 1, 2 Drain 1, 3 Gate 1,
4 Case, 5 Source 2, 6 Drain 2,
7 Gate 2, 8 Omitted

Surface Mount
SMP5911, SMP5912

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2N6449, 2N6450

N-Channel Silicon Junction Field-Effect Transistor

- **High Voltage**

Absolute maximum ratings at T_A = 25°C

	2N6449	2N6450
Reverse Gate Source Voltage	– 300 V	– 200 V
Reverse Gate Drain Voltage	– 300 V	– 200 V
Continuous Forward Gate Current	10 mA	10 mA
Continuous Device Power Dissipation	800 mW	800 mW
Power Derating	6.4 mW/°C	6.4 mW/°C

At 25°C free air temperature:		2N6449		2N6450		Process NJ42		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 300		– 200		V	I_G = – 10 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 100			nA	V_{GS} = – 150V, V_{DS} = ØV	
					– 100	nA	V_{GS} = – 100V, V_{DS} = ØV	
			– 100			µA	V_{GS} = – 150V, V_{DS} = ØV	T_A = 150°C
					– 100	µA	V_{GS} = – 100V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 2	– 15	– 2	– 15	V	V_{DS} = 30V, I_D = 4 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	2	10	2	10	mA	V_{DS} = 30V, V_{GS} = ØV	
Dynamic Electrical Characteristics								
Common Source Forward Transfer Admittance	Y_{fs}	0.5	3	0.5	3	mS	V_{DS} = 30V, V_{GS} = ØV	f = 1 kHz
Common Source Output Conductance	Y_{os}		100		100	µS	V_{DS} = 30V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		20		20	pF	V_{DS} = 30V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		2.5		2.5	pF	V_{DS} = 30V, V_{GS} = ØV	f = 1 MHz

TO-39 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

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2N6451, 2N6452

N-Channel Silicon Junction Field-Effect Transistor

- Audio Amplifiers
- Low-Noise, High Gain Amplifiers
- Low-Noise Preamplifiers

Absolute maximum ratings at T_A = 25°C

	2N6451	2N6452
Reverse Gate Source Voltage	– 20 V	– 25 V
Reverse Gate Drain Voltage	– 20 V	– 25 V
Continuous Forward Gate Current	10 mA	10 mA
Continuous Device Power Dissipation	360 mW	360 mW
Power Derating	2.88 mW/°C	2.88 mW/°C

At 25°C free air temperature:		2N6451		2N6452		Process NJ132L		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20		– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1			nA	V_{GS} = – 10V, V_{DS} = ØV	
					– 0.5	nA	V_{GS} = – 15V, V_{DS} = ØV	
			– 0.2			µA	V_{GS} = – 10V, V_{DS} = ØV	T_A = 125°C
					– 1	µA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 125°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.5	– 3.5	– 0.5	– 3.5	V	V_{DS} = 10V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	5	20	5	20	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics								
Common Source Forward Transmittance	$\lvert Y_{fs} \rvert$	15	30	15	30	mS	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
						mS	V_{DS} = 10V, I_D = 15 mA	f = 1 kHz
Common Source Output Conductance	$\lvert Y_{os} \rvert$		50		50	µS	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
						µS	V_{DS} = 10V, I_D = 15 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		25		25	pF	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
						pF	V_{DS} = 10V, I_D = 15 mA	f = 1 kHz
Common Source Reverse Transfer Capacitance	C_{rss}		5		5	pF	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
						pF	V_{DS} = 10V, I_D = 15 mA	f = 1 kHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		5		10	nV/√Hz	V_{DS} = 10V, I_D = 5 mA	f = 10 kHz
			3		8	nV/√Hz	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
Noise Figure	NF		1.5		2.5	dB	V_{DS} = 10V, I_D = 5 mA R_G = 10 kΩ	f = 10 Hz

TO-72 Package

Dimensions in Inches (mm)

Pin Configuration

1 Source, 2 Drain, 3 Gate, 4 Case

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2N6453, 2N6454

N-Channel Silicon Junction Field-Effect Transistor

- Audio Amplifiers
- Low-Noise, High Gain Amplifiers
- Low-Noise Preamplifiers

Absolute maximum ratings at T_A = 25°C

	2N6453	2N6454
Reverse Gate Source Voltage	– 20 V	– 25 V
Reverse Gate Drain Voltage	– 20 V	– 25 V
Continuous Forward Gate Current	10 mA	10 mA
Continuous Device Power Dissipation	360 mW	360 mW
Power Derating	2.88 mW/°C	2.88 mW/°C

At 25°C free air temperature:		2N6453		2N6454		Process NJ132L		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20		– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1			nA	V_{GS} = – 10V, V_{DS} = ØV	
					– 0.5	nA	V_{GS} = – 15V, V_{DS} = ØV	
			– 0.2			µA	V_{GS} = – 10V, V_{DS} = ØV	T_A = 125°C
					– 1	µA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 125°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.75	– 5	– 0.75	– 5	V	V_{DS} = 10V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	15	50	15	50	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics								
Common Source Forward Transmittance	$\lvert Y_{fs} \rvert$					mS	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
		20	40	20	40	mS	V_{DS} = 10V, I_D = 15 mA	f = 1 kHz
Common Source Output Conductance	$\lvert Y_{os} \rvert$					µS	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
			100		100	µS	V_{DS} = 10V, I_D = 15 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}					pF	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
			25		25	pF	V_{DS} = 10V, I_D = 15 mA	f = 1 kHz
Common Source Reverse Transfer Capacitance	C_{rss}					pF	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
			5		5	pF	V_{DS} = 10V, I_D = 15 mA	f = 1 kHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		5		10	nV/√Hz	V_{DS} = 10V, I_D = 5 mA	f = 10 kHz
			3		8	nV/√Hz	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
Noise Figure	NF		1.5		2.5	dB	V_{DS} = 10V, I_D = 5 mA R_G = 10 kΩ	f = 10 Hz

TO-72 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate, 4 Case

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2N6550

N-Channel Silicon Junction Field-Effect Transistor

- **Low-Noise, High Gain Amplifier**

Absolute maximum ratings at T_A =25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 20 V
Continuious Forward Gate Current	50 mA
Continuous Device Power Dissipation	400 mW
Power Derating	2.3 mW/°C
Junction Temperature (Operating & Storage)	– 65°C to +200°C

At 25°C free air temperature:		2N6550			Process NJ450L		
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20			V	I_G = 10 µA, V_{DS} = ØV	
Gate Leakage Current	I_{GSS}			– 3	nA	V_{GS} = – 10V, V_{DS} = ØV	
				– 0.1	µA	V_{GS} = – 10V, V_{DS} = ØV	T_A = 85°C
Zero Gate Voltage Drain Current (Pulsed)	I_{DSS}	10	100	250	mA	V_{DS} = 10V, V_{GS} = Ø V	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.3		– 3	V	V_{DS} = 10V, I_D = 0.1 mA	
Dynamic Electrical Characteristics							
Transconductance	g_{fs}	25		150	mS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Common Source Output Conductance	$\|Y_{os}\|$			150	µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		30	35	pF	V_{DS} = 10V, I_D = 10 mA	f = 140 kHz
Common Source Reverse Transfer Capacitance	C_{rss}		10	20	pF	V_{DS} = 10V, V_{DS} = ØV	f = 140 kHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		1.4	2	nV/√Hz	V_{DS} = 5V, I_D = 10 mA	f = 1 kHz
			6	10	nV/√Hz	V_{DS} = 5V, I_D = 10 mA	f = 10 Hz
	$\bar{e}_N$ Total		0.4	0.6	µVrms	V_{DS} = 5V, I_D = 10 mA	f = 10 kHz to 20 kHz
Equivalent Open Circuit Input Noise Current	$\bar{i}_N$		0.1		pA/√Hz	R_S < 100 KΩ	f = 1 kHz

TO-46 Package

Dimensions in Inches (mm)

Pin Configuration

1 Drain, 2 Source, 3 Gate & Case

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IF140, IF140A

N-Channel Silicon Junction Field-Effect Transistor

- Low-Noise, High Gain Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 20 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	375 mW
Power Derating	3 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IF140		IF140A		Process NJ14AL		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20		– 20		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1		– 0.1	nA	V_{GS} = – 15V, V_{DS} = ØV	
			– 0.2		– 0.2	nA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$		– 6		– 6	V	V_{DS} = 15V, I_D = 5 nA	
Gate Source Voltage	V_{GS}		– 5	– 2.5	– 6	V	V_{DS} = 15V, I_D = 50 µA	
Gate Source Forward Voltage	$V_{GS(F)}$		1		1	V	V_{DS} = Ø, I_G = 1 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	5	15	5	15	mA	V_{DS} = 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics								
Common Source Forward Transmittance	Y_{fs}	4.5		4.5		mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Output Conductance	Y_{os}		0.05		0.05	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		3		3	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		0.6		0.6	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
		Typ		**Typ**				
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$	4		4		nV/√Hz	V_{DS} = 12V, V_{GS} = ØV	f = 10 Hz

TO-72 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate, 4 Case

InterFET Corporation
1000 N. Shiloh Road, Garland, TX 75042
(972) 487-1287 FAX (972) 276-3375
www.interfet.com

IF142

N-Channel Silicon Junction Field-Effect Transistor

- **Low-Noise, High Gain Amplifier**

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 20 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	375 mW
Power Derating	3 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IF142		Process NJ14AL		
Static Electrical Characteristics		**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1	nA	V_{GS} = – 15V, V_{DS} = ØV	
			– 0.2	nA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$		– 6	V	V_{DS} = 15V, I_D = 5 nA	
Gate Source Voltage	V_{GS}		– 5	V	V_{DS} = 15V, I_D = 50 µA	
Gate Source Forward Voltage	$V_{GS(F)}$		1	V	V_{DS} = Ø, I_G = 1 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	5	15	mA	V_{DS} = 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics						
Common Source Forward Transmittance	Y_{fs}	3.5		mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Output Conductance	Y_{os}		0.05	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		3	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		0.6	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
		Typ				
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$	4		nV/√Hz	V_{DS} = 12V, V_{GS} = ØV	f = 10 Hz

TO-236AB Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

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IF1320

N-Channel Silicon Junction Field-Effect Transistor

- Low-Noise, High Gain Amplifier

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 20 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	225 mW
Power Derating	1.8 mW°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IF1320		Process NJ132L		
Static Electrical Characteristics		**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1	nA	V_{DS} = ØV, V_{GS} = – 10V	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.35	– 1.5	V	V_{DS} = 10V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	5	20	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics						
Common Source Forward Transconductance	g_{fs}	15		mS	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		20	pF	V_{DS} = 10V, I_D = 5 mA	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		5	pF	V_{DS} = 10V, I_D = 5 mA	f = 1 MHz
		Typ				
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$	2.5		nV/√Hz	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz

TO-236AB Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

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IF1330

N-Channel Silicon Junction Field-Effect Transistor

- **Low-Noise, High Gain Amplifier**

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 20 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	225 mW
Power Derating	1.8 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IF1330		Process NJ132H		
Static Electrical Characteristics		**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1	nA	V_{DS} = ØV, V_{GS} = – 10V	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.35	– 1.5	V	V_{DS} = 10V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	5	20	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics						
Common Source Forward Transconductance	g_{fs}	10		mS	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		20	pF	V_{DS} = 10V, I_D = 5 mA	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		5	pF	V_{DS} = 10V, I_D = 5 mA	f = 1 MHz
		Typ				
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$	2.5		nV/√Hz	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz

TO-236AB Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

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IF1331

N-Channel Silicon Junction Field-Effect Transistor

- Low-Noise, High Gain Amplifier

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 20 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	225 mW
Power Derating	1.8 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IF1331		Process NJ132H		
Static Electrical Characteristics		**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1	nA	V_{DS} = ØV, V_{GS} = – 10V	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.35	– 1.5	V	V_{DS} = 10V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	5	20	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics						
Common Source Forward Transconductance	g_{fs}	10		mS	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		20	pF	V_{DS} = 10V, I_D = 5 mA	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		5	pF	V_{DS} = 10V, I_D = 5 mA	f = 1 MHz
		Typ				
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$	2.5		nV/√Hz	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz

TO-72 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate, 4 Case

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IF1801

N-Channel Silicon Junction Field-Effect Transistor

- **Low-Noise, High Gain Amplifier**

Absolute maximum ratings = T_A at 25°C

Reverse Gate Source Voltage & Gate Drain Voltage	– 20 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	2 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IF1801		Process NJ1800DL		
Static Electrical Characteristics		**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1	nA	V_{GS} = – 10V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.35	– 2	V	V_{DS} = 10V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	30		mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics						
Common Source Forward Transconductance	g_{fs}	50		mS	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		100	pF	V_{DS} = 10V, I_D = 5 mA	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		50	pF	V_{DS} = 10V, I_D = 5 mA	f = 1 MHz
		Typ				
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$	0.5		nV/√Hz	V_{DG} = 4V, I_D = 5 mA	f = 1 kHz

TO-52 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

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IF3601

N-Channel Silicon Junction Field-Effect Transistor

- Low-Noise, High Gain Amplifier

Absolute maximum ratings = T_A at 25°C

Reverse Gate Source Voltage & Gate Drain Voltage	– 20 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	2 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature: Static Electrical Characteristics		IF3601 Min	IF3601 Max	Process NJ3600L Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1	nA	V_{GS} = – 10V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.35	– 2	V	V_{DS} = 10V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	30		mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics		**Typ**				
Common Source Forward Transconductance	g_{fs}	750		mS	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}	300		pF	V_{DS} = ØV, V_{GS} = – 4V	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}	200		pF	V_{DS} = ØV, V_{GS} = – 4V	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$	0.3		nV/√Hz	V_{DG} = 3V, I_D = 5 mA	f = 100 Hz

TO-39 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

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IF3602

Dual N-Channel Silicon Junction Field-Effect Transistor

- **Low-Noise, High Gain Amplifier**

Absolute maximum ratings = T_A at 25°C

Reverse Gate Source Voltage & Gate Drain Voltage	– 20 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	4 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IF3602		Process NJ3600L		
Static Electrical Characteristics		**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.5	nA	V_{GS} = – 10V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.35	– 3	V	V_{DS} = 10V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	30		mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics		**Typ**				
Common Source Forward Transconductance	g_{fs}	750		mS	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}	300		pF	V_{DS} = ØV, V_{GS} = – 4V	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}	200		pF	V_{DS} = ØV, V_{GS} = – 4V	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$	0.3		nV/√Hz	V_{DG} = 3V, I_D = 5 mA	f = 100 Hz
		Max				
Differential Gate Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	100		mV	V_{DS} = 10V, V_{GS} = ØV	

TO-78 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate, 4 Omitted,
5 Source, 6 Drain, 7 Gate, 8 Omitted

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IF4500

N-Channel Silicon Junction Field-Effect Transistor

- Low-Noise, High Gain Amplifier

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 20 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	225 mW
Power Derating	1.8 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IF4500		Process NJ450L		
Static Electrical Characteristics		**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1	nA	V_{GS} = – 30V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.35	– 1.5	V	V_{DS} = 15V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	5		mA	V_{DS} = 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics						
Common Source Forward Transconductance	g_{fs}	15		mS	V_{DS} = 15V, I_D = 5 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		35	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		8	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
		Typ				
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$	1.5		nV/√Hz	V_{DS} = 12V, V_{GS} = ØV	f = 1 kHz

TO-236AB Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

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IF4501

N-Channel Silicon Junction Field-Effect Transistor

- **Low-Noise, High Gain Amplifier**

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 20 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	2.4 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IF4501		Process NJ450L		
Static Electrical Characteristics		**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1	nA	V_{GS} = – 10V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.35	– 1.5	V	V_{DS} = 10V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	5		mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics						
Common Source Forward Transconductance	g_{fs}	15		mS	V_{DS} = 15V, I_D = 5 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		35	pF	V_{DS} = 15V, I_D = 5 mA	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		9	pF	V_{DS} = 15V, I_D = 5 mA	f = 1 MHz
		Typ				
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$	1.5		nV/√Hz	V_{DG} = 12V, I_D = 5 mA	f = 1 kHz

TO-72 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate, 4 Case

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IF4510

N-Channel Silicon Junction Field-Effect Transistor

- Low-Noise, High Gain Amplifier

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 20 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	1.8 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IF4510		Process NJ450H		
Static Electrical Characteristics		**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1	nA	V_{GS} = – 15V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.35	– 1.5	V	V_{DS} = 15V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	5		mA	V_{DS} = 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics						
Common Source Forward Transconductance	g_{fs}	15		mS	V_{DS} = 15V, I_D = 5 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		35	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		8	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
		Typ				
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$	1.5		nV/√Hz	V_{DG} = 12V, V_{GS} = ØV	f = 1 kHz

TO-236AB Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

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IF4511

N-Channel Silicon Junction Field-Effect Transistor

- **Audio Amplifier**

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 20 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	1.8 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IF4511		Process NJ450H		
Static Electrical Characteristics		**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1	nA	V_{GS} = – 30V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.35	– 1.5	V	V_{DS} = 15V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	5		mA	V_{DS} = 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics						
Common Source Forward Transconductance	g_{fs}	15		mS	V_{DS} = 15V, I_D = 5 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		35	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		8	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
		Typ				
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$	1.5		nV/√Hz	V_{DG} = 12V, V_{GS} = ØV	f = 1 kHz

TO-72 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate, 4 Case

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IF9030

N-Channel Silicon Junction Field-Effect Transistor

- Low-Noise, High Gain Amplifier

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 20 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	2.4 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IF9030		Process NJ903L		
Static Electrical Characteristics		**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1	nA	V_{GS} = – 10V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.35	– 2	V	V_{DS} = 10V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	30	300	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics						
Common Source Forward Transconductance	g_{fs}	80		mS	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		60	pF	V_{DS} = 10V, I_D = 5 mA	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		20	pF	V_{DS} = 10V, I_D = 5 mA	f = 1 MHz
		Typ				
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$	0.5		nV/√Hz	V_{DG} = 4V, I_D = 5 mA	f = 1 kHz

TO-52 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

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IFN421, IFN422, IFN423

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- Very High Input Impedance Differential Amplifiers
- Electrometers

Absolute maximum ratings at T_A = 25°C

Device Dissipation (Derate 3.2 mW/°C to 50°C)	400 mW
Total Device Dissipation (Derate 6 mW/°C to 150°C)	750 mW
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IFN421, IFN422, IFN423			Process NJ01		
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 40	– 60		V	I_G = – 1 µA, V_{DS} = ØV	
Gate to Gate Breakdown Voltage	BV_{G1G2}	±40			V	I_G = – 1 µA, I_D = ØA, I_S = ØA	
Gate Reverse Current	I_{GSS}			– 1	pA	V_{GS} = – 20V, V_{DS} = ØV	
				– 1	nA	V_{GS} = – 20V, V_{DS} = ØV	T_A = +125°C
Gate Operating Current	I_G			– 0.25	pA	V_{DS} = 10V, I_D = 30 µA	
				– 250	pA	V_{DS} = 10V, I_D = 30 µA	T_A = +125°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.4		– 2	V	V_{DS} = 10V, I_D = 1 nA	
Gate Source Voltage	V_{GS}			– 1.8	V	V_{DS} = 10V, I_D = 30 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	60		1000	µA	V_{DS} = 10V, V_{GS} = Ø V	
Dynamic Electrical Characteristics							
Common Source Forward Transconductance	g_{fs}	100		1500	µS	V_{DS} = 10V, V_{GS} = Ø V	f = 1 kHz
Common Source Output Conductance	g_{os}			3	µS	V_{DS} = 10V, I_D = 30 µA	f = 1 kHz
Common Source Input Capacitance	C_{iss}			3	pF	V_{DS} = 10V, V_{GS} = Ø V	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}			1.5	pF	V_{DS} = 10V, V_{GS} = Ø V	f = 1 MHz
Equivalent Circuit Input Noise Voltage	$\bar{e}_N$		20	70	nV/√Hz	V_{DS} = 10V, I_D = 30 µA	f = 10 Hz
Noise Figure	NF			1	dB	V_{DS} = 10V, I_D = 30 µA R_G = 10 MΩ	f = 10 Hz
		Max -	**IFN421**	**IFN422**	**IFN423**		
Differential Gate Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	10	15	25	mV	V_{DG} = 10V, I_D = 30 µA	
Differential Gate Source Voltage With Temperature	$\frac{\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	10	25	40	µV/°C	V_{DG} = 10V, I_D = 30 µA	T_A = – 55°C T_B = 25°C T_C = 125°C
		Min -	**IFN421**	**IFN422**	**IFN423**		
Common Mode Rejection Ratio	CMRR	90	80	80	dB	V_{DG} = 10V to 20V, I_D = 30 µA	

TO-78 Package

See Section G for Outline Dimensions

Pin Configuration

1 Source 1, 2 Drain 1, 3 Gate 1, 4 Case,
5 Source 2, 6 Drain 2, 7 Gate 2,
8 Omitted

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IFN424, IFN425, IFN426

Dual N-Channel Silicon Junction Field-Effect Transistor

- Very High Impedance Differential Amplifiers
- Electrometers

Absolute maximum ratings at T_A = 25°C

Device Dissapation (Derate 3.2 mW/°C to 50°C)	400 mW
Total Device Dissipation (Derate 6 mW/°C to 150 °C)	750 mW
Storage Temperature Range	– 60 °C to 200 °C

At 25°C free air temperature:		IFN424, IFN425, IFN426			Process NJ01		
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 40	– 60		V	I_G = – 1 µA, V_{DS} = ØV	
Gate to Gate Breakdown Voltage	BV_{G1G2}	±40			V	I_G = – 1 µA, I_D = ØA, I_S = ØA	
Gate Reverse Current	I_{GSS}			– 3	pA	V_{GS} = – 20V, V_{DS} = ØV	
				– 3	nA	V_{GS} = – 20V, V_{DS} = ØV	T_A = +125°C
Gate Operating Current	I_G			– 0.5	pA	V_{DS} = 10V, I_D = 30 µA	
				– 500	pA	V_{DS} = 10V, I_D = 30 µA	T_A = +125°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.4		– 3	V	V_{DS} = 10V, I_D = 1 nA	
Gate Source Voltage	V_{GS}			– 2.9	V	V_{DS} = 10V, I_D = 30 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	60	1800		µA	V_{DS} = 10V, V_{GS} = Ø V	
Dynamic Electrical Characteristics							
Common Source Forward Transconductance	g_{fs}	100		1500	µS	V_{DS} = 10V, V_{GS} = Ø V	f = 1 kHz
Common Source Output Conductance	g_{os}			3	µS	V_{DS} = 10V, I_D = 30 µA	f = 1 kHz
Common Source Input Capacitance	C_{iss}			3	pF	V_{DS} = 10V, V_{GS} = Ø V	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}			1.5	pF	V_{DS} = 10V, V_{GS} = Ø V	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		20	70	nV/√Hz	V_{DS} = 10V, I_D = 30 µA	f = 10 Hz
Noise Figure	NF			1	dB	V_{DS} = 10V, I_D = 30 µA R_G = 1 MΩ	f = 10 Hz
		Max -	**IFN424**	**IFN425**	**IFN426**		
Differential Gate Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	10	15	25	mV	V_{DG} = 10V, I_D = 30 µA	
Differential Gate Source Voltage With Temperature	$\frac{\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	10	25	40	µV/°C	V_{DG} = 10V, I_D = 30 µA	T_A = – 55°C T_B = 25°C T_C = 125°C
		Min -	**IFN424**	**IFN425**	**IFN426**		
Common Mode Rejection Ratio	CMRR	90	80	80	dB	V_{DG} = 10V to 20V, I_D = 30 µA	

TO-78 Package
See Section G for Outline Dimensions

Pin Configuration
1 Source 1, 2 Drain 1, 3 Gate 1, 4 Case,
5 Source 2, 6 Drain 2, 7 Gate 2,
8 Omitted

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IFN860

Dual N-Channel Silicon Junction Field-Effect Transistor

- Low-Noise Audio Amplifier
- Equivalent to Crystalonics CD860

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 20 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	400 mW
Power Derating	2.3 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IFN860			Process NJ450L		
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20			V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Leakage Voltage	I_{GSS}			3	nA	V_{GS} = – 10V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.3		– 3	V	V_{DS} = 10V, I_D = 100 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	10			mA	V_{DS} = 10V, V_{GS} = Ø V	
Differential Gate Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$			25	mV	V_{DS} = 10V, I_D = 100 µA	
Dynamic Electrical Characteristics							
Transconductance	g_m	25	40		mS	V_{DS} = 10V, I_D = – 10 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		30	35	pF	V_{DS} = 10V, I_D = – 10 mA	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		17	20	pF	V_{DS} = 10V, I_D = – 10 mA	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$			2	nV/√Hz	V_{DG} = 3V, I_D = 10 mA	f = 1 kHz

TO-71 Package

Dimensions in Inches (mm)

Pin Configuration

1 Source, 2 Drain, 3 Gate, 5 Source, 6 Drain, 7 Gate

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IFN5114, IFN5115, IFN5116

P-Channel Silicon Junction Field-Effect Transistor

- Analog Switches

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 50 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	500 mW
Power Derating	4 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature: Static Electrical Characteristics		IFN5114		IFN5115		IFN5116		Process PJ99		
		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	30		30		30		V	I_G = – 1 mA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		2		2		2	nA	V_{GS} = 20V, V_{DS} = ØV	
			10		10		10	µA	V_{GS} = 20V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	5	10	3	6	1	4	V	V_{DS} = – 15V, I_G = – 1 nA	
Gate Source Forward Voltage	$V_{GS(F)}$		– 1		– 1		– 1	V	V_{DS} = ØV, I_G = – 1 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	– 30	– 90					mA	V_{DS} = – 15V, V_{GS} = 18V	
				– 15	– 60	– 5	– 25	mA	V_{DS} = – 15V, V_{GS} = 15V	
Drain Cutoff Current	$I_{D(OFF)}$		– 2		– 2		– 2	nA	V_{DS} = – 15V, V_{GS} = 12V	
			– 10		– 10		– 10	µA	V_{DS} = – 15V, V_{GS} = 7V	T_A = 150°C
Drain Source ON Voltage	$V_{DS(ON)}$		– 1.3					V	V_{GS} = ØV, I_D = – 15 mA	
					– 0.8			V	V_{GS} = ØV, I_D = – 7 mA	
							– 0.6	V	V_{GS} = ØV, I_D = – 3 mA	
Static Drain Source ON Resistance	$r_{DS(ON)}$		75		100		150	Ω	V_{GS} = ØV, I_D = – 1 mA	
Dynamic Electrical Characteristics										
Drain Source ON Resistance	$r_{ds(on)}$		75		100		150	Ω	V_{GS} = ØV, I_D = ØA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		25		25		27	pF	V_{DS} =– 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		7					pF	V_{DS} = – 10V, V_{GS} = 12V	f = 1 MHz
					7			pF	V_{DS} = – 10V, V_{GS} = 7V	f = 1 MHz
							7	pF	V_{DS} = – 10V, V_{GS} = 5V	f = 1 MHz

Switching Characteristics										IFN5114	IFN5115	IFN5116	
Turn ON Delay Time	$t_{d(on)}$		6		10		25	ns	V_{DD}	– 10	– 6	– 6	V
Rise Time	t_r		10		20		35	ns	V_{GG}	20	12	8	V
Turn OFF Delay Time	$t_{d(off)}$		6		8		20	ns	R_L	130	910	2000	Ω
Fall Time	t_f		15		30		60	ns	R_G	100	220	390	Ω
									$I_{D(ON)}$	– 15	– 7	– 3	mA

TO-18 Package
See Section G for Outline Dimensions

Surface Mount
SMP5114, SMP5115, SMP5116

Pin Configuration
1 Source 1, 2 Gate & Case, 3 Drain

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IFN5432, IFN5433, IFN5434

N-Channel Silicon Junction Field-Effect Transistor

- Analog Low On Resistance Switches
- Choppers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 25 V
Continuous Forward Gate Current	100 mA
Continuous Device Power Dissipation	300 mW
Power Derating	2.4 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		IFN5432		IFN5433		IFN5434		Process NJ903		
		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25		– 25		– 25		V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 200		– 200		– 200	pA	V_{GS} = – 15V, V_{DS} = ØV	
			– 200		– 200		– 200	nA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 4	– 10	– 3	– 9	– 1	– 4	V	V_{DS} = 5V, I_G = 3 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	150		100		30		mA	V_{DS} = 15V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$		200		200		200	pA	V_{DS} = 5V, V_{GS} = – 10V	
			200		200		200	nA	V_{DS} = 5V, V_{GS} = – 10V	T_A = 150°C
Drain Source ON Voltage	V_{DS}		50		70		100	mV	V_{GS} = ØV, I_D = 10 mA	
Static Drain Source ON Resistance	$r_{DS(ON)}$	2	5		7		10	Ω	V_{DS} = ØV, I_D = 10 mA	
Dynamic Electrical Characteristics										
Drain Source ON Resistance	$r_{ds(on)}$		5		7		10	Ω	V_{GS} = ØV, I_D = ØA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		60		60		60	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		20		20		20	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Switching Characteristics										
Turn ON Delay Time	$t_{d(on)}$		4		4		4	ns	V_{DD} = 1.5 V, $V_{GS(ON)}$ = ØV $V_{GS(OFF)}$ = – 12V, $I_{D(ON)}$ = 10 mA **(IFN5432)** R_L = 145 Ω **(IFN5433)** R_L = 143 Ω **(IFN5433)** R_L = 140 Ω	
Rise Time	t_r		1		1		1	ns		
Turn OFF Delay Time	$t_{d(off)}$		6		6		6	ns		
Fall Time	t_f		30		30		30	ns		

TO-52 Package

Dimensions in Inches (mm)

Pin Configuration

1 Source, 2 Drain, 3 Gate & Case

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IFN5564, IFN5565, IFN5566

N-Channel Dual Silicon Junction Field-Effect Transistor

- Wide Band Differential Amplifier
- Commutators

Absolute maximum ratings at T_A = 25°C.

Reverse Gate Source & Reverse Gate Drain Voltage	– 40 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	650 mW
Power Derating	3.3 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		IFN5564		IFN5565		IFN5566		Process NJ72		
		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 40		– 40		– 40		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Leakage Voltage	I_{GSS}		– 100		– 100		– 100	pA	V_{GS} = – 20 V, V_{DS} = ØV	
			– 200		– 200		– 200	nA		T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.5	– 3	– 0.5	– 3	– 0.5	– 3	V	V_{DS} = 15 V, I_D = 1 nA	
Gate Source Voltage	$V_{GS(f)}$		1		1		1	V	V_{DS} = ØV, I_G = 2 mA	
Saturation Current (Pulsed)	I_{DSS}	5	30	5	30	5	30	mA	V_{DS} = 15 V, V_{GS} = ØV	
Static Drain Source ON Resistance	$rDS_{(ON)}$		100		100		100	Ω	I_D = 1 mA, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Common Source Forward Transconductance	g_{fs}	7000	12500	7000	12500	7000	12500	µhmo	V_{DG} = 15 V, I_D = 2 mA	f = 1 kHz
		7000		7000		7000		µhmo		f = 100 MHz
Common Source Output Transconductance	g_{os}		45		45		45	µhmo	V_{DS} = 15 V, I_D = 2 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}		12		12		12	pF	V_{DS} = 15 V, I_D = 2 mA	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		3		3		3	pF	V_{DS} = 15 V, I_D = 2 mA	f = 1 MHz
Noise Figure	NF		1		1		1	dB	V_{DS} = 15 V, I_D = 2 mA, R_G = 1 MΩ	f = 10 Hz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		50		50		50	nV/√Hz	V_{DG} = 15 V, I_D = 2 mA	f = 10 Hz
Characteristics										
Saturation Drain Current Ratio (Pulsed)	$\frac{I_{DSS1}}{I_{DSS2}}$	0.95	1	0.95	1	0.95	1	– / –	V_{DG} = 15 V, V_{GS} = ØV	
Differential Gate Source Voltage	$\lvert V_{GS(1)} - V_{GS(2)} \rvert$		5		10		20	mV	V_{DS} = 15 V, I_D = 2 mA	
Gate Source Voltage Differential Drift	$\frac{\Delta \lvert V_{GS(f)} - V_{GS(f)} \rvert}{\Delta T}$		10		25		50	µV/°C	V_{DS} = 15 V,	T_A = 25°C T_B = 125°C
			10		25		50	µV/°C	I_D = 2 mA	T_A = 55°C T_B = 25°C
Transconductance Ratio (Pulsed)	$\frac{g_{fs(1)}}{g_{fs(2)}}$	0.95	1	0.9	1	0.9	1	– / –	V_{DS} = 15 V, I_D = 2 mA	

TO-71 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate, 4 Omitted,
5 Source, 6 Drain, 7 Gate, 8 Omitted

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IFN5911, IFN5912

N-Channel Dual Silicon Junction Field-Effect Transistor

- VHF Amplifiers
- Wideband Differential Amplifiers

Absolute maximum ratings at T_A = 25°C

Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	500 mW
Power Derating	4 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IFN5911		IFN5912		Process NJ30L or NJ36D		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25		– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 100		– 100	pA	V_{GS} = – 15V, V_{DS} = ØV	
			– 250		– 250	nA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 150°C
Gate Operating Current	I_G		– 100		– 100	pA	V_{DG} = 10V, I_D = 5 mA	
			– 100		– 100	nA	V_{DG} = 10V, I_D = 5 mA	T_A = 125°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1	– 5	– 1	– 5	V	V_{DS} = 10V, I_D = 1 nA	
Gate Source Voltage	V_{GS}	– 0.3	– 4	– 0.3	– 4	V	V_{DS} = 10V, I_D = 5 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	7	40	7	40	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics								
Common Source Forward Transconductance	g_{fs}	3000	10000	3000	10000	µS	V_{DG} = 10V, I_D = 5 mA	f = 1 kHz
		3000	10000	3000	10000	µS	V_{DG} = 10V, I_D = 5 mA	f = 100 MHz
Common Source Output Conductance	g_{os}		100		100	µS	V_{DG} = 10V, I_D = 5 mA	f = 1 kHz
			150		150	µS	V_{DG} = 10V, I_D = 5 mA	f = 100 MHz
Common Source Input Capacitance	C_{iss}		5		5	pF	V_{DG} = 10V, I_D = 5 mA	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		1.2		1.2	pF	V_{DG} = 10V, I_D = 5 mA	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		20		20	nV/√Hz	V_{DG} = 10V, I_D = 5 mA	f = 10 kHz
Noise Figure	NF		1		1	dB	V_{DG} = 10V, I_D = 5 mA R_G = 100 KΩ	f = 10 Hz
Differential Gate Current	$\lvert I_{G1}\rvert - \lvert I_{G2}\rvert$		20		20	nA	V_{DG} = 10V, I_D = 5 mA	T_A = 125°C
Saturation Drain Current Ratio	I_{DSS1}/I_{DSS2}	0.95	1	0.95	1		V_{DS} = 10V, V_{GS} = ØV	
Differential Gate Source Voltage	$V_{GS1} - V_{GS2}$		10		15	mV	V_{DG} = 10V, I_D = 5 mA	
Gate Source Voltage Differential Drift	$\frac{\Delta V_{GS1} - V_{GS2}}{\Delta T}$		20		40	µV/°C	V_{DG} = 10V, I_D = 5 mA	T_A = 25°C T_B = 125°C
	$\frac{\Delta V_{GS1} - V_{GS2}}{\Delta T}$		20		40	µV/°C	V_{DG} = 10V, I_D = 5 mA	T_A = – 55°C T_B = 25°C
Transconductance Ratio	g_{fs1}/g_{fs2}	0.95	1	0.95	1		V_{DG} = 10V, I_D = 5 mA	f = 1 kHz

TO-78 Package

See Section G for Outline Dimensions

Pin Configuration

1 Source, 2 Drain, 3 Gate, 4 Case,
5 Source, 6 Drain, 7 Gate, 8 Omitted

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IFN6449, IFN6450

N-Channel Silicon Junction Field-Effect Transistor

- High Voltage

Absolute maximum ratings at T_A = 25°C

	IFN6449	IFN6450
Reverse Gate Source Voltage	– 100 V	– 100 V
Reverse Gate Drain Voltage	– 300 V	– 200 V
Continuous Forward Gate Current	10 mA	10 mA
Continuous Device Power Dissipation	800 mW	800 mW
Power Derating	6.4 mW/°C	6.4 mW/°C

At 25°C free air temperature:		IFN6449		IFN6450		Process NJ42		
Static Electrical Characteristics		Min	Max	Min	Max	Unit	Test Conditions	
Gate Drain Breakdown Voltage	$V_{(BR)GDO}$	– 300		– 200		V	I_G = – 10 µA, I_S = ØA	
Gate Source Breakdown Voltage	$V_{(BR)GSO}$	– 100		– 100		V	I_G = – 10 µA, I_D = ØA	
Gate Reverse Current	I_{GSS}				– 100	nA	V_{GS} = – 80V, V_{DS} = ØV	
					– 100	µA	V_{GS} = – 80V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 2	– 15	– 2	– 15	V	V_{DS} = 30V, I_D = 4 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	2	10	2	10	mA	V_{DS} = 30V, V_{GS} = ØV	
Dynamic Electrical Characteristics								
Common Source Forward Transfer Transmittance	$\lvert Y_{fs} \rvert$	0.5	3	0.5	3	mS	V_{DS} = 30V, V_{GS} = ØV	f = 1 kHz
Common Source Output Conductance	g_{os}		100		100	µS	V_{DS} = 30V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		10		10	pF	V_{DS} = 30V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		5		5	pF	V_{DS} = 30V, V_{GS} = ØV	f = 1 MHz

TO-39 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

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J108, J109

N-Channel Silicon Junction Field-Effect Transistor

- Choppers
- Commutators
- Analog Switches

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 25 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature:		J108		J109		Process NJ450		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25		– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 3		– 3	nA	V_{GS} = – 15V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 3	– 10	– 2	– 6	V	V_{DS} = 5V, I_D = 1 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	80		40		mA	V_{DS} = 15V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$		3		3	nA	V_{DS} = 5V, V_{GS} = – 10V	
Dynamic Electrical Characteristics								
Drain Source ON Resistance	$r_{ds(on)}$		8		12	Ω	V_{GS} = Ø, V_{DS} < = 0.1V	f = 1 kHz
Drain Gate Capacitance	C_{gd}		15		15	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Source Gate Capacitance	C_{gs}		15		15	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Drain Gate + Source Gate Capacitance	C_{gd} + C_{gs}		85		85	pF	V_{DS} = V_{GS} = ØV	f = 1 MHz
Switching Characteristics		**Typ**		**Typ**				
Turn ON Delay Time	$td_{(on)}$	3		3		ns		
Rise Time	t_r	1		1		ns		
Turn OFF Delay Time	$td_{(off)}$	4		4		ns		
Fall Time	t_f	18		18		ns		

	J108	J109	
V_{DD}	1.5	1.5	V
$V_{GS(OFF)}$	– 12	– 7	V
R_L	150	150	Ω

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

Surface Mount
SMPJ108, SMPJ109

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J110, J110A

N-Channel Silicon Junction Field-Effect Transistor

- Choppers
- Commutators
- Analog Switches

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 25 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature:		J110		J110A		Process NJ450		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25		– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 3		– 3	nA	V_{GS} = – 15V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.5	– 4	– 0.5	– 4	V	V_{DS} = 5V, I_D = 1 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	10		10		mA	V_{DS} = 15V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$		3		3	nA	V_{DS} = 5V, V_{GS} = – 10V	
Dynamic Electrical Characteristics								
Drain Source ON Resistance	$r_{ds(on)}$		18		25	Ω	V_{GS} = Ø, V_{DS} < = 0.1V	f = 1 kHz
Drain Gate Capacitance	C_{gd}		15		15	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Source Gate Capacitance	C_{gs}		15		15	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Drain Gate + Source Gate Capacitance	C_{gd} + C_{gs}		85		85	pF	V_{DS} = V_{GS} = ØV	f = 1 MHz

Switching Characteristics		**Typ**	**Typ**					
Turn ON Delay Time	$td_{(on)}$	4	4	ns		**J110**	**J110A**	
Rise Time	t_r	1	1	ns	V_{DD}	1.5	1.5	V
Turn OFF Delay Time	$td_{(off)}$	6	6	ns	$V_{GS(OFF)}$	– 5	– 5	V
Fall Time	t_f	30	30	ns	R_L	150	150	Ω

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

Surface Mount
SMPJ110, SMPJ110A

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J111, J112, J113

N-Channel Silicon Junction Field-Effect Transistor

- Choppers
- Commutators
- Analog Switches

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 35 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature Static Electrical Characteristics		J111		J112		J113		Process NJ132		
		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 35		– 35		– 35		V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 1		– 1		– 1	nA	V_{GS} = – 15V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 3	– 10	– 1	– 5		– 3	V	V_{DS} = 5V, I_D = 1 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	20		5		2		mA	V_{DS} = 15V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$		– 1		– 1		– 1	nA	V_{DS} = 15V, V_{GS} = – 10V	
Dynamic Electrical Characteristics										
Drain Source ON Resistance	$r_{ds(on)}$		30		50		100	Ω	V_{GS} = ØV, V_{DS} = 0.1V	f = 1 kHz
Drain Gate Capacitance	C_{dg}		5		5		5	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Source Gate Capacitance	C_{gs}		5		5		5	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Drain Gate + Source Gate Capacitance	C_{gd} + C_{gs}		28		28		28	pF	V_{DS} = V_{GS} = ØV	f = 1 MHz

Switching Characteristics		Typ	Typ	Typ			J111	J112	J113	
Turn ON Delay Time	$t_{d(on)}$	7	7	7	ns					
Rise Time	t_r	6	6	2	ns	V_{DD}	10	10	10	V
Turn OFF Delay Time	$t_{d(off)}$	20	20	20	ns	$V_{GS(OFF)}$	– 12	– 7	– 5	V
Fall Time	t_f	15	15	15	ns	R_L	800	1600	3200	Ω

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

Surface Mount
SMPJ111, SMPJ112, SMPJ113

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J174, J175

P-Channel Silicon Junction Field-Effect Transistor

- Choppers
- Commutators
- Analog Switches

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 30 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature:		J174		J175		Process PJ99		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	30		30		V	I_G = 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		1		1	nA	V_{GS} = 20V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	5	10	3	6	V	V_{DS} = – 15V, I_D = – 10 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	– 20	– 125	– 7	– 70	mA	V_{DS} = – 15V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$		– 1		– 1	nA	V_{DS} = – 15V, V_{GS} = 10V	
Dynamic Electrical Characteristics			**Max**		**Max**			
Drain Source ON Resistance	$r_{ds(on)}$		85		85	Ω	V_{GS} = Ø, V_{DS} < = 0.1V	f = 1 kHz
Dynamic Electrical Characteristics			**Typ**		**Typ**			
Drain Gate Capacitance	C_{gd}		5.5		5.5	pF	V_{DS} = ØV, V_{GS} = 10V	f = 1 MHz
Source Gate Capacitance	C_{gs}		5.5		5.5	pF	V_{DS} = ØV, V_{GS} = 10V	f = 1 MHz
Drain Gate + Source Gate Capacitance	C_{gd} + C_{gs}		32		32	pF	V_{DS} = V_{GS} = ØV	f = 1 MHz
Switching Characteristics								
Turn ON Delay Time	$td_{(on)}$		2		5	ns		
Rise Time	t_r		5		10	ns		
Turn OFF Delay Time	$td_{(off)}$		5		10	ns		
Fall Time	t_f		10		20	ns		

	J174	J175	
V_{DD}	– 10	– 6	V
$V_{GS(OFF)}$	12	8	V
R_L	560	1.2 k	Ω
$V_{GS(ON)}$	Ø	Ø	V

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Gate, 3 Source

Surface Mount
SMPJ174, SMPJ175

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J176, J177

P-Channel Silicon Junction Field-Effect Transistor

- Choppers
- Commutators
- Analog Switches

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 30 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature:		J176		J177		Process PJ99		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	30		30		V	I_G = 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		1		1	nA	V_{GS} = 20V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	1	4	0.8	2.25	V	V_{DS} = – 15V, I_D = – 10 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	– 2	– 35	– 1.5	– 20	mA	V_{DS} = – 15V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$		– 1		– 1	nA	V_{DS} = – 15V, V_{GS} = 10V	
Dynamic Electrical Characteristics			**Max**		**Max**			
Drain Source ON Resistance	$r_{ds(on)}$		250		300	Ω	V_{GS} = Ø, V_{DS} < = 0.1V	f = 1 kHz
Dynamic Electrical Characteristics			**Typ**		**Typ**			
Drain Gate Capacitance	C_{gd}		5.5		5.5	pF	V_{DS} = ØV, V_{GS} = 10V	f = 1 MHz
Source Gate Capacitance	C_{gs}		5.5		5.5	pF	V_{DS} = ØV, V_{GS} = 10V	f = 1 MHz
Drain Gate + Source Gate Capacitance	C_{gd} + C_{gs}		32		32	pF	V_{DS} = V_{GS} = ØV	f = 1 MHz
Switching Characteristics								
Turn ON Delay Time	$td_{(on)}$		15		20	ns		
Rise Time	t_r		20		25	ns		
Turn OFF Delay Time	$td_{(off)}$		15		20	ns		
Fall Time	t_f		20		25	ns		

	J176	J177	
V_{DD}	– 6	– 6	V
$V_{GS(OFF)}$	6	3	V
R_L	5.6 k	10 k	Ω
$V_{GS(ON)}$	Ø	Ø	V

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Gate, 3 Source

Surface Mount
SMPJ176, SMPJ177

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J201, J202

N-Channel Silicon Junction Field-Effect Transistor

- Audio Amplifiers
- General Purpose Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 40 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		J201			J202			Process NJ16		
		Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 40			– 40			V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 100			– 100	pA	V_{GS} = – 20V, V_{DS} = ØV	
Gate Operating Current	I_G		– 10			– 10		pA	V_{DG} = 20V, I_D = $I_{DSS(min)}$	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.3		– 1.5	– 0.8		– 4	V	V_{DS} = 20V, I_D = 10 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	0.2		1	0.9		4.5	mA	V_{DSS} = 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Common Source Forward Transconductance	g_{fs}	500			1000			µS	V_{DS} = 20V, V_{GS} = ØV	f = 1 kHz
Common Source Output Conductance	g_{os}		1			3.5		µS	V_{DS} = 20V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		4			4		pF	V_{DS} = 20V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		1			1		pF	V_{DS} = 20V, V_{GS} = ØV	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		5			5		nV/√Hz	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

Surface Mount
SMPJ201, SMPJ202

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J203, J204

N-Channel Silicon Junction Field-Effect Transistor

- Audio Amplifiers
- General Purpose Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 40 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature:		J203			J204			Process NJ16		
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 40			– 25			V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 100			– 100	pA	V_{GS} = – 20V, V_{DS} = ØV	
Gate Operating Current	I_G		– 10			– 10		pA	V_{DG} = 20V, I_D = $I_{DSS(min)}$	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 2		– 10	– 0.3		– 2	V	V_{DS} = 20V, I_D = 10 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	4		20	0.2	1.2	3	mA	V_{DS} = 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Common Source Forward Transconductance	g_{fs}	1500			500	1500		µS	V_{DS} = 20V, V_{GS} = ØV	f = 1 kHz
Common Source Output Conductance	g_{os}		10			2.5		µS	V_{DS} = 20V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		4			4		pF	V_{DS} = 20V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		1			1		pF	V_{DS} = 20V, V_{GS} = ØV	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		5			10		nV/√Hz	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

Surface Mount
SMPJ203, SMPJ204

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J210, J211

N-Channel Silicon Junction Field-Effect Transistor

- Audio Amplifiers
- General Purpose Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 25 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		J210			J211			Process NJ26L		
		Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25			– 25			V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 100			– 100	pA	V_{GS} = – 15V, V_{DS} = ØV	
Gate Operating Current	I_G		– 10			– 10		pA	V_{DS} = 20V, I_D = 1 mA	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1		– 3	– 2.5		– 4.5	V	V_{DS} = 15V, I_D = 1 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	2		15	7		20	mA	V_{DS} = 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Common Source Forward Transconductance	g_{fs}	4000		12000	6000		12000	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Output Conductance	g_{os}			150			200	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		4			4		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		1			1		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		10			10		nV/√Hz	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

Surface Mount
SMPJ210, SMPJ211

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J212

N-Channel Silicon Junction Field-Effect Transistor

- Audio Amplifier
- General Purpose Amplifier

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 25 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature:		J212			Process NJ26L		
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25			V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 100	pA	V_{GS} = – 15V, V_{DS} = ØV	
Gate Operating Current	I_G		– 10		pA	V_{DS} = 20V, I_D = 1 mA	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 4		– 6	V	V_{DS} = 15V, I_D = 1 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	15		40	mA	V_{DS} = 15V, V_{GS} = Ø V	
Dynamic Electrical Characteristics							
Common Source Forward Transconductance	g_{fs}	7000		12000	µS	V_{DS} = 15V, V_{GS} = Ø V	f = 1 kHz
Common Source Output Conductance	g_{os}			200	µS	V_{DS} = 15V, V_{GS} = Ø V	f = 1 kHz
Common Source Input Capacitance	C_{iss}		4		pF	V_{DS} = 15V, V_{GS} = Ø V	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		1		pF	V_{DS} = 15V, V_{GS} = Ø V	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		10		nV/√Hz	V_{DS} = 15V, V_{GS} = Ø V	f = 1 kHz

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

Surface Mount
SMPJ212

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J230, J231

N-Channel Silicon Junction Field-Effect Transistor

- Audio Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 40 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		J230			J231			Process NJ16		
		Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 40			– 40			V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 250			– 250	pA	V_{GS} = – 30V, V_{DS} = ØV	
Gate Operating Current	I_G		– 2			– 2		pA	V_{DS} = 20V, I_D = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.5		– 3	– 1.5		– 5	V	V_{DS} = 20V, I_D = 1 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	0.7		3	2		6	mA	V_{DS} = 20V, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Common Source Forward Transconductance	g_{fs}	1000		3500	1500		4000	µS	V_{DS} = 20V, V_{GS} = ØV	f = 1 kHz
Common Source Output Conductance	g_{os}		1.5			3		µS	V_{DS} = 20V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		4			4		pF	V_{DS} = 20V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		1			1		pF	V_{DS} = 20V, V_{GS} = ØV	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		8	30		8	30	nV/√Hz	V_{DS} = 10V, V_{GS} = ØV	f = 10 Hz
			2			2		nV/√Hz	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

Surface Mount
SMPJ230, SMPJ231

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J232

N-Channel Silicon Junction Field-Effect Transistor

- **Audio Amplifier**

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 40 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature:		J232			Process NJ16		
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 40			V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 250	pA	V_{GS} = – 30V, V_{DS} = ØV	
Gate Operating Current	I_G		– 2		pA	V_{DS} = 20V, I_D = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 3		– 6	V	V_{DS} = 20V, I_D = 1 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	5		10	mA	V_{DS} = 20V, V_{GS} = Ø V	
Dynamic Electrical Characteristics							
Common Source Forward Transconductance	g_{fs}	2500		5000	µS	V_{DS} = 20V, V_{GS} = Ø V	f = 1 kHz
Common Source Output Conductance	g_{os}		5		µS	V_{DS} = 20V, V_{GS} = Ø V	f = 1 kHz
Common Source Input Capacitance	C_{iss}		4		pF	V_{DS} = 20V, V_{GS} = Ø V	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		1		pF	V_{DS} = 20V, V_{GS} = Ø V	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		20	30	nV/√Hz	V_{DS} = 10V, V_{GS} = Ø V	f = 10 Hz
			6		nV/√Hz	V_{DS} = 10V, V_{GS} = Ø V	f = 1 kHz

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

Surface Mount
SMPJ232

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J304, J305

N-Channel Silicon Junction Field-Effect Transistor

- Mixers
- Oscillators
- VHF/UHF Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 30 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		J304			J305			Process NJ26		
		Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 30			– 30			V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 100			– 100	pA	V_{GS} = – 20V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 2		– 6	– 0.5		– 3	V	V_{DS} = 15V, I_D = 1 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	5		15	1		8	mA	V_{DS} = 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Common Source Forward Transconductance	g_{fs}	4500		7500	3000			µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
						3000		µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
			4200					µS	V_{DS} = 15V, V_{GS} = ØV	f = 400 MHz
Common Source Output Conductance	g_{os}			50			50	µS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		3			3		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		0.85			0.85		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Output Capacitance	C_{oss}		1			1		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Output Conductance	g_{os}		60			60		µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
			80					µS	V_{DS} = 15V, V_{GS} = ØV	f = 400 MHz
Common Source Output Susceptance	b_{os}		800			800		µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
			3600					µS	V_{DS} = 15V, V_{GS} = ØV	f = 400 MHz
Common Source Input Conductance	g_{is}		80			80		µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
			800					µS	V_{DS} = 15V, V_{GS} = ØV	f = 400 MHz
Common Source Input Susceptance	b_{is}		2000			2000		µS	V_{DS} = 15V, V_{GS} = ØV	f = 100 MHz
			7500					µS	V_{DS} = 15V, V_{GS} = ØV	f = 400 MHz
Common Source Power Gain	G_{ps}		20					dB	V_{DS} = 15V, I_D = 5 mA	f = 100 MHz
			11					dB	V_{DS} = 15V, I_D = 5 mA	f = 400 MHz
Noise Figure	NF		1.7					dB	V_{DS} = 15V, I_D = 5 mA R_G = 1 Ω	f = 100 MHz
			3.8					dB		f = 400 MHz

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

Surface Mount
SMPJ304, SMPJ305

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J308, J309

N-Channel Silicon Junction Field-Effect Transistor

- Mixers
- Oscillators
- VHF/UHF Amplifiers

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 25 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		J308			J309			Process NJ72		
		Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25			– 25			V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 1			– 1	nA	V_{GS} = – 15V, V_{DS} = ØV	
				– 1			– 1	µA	V_{GS} = – 15V, V_{DS} = ØV	T_A = +125°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1		– 6.5	– 1		– 4	V	V_{DS} = 10V, I_D = 1 nA	
Gate Source Forward Voltage	$V_{GS(F)}$			1			1	V	V_{DS} = ØV, I_G = 1 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	12		60	12		30	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Common Source Forward Transconductance	g_{fs}	8000	17000		10000	17000		µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Common Source Output Conductance	g_{os}			250			250	µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Common Gate Forward Transconductance	g_{fg}		13000			13000		µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Common Gate Output Transconductance	g_{og}		150			100		µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Gate Drain Capacitance	C_{dg}		1.8	2.5		1.8	2.5	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Gate Source Capacitance	C_{gs}		4	5		4	5	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		10			10		nV/√Hz	V_{DS} = 10V, I_D = 10 mA	f = 100 kHz
Common Source Forward Transconductance	$Re_{(Yfs)}$		12			12		µS	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
Common Gate Input Conductance	$Re_{(Yig)}$		14			14		µS	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
Common Source Input Conductance	$Re_{(Yis)}$		0.4			0.4		µS	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
Common Source Output Conductance	$Re_{(Gos)}$		0.15			0.15		µS	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
Common Gate Power Gain at Noise Match	G_{pg}		16			16		dB	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
			11			11		dB	V_{DS} = 10V, I_D = 10 mA	f = 450 MHz
Noise Figure	NF		1.5			1.5		dB	V_{DS} = 15V, I_D = 10 mA	f = 105 MHz
			2.7			2.7		dB	V_{DS} = 15V, I_D = 10 mA	f = 450 MHz

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

Surface Mount
SMPJ308, SMPJ309

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J310

N-Channel Silicon Junction Field-Effect Transistor

- Mixer
- Oscillator
- VHF/UHF Amplifier

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source Voltage	– 25 V
Reverse Gate Drain Voltage	– 25 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	360 mW

At 25°C free air temperature:		J310			Process NJ72		
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25			V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 1	nA	V_{GS} = – 15V, V_{DS} = ØV	
				– 1	µA	V_{GS} = – 15V, V_{DS} = ØV	T_A = + 125°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 2		– 6.5	V	V_{DS} = 10V, I_D = 1 nA	
Gate Source Forward Voltage	$V_{GS(F)}$			1	V	V_{DS} = ØV, I_G = 1 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	24		60	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics							
Common Source Forward Transconductance	g_{fs}	8000	17000		µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Common Source Output Conductance	g_{os}			250	µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Common Gate Forward Transconductance	g_{fg}		1200		µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Common Gate Output Transconductance	g_{og}		150		µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Gate Drain Capacitance	C_{dg}		1.8	2.5	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Gate Source Capacitance	C_{gs}		4	5	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		10		nV/√Hz	V_{DS} = 10V, I_D = 10 mA	f = 100 Hz
Common Source Forward Transconductance	Re (Y_{fs})		12		µS	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
Common Gate Input Conductance	Re (Y_{ig})		14		µS	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
Common Source Input Conductance	Re (Y_{is})		0.4		µS	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
Common Source Output Conductance	Re (g_{os})		0.15		µS	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
Common Gate Power Gain at Noise Match	G_{pg}		16		dB	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
			11		dB	V_{DS} = 10V, I_D = 10 mA	f = 450 MHz
Noise Figure	NF		1.5		dB	V_{DS} = 15V, I_D = 10 mA	f = 105 MHz
			2.7		dB	V_{DS} = 15V, I_D = 10 mA	f = 450 MHz

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Drain, 2 Source, 3 Gate

Surface Mount
SMPJ310

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P1086, P1087

P-Channel Silicon Junction Field-Effect Transistor

- Choppers
- Analog Switches

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	30 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature:		P1086		P1087		Process PJ99		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	30		30		V	I_G = 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		2		2	nA	V_{GS} = 15V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$		10		5	V	V_{DS} = – 15V, I_D = – 1 µA	
Saturation Drain Current (Pulsed)	I_{DSS}	– 10		– 5.0		mA	V_{DS} = – 20V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$		– 10		– 10	nA	V_{DS} = – 15V, V_{GS} = 12V (P1086)	
			– 0.5		– 0.5	µA	V_{GS} = 7V (P1087)	T_A = 85°C
Drain Reverse Current	I_{DGO}		2		2	nA	V_{DG} = – 15V, I_S = ØA	
			0.1		0.1	µA	V_{DG} = – 15V, I_S = ØA	T_A = 85°C
Drain Source ON Voltage	$V_{DS(ON)}$		– 0.5		– 0.5	V	V_{GS} = ØV, I_D = – 6 mA (P1086)	
			– 0.5		– 0.5	V	V_{GS} = ØV, I_D = – 3 mA (P1087)	
Static Drain Source ON Resistance	$r_{DS(ON)}$		75		150	Ω	I_D = – 1 mA, V_{GS} = ØV	
Dynamic Electrical Characteristics								
Drain Source ON Resistance	$r_{ds(on)}$		75		150	Ω	I_D = Ø, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		45		45	pF	V_{DS} = – 15V, V_{GS} = ØV	f = 1 kHz
Common Source Reverse Transfer Capacitance	C_{rss}		10		10	pF	V_{DS} = ØV, V_{GS} = 12V (P1086)	f = 1 MHz
			10		10	pF	V_{DS} = ØV, V_{GS} = 7V (P1087)	
Switching Characteristics								
Turn ON Delay Time	$td_{(on)}$		15		15	ns	V_{DD} = – 6V, $V_{GS(ON)}$ = ØV	
Rise Time	t_r		20		75	ns		
Turn OFF Delay Time	$td_{(off)}$		15		25	ns		
Fall Time	t_f		50		100	ns		

	P1086	P1087	
$V_{GS(OFF)}$	12	7	V
$V_{D(ON)}$	– 6	– 3	MA
R_L	910	1.8K	Ω

TO-226AA Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate

Surface Mount
SMPP1086, SMPP1087

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SMP5911, SMP5912

Dual N-Channel Silicon Junction Field-Effect Transistor

- **Wideband Differential Amplifiers**

At 25°C free air temperature:		SMP5911		SMP5912		Process NJ30L		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25		– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 100		– 100	pA	V_{GS} = – 15V, V_{DS} = ØV	
			– 250		– 250	nA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 150°C
Gate Operating Current	I_G		– 100		– 100	pA	V_{DG} = 10V, I_D = 5 mA	
			– 100		– 100	nA	V_{DG} = 10V, I_D = 5 mA	T_A = 125°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1.0	– 5	– 1.0	– 5	V	V_{DS} = 15V, I_D = 5 nA	
Gate Source Voltage	V_{GS}	– 0.3	– 4	– 0.3	– 4	V	V_{DS} = 15V, I_D = 5 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	7	40	7	40	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics								
Common Source Forward Transconductance	g_{fs}	3000	10000	3000	10000	µS	V_{DG} = 10V, I_D = 5 mA	f = 1 kHz
		3000	10000	3000	10000	µS	V_{DG} = 10V, I_D = 5 mA	f = 100 MHz
Common Source Output Conductance	g_{os}		100		100	µS	V_{DG} = 10V, I_D = 5 mA	f = 1 kHz
			150		150	µS	V_{DG} = 10V, I_D = 5 mA	f = 100 MHz
Common Source Input Capacitance	C_{iss}		5		5	pF	V_{DG} = 10V, I_D = 5 mA	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		1.2		1.2	pF	V_{DG} = 10V, I_D = 5 mA	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		20		20	nV/√Hz	V_{DG} = 10V, I_D = 5 mA	f = 10 kHz
Noise Figure	NF		1		1	dB	V_{DG} = 10V, I_D = 5 mA R_G = 100 KΩ	f = 10 kHz
Gate Source Differential Voltage	$V_{GS1} - V_{GS2}$		10		15	mV	V_{DG} = 10V, I_D = 5 mA	
Gate Differential Current	$I_{G1} - I_{G2}$		20		20	nA	V_{DG} = 10V, I_D = 5 mA	T_A = 125°C
Drain Saturation Current Ratio	I_{DSS1} / I_{DSS2}	0.95	1	0.95	1		V_{DG} = 10V, V_{GS} = ØV	
Transconductance Ratio	g_{fs1} / g_{fs2}	0.95	1	0.95	1		V_{DG} = 10V, I_D = 5 mA	f = 1 kHz
Gate Source Differential Voltage With Temperature	$\frac{\Delta V_{GS1} - V_{GS2}}{\Delta T}$		20		40	µV/°C	V_{DG} = 10V, I_D = 5 mA	T_A = 25°C
			20		40	µV/°C	V_{DG} = 10V, I_D = 5 mA	T_B = 125°C
			20		40	µV/°C	V_{DG} = 10V, I_D = 5 mA	T_A = 35°C
			20		40	µV/°C	V_{DG} = 10V, I_D = 5 mA	T_B = 25°C

SOIC-8 Package
See Section G for Outline Dimensions

Pin Configuration
1 Source 1, 2 Drain 1, 3 Gate 1, 4 N/C,
5 Source 2, 6 Drain 2, 7 Gate 2,
8 Omitted

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U290, U291

N-Channel Silicon Junction Field-Effect Transistor

- Choppers
- Low On Resistance Switches

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 30 V
Continuous Forward Gate Current	100 mA
Continuous Device Power Dissipation	500 mW
Power Derating	4 mW/°C

At 25°C free air temperature:		U290		U291		Process NJ1800D		
Static Electrical Characteristics		**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 30		– 30		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 1		– 1	nA	V_{GS} = – 15V, V_{DS} = ØA	
			– 1		– 1	µA	V_{GS} = – 15V, V_{DS} = ØA	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 4	– 10	– 1.5	– 4.5	V	V_{DS} = 15V, I_D = 3 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	500		200		mA	V_{DS} = 10V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$		1		1	nA	V_{DS} = 5V, V_{GS} = – 10V	
			1		1	µA	V_{DS} = 5V, V_{GS} = – 10V	T_A = 150°C
Drain Source ON Voltage	$V_{DS(ON)}$		30		70	mV	V_{GS} = ØV, I_D = 10 mA	
Static Drain Source ON Resistance	$r_{DS(ON)}$	1	3	2	7	Ω	V_{GS} = ØV, I_D = 10 mA	
Dynamic Electrical Characteristics								
Drain Source ON Resistance	$r_{ds(on)}$	1	3	2	7	Ω	V_{GS} = ØV, I_D = Ø	f = 1 kHz
Drain Gate OFF Capacitance	C_{dgo}		30		30	pF	V_{DG} = 15V, I_S = ØV	f = 1 MHz
Source Gate OFF Capacitance	C_{sgo}		30		30	pF	V_{DG} = 15V, I_S = ØV	f = 1 MHz
Source Gate Plus Drain Gate	C_{iss}		160		160	pF	V_{DG} = ØV, V_{GS} = ØV	f = 1 MHz
Switching Characteristics								
Turn ON Delay Time	$td_{(on)}$		15		15	ns	V_{DD} = 1.5V, $I_{D(ON)}$ = 30 mA R_L = 50Ω $V_{GS(ON)}$ = ØV **(U290)** $V_{GS(OFF)}$ = – 12V **(U291)** $V_{GS(OFF)}$ = – 7V	
Rise Time	t_r		20		20	ns		
Turn OFF Delay Time	$td_{(off)}$		15		15	ns		
Fall Time	t_f		20		20	ns		

TO-52 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

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U308, U309

N-Channel Silicon Junction Field-Effect Transistor

- Mixers
- Oscillators
- VHF/UHF Amplifiers

Absolute maximum ratings at T_A = 25°C.

Reverse Gate Source & Reverse Gate Drain Voltage	– 25 V
Continuous Forward Gate Current	20 mA
Continuous Device Power Dissipation	500 mW
Power Derating	4 mw/°C

At 25°C free air temperature: Static Electrical Characteristics		U308			U309			Process NJ72		
		Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25			– 25			V	V_{GS} = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 150			– 150	pA	V_{GS} = – 15V, V_{DS} = ØV	
				– 150			– 150	nA	V_{GS} = – 15V, V_{DS} = ØV	T_A = +125°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1		– 6	– 1		– 4	V	V_{DS} = 10V, I_D = 1 nA	
Gate Source Forward Voltage	$V_{GS(F)}$			1			1	V	V_{DS} = ØV, I_G = 10 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	12		60	12		30	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Common Gate Forward Transconductance	G_{fs}	10	17		10	17		mS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
			15			15		mS	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
			14			14		mS	V_{DS} = 10V, I_D = 10 mA	f = 450 MHz
Common Gate Output Conductance	G_{og}			250			250	µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
			0.18			0.18		µS	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
			0.32			0.32		µS	V_{DS} = 10V, I_D = 10 mA	f = 450 MHz
Drain Gate Capacitance	C_{dg}			2.5			2.5	pF	V_{DS} = 10V, V_{GS} = – 10V	f = 1 MHz
Gate Source Capacitance	C_{gs}			5		5		pF	V_{DS} = 10V, V_{GS} = – 10V	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		10			10		nV/√Hz	V_{DS} = 10V, I_D = 10 mA	f = 100 kHz
Common Gate Power Gain	G_{pg}	14	16		14	16		dB	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
		10	11		10	11		dB	V_{DS} = 10V, I_D = 10 mA	f = 450 MHz
Noise Figure	NF		1.5	2		1.5	2	dB	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
			2.7	3.5		2.7	3.5	dB	V_{DS} = 10V, I_D = 10 mA	f = 450 MHz

TO-52 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

Surface Mount
SMPJ308/J309

InterFET Corporation
1000 N. Shiloh Road, Garland, TX 75042
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U310

N-Channel Silicon Junction Field-Effect Transistor

- Mixer
- Oscillator
- VHF/UHF Amplifier

Absolute maximum ratings at T_A = 25°C.

Reverse Gate Source & Reverse Gate Drain Voltage	– 25 V
Continuous Forward Gate Current	20 mA
Continuous Device Power Dissipation	500 mW
Power Derating	4 mW/°C

At 25°C free air temperature:		U310			Process NJ72L		
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25			V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 150	pA	V_{GS} = – 15V, V_{DS} = ØV	
				– 150	nA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 125°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 2.5		– 6	V	V_{DS} = 10V, I_D = 1 nA	
Gate Source Forward Voltage	$V_{GS(F)}$			1	V	V_{DS} = ØV, I_G = 10 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	24		60	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics							
Common Gate Forward Transconductance		10	17		mS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
	g_{fg}		15		mS	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
			14		mS	V_{DS} = 10V, I_D = 10 mA	f = 450 MHz
Common Gate Output Conductance				250	µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
	g_{og}		0.18		µS	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
			0.32		µS	V_{DS} = 10V, I_D = 10 mA	f = 450 MHz
Drain Gate Capacitance	C_{dg}			2.5	pF	V_{DS} = 10V, V_{GS} = – 10V	f = 1 MHz
Gate Source Capacitance	C_{gs}			5	pF	V_{DS} = 10V, V_{GS} = – 10V	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		10		nV/√Hz	V_{DS} = 10V, I_D = 10 mA	f = 100 Hz
Common Gate Power Gain	G_{pg}	14	16		dB	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
		10	11		dB	V_{DS} = 10V, I_D = 10 mA	f = 450 MHz
Noise Figure	NF		1.5	2	dB	V_{DS} = 10V, I_D = 10 mA	f = 105 MHz
			2.7	3.5	dB	V_{DS} = 10V, I_D = 10 mA	f = 450 MHz

TO-52 Package
See Section G for Outline Dimensions

Surface Mount
SMPJ310

Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

InterFET Corporation
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U311

N-Channel Silicon Junction Field-Effect Transistor

- Mixer
- Oscillator
- VHF/UHF Amplifier

Absolute maximum ratings at T_A = 25°C.

Reverse Gate Source & Reverse Gate Drain Voltage	– 25 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	2.4 mW/°C

At 25°C free air temperature:		U311			Process NJ72L		
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25			V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 150	pA	V_{GS} = – 15V, V_{DS} = ØV	
				– 150	nA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1		– 6	V	V_{DS} = 10V, I_D = 1 nA	
Gate Source Forward Voltage	$V_{GS(F)}$			1	V	V_{DS} = ØV, I_G = 1 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	20		60	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics							
Common Gate Forward Transconductance	g_{fg}	1000	17000		µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Common Gate Output Conductance	g_{og}			250	µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Gate Drain Capacitance	C_{dg}			2.5	pF	V_{DS} = 10V, I_D = 10 mA	f = 1 MHz
Gate Source Capacitance	C_{gs}			5	pF	V_{DS} = 10V, I_D = 10 mA	f = 1 MHz

TO-72 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate, 4 Case

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U350

Hybrid Quad Silicon Junction Field-Effect Transistor Array

- Analog Multiplier
- VHF Double-Balanced Mixer

Absolute maximum ratings at T_A = 25°C.

Reverse Gate Source & Reverse Gate Drain Voltage	– 25 V
Gate Current	25 mA
Continuous Device Power Dissipation	400 mW
Power Derating	3.2 mW/°C

At 25°C free air temperature:		U350			Four Matched Process NJ72L		
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25			V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 1	nA	V_{GS} = – 15V, V_{DS} = ØV	
				– 1	µA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 125°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 2		– 6	V	V_{DS} = 10V, I_D = 1 nA	
Gate Source Forward Voltage	$V_{GS(F)}$			1	V	V_{DS} = ØV, I_G = 1 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	24		60	mA	V_{DS} = 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics							
Drain Source ON Resistance	$r_{ds(on)}$		50	90	Ω	V_{GS} = ØV, I_D = mA	f = 1 kHz
Common Source Forward Transconductance	g_{fs}	10		18	mS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Common Source Output Conductance	g_{os}			150	µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
Drain Gate Capacitance	C_{dgo}			2.5	pF	V_{GD} = – 10V, I_S = ØV	f = 1 MHz
Gate Source Capacitance	C_{sgo}			5	pF	V_{GS} = – 10V, I_D = ØV	f = 1 MHz
(Conversion Gain)	G_c		4		dB	V_{DS} = 20V, V_{GS} = 1/2 $V_{GS(OFF)}$ R_D = 1,700 Ω	f = 100 MHz
Noise Figure	NF		7		dB	V_{DS} = 20V, V_{GS} = 1/2 $V_{GS(OFF)}$ R_D = 1,700 Ω	f = 100 MHz
Saturation Drain Current Ratio	I_{DSS} / I_{DSS}	0.9		1		V_{DS} = 15V, V_{DS} = ØV	
Gate Source Cutoff Voltage Ratio	$V_{GS(OFF)}$ / $V_{GS(OFF)}$	0.9		1		V_{DS} = 15V, I_D = 1 nA	
Common Source Forward Transconductance	g_{fs} / g_{fs}	0.9		1		V_{DS} = 15V, I_D = 10 mA	f = 1 kHz
Differential Output Conductance	Y_{os} / Y_{os}	0.9		1		V_{DS} = 15V, I_D = 10 mA	f = 1 kHz

TO-78 Package
Dimensions in Inches (mm)

Pin Configuration
1 Gate 1 & 3, 2 Drain 1 & 4,
3 Source 1 & 2, 4 Ground & Case,
5 Source 3 & 4, 6 Drain 2 & 3,
7 Gate 2 & 4, 8 Omitted

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U430, U431

Dual N-Channel Silicon Junction Field-Effect Transistor

- Balanced Mixers
- Differential Amplifiers

Absolute maximum ratings at T_A = 25°C.

Total Device Dissipation (Derate 4 mW/°C to150°C)	500 mW
Storage Temperature Range	– 65°C to +150°C
Lead Temperature	300°C

At 25°C free air temperature: Static Electrical Characteristics		U430			U431			Process NJ72		
		Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25			– 25			V	I_G = – 1µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 150			– 150	pA	V_{GS} = – 15V, V_{DS} = ØV	
				– 150			– 150	nA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1		– 4	– 2		– 6	V	V_{DS} = 10V, I_D = 1 nA	
Gate Source Forward Voltage	$V_{GS(F)}$			1			1	V	V_{DS} = ØV, I_G = 10 mA	
Drain Saturation Current (Pulsed)	I_{DSS}	12		30	24		60	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics										
Common Source Forward Transconductance	G_{fs}	10	17		10	17		mS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
			12			12		mS	V_{DS} = 10V, I_D = 10 mA	f = 100 MHz
Common Source Output Conductance	G_{os}			250			250	µS	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
			0.15			0.15		µS	V_{DS} = 10V, I_D = 10 mA	f = 100 MHz
Drain Gate Capacitance	C_{dg}			5			5	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Source Gate Capacitance	C_{gs}			2.5			2.5	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$		10			10		nV/√Hz	V_{DS} = 10V, I_D = 10 mA	f = 100 kHz
Power Match Source Admittance	g_{ig}		12			12			V_{DS} = 10V, I_D = 10 mA	f = 100 MHz
Conversion Gain	G_c		3			3		dB	V_{DS} = 20V, R_L = 2 kΩ V_{GS} = 1/2 $V_{GS(OFF)}$	f = 100 MHz
Saturation Drain Current Ratio	I_{DSS1}/I_{DSS2}	0.9		1	0.9		1		V_{DS} = 10V, V_G = ØV	
Gate Source Cutoff Voltage Ratio	$\frac{V_{GS(OFF)1}}{V_{GS(OFF)2}}$	0.9		1	0.9		1		V_{DS} = 10V, I_D = 1 nA	
Transconductance Ratio	g_{fs1}/g_{fs2}	0.9		1	0.9		1		V_{DS} = 10V, I_D = 10 mA	

TO-78 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source 1, 2 Gate 1, Drain 1,
4 Case, 5 Drain 2, 6 Gate 2,
7 Source 2, 8 Omitted

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Semiconductor Databook

Section C

Diode, Regulator & VCR Data Sheets

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DPAD1, DPAD2, DPAD5, DPAD10

Dual Pico-AMP Diode

- **High Impedance Protection Circuits**

Absolute maximum ratings at T_A = 25°C

Continuous Forward Gate Current	50 mA
Storage Temperature Range	– 55°C to +125°C

At 25°C free air temperature: Electrical Characteristics		DPAD1			DPAD2			Process NJ01		
		Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions	
Reverse Current	I_R			– 1			– 2	pA	V_R = – 20V	
Breakdown Reverse Voltage	BV_R	– 45			– 45			V	I_R = – 1 µA	
Forward Voltage Drop	V_F		0.8	1.5		0.8	1.5	V	I_F = 5 mA	
Capacitance	C_R			0.8			0.8	pF	V_R = – 5 V	f = 1 MHz
Differential Capacitance	$\|C_{R1} - C_{R2}\|$			0.2			0.2	pF	$V_{R1} = V_{R2}$ =– 5 V	f = 1 MHz

At 25°C free air temperature: Electrical Characteristics		DPAD5			DPAD10			Process NJ01		
		Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions	
Reverse Current	I_R			– 5			– 10	pA	V_R = – 20V	
Breakdown Reverse Voltage	BV_R	– 45			– 45			V	I_R = – 1 µA	
Forward Voltage Drop	V_F		0.8	1.5		0.8	1.5	V	I_F = 5 mA	
Capacitance	C_R			0.8			2.0	pF	V_R = – 5 V	f = 1 MHz
Differential Capacitance	$\|C_{R1} - C_{R2}\|$		0.2			0.2		pF	$V_{R1} = V_{R2}$ =– 5 V	f = 1 MHz

TO-72 Package

Dimensions in Inches (mm)

Pin Configuration

1 Cathode 1, 2 Anode 1,
3 Cathode 2, 4 Anode 2

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PAD1, PAD2, PAD5

Low Leakage Pico-AMP Diode

- **High Impedance Protection Circuits**

Absolute maximum ratings at T_A = 25°C

Continuous Forward Gate Current	50 mA
Storage Temperature Range	– 55°C to +125°C
Lead Temperature	300°C

At 25°C free air temperature: Electrical Characteristics		PAD1			PAD2			Process NJ01		
		Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions	
Reverse Current	I_R			– 1			– 2	pA	V_R = – 20V	
Breakdown Reverse Voltage	BV_R	– 45			– 45			V	I_R = – 1 µA	
Forward Voltage Drop	V_F		0.8	1.5		0.8	1.5	V	I_F = 5 mA	
Capacitance	C_R			0.8			0.8	pF	V_R = – 5 V	f = 1 MHz

At 25°C free air temperature: Electrical Characteristics		PAD5			Process NJ01		
		Min	Typ	Max	Unit	Test Conditions	
Reverse Current	I_R			– 5	pA	V_R = – 20V	
Breakdown Reverse Voltage	BV_R	– 45			V	I_R = – 1 µA	
Forward Voltage Drop	V_F		0.8	1.5	V	I_F = 5 mA	
Capacitance	C_R			0.8	pF	V_R = – 5 V	f = 1 MHz

TO-18 Package

Dimensions in Inches (mm)

Pin Configuration

1 Cathode, 2 Case, 3 Anode

Surface Mount

TO-236AB Package

See Section G

Pin Configuration

1 Cathode, 2 Cathode, 3 Anode

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J500, J501, J502, J503, J504, J505

Current Regulator Diode

- Current Regulation
- Current Limiting

Absolute maximum ratings at T_A = 25°C

Peak Operating Voltage	50 V
Forward Current	20 mA
Reverse Current	50 mA
Operating & Storage Temperature Range	– 55°C to 135°C

At 25°C free air temperature Electrical Characteristics		J500			J501			J502			Process NJ16	
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Unit	Test Conditions
Forward Current	I_{F1}	0.192	0.240	0.288	0.264	0.33	0.396	0.344	0.43	0.516	mA	V_F = 25V
			Typ			Typ			Typ			
Limiting Voltage	V_L		0.8	1.2		0.9	1.3		1.1	1.5	V	I_F = 0.9 $I_{F(MIN)}$
Peak Operating Voltage	V_{OP}	50			50			50			V	I_F = 1.1 $I_{F(MAX)}$
Dynamic Impedance	Z_{fi}	4	8		2.2	6		1.5	4.4		MΩ	V_F = 25V, f = 1 kHz
Anode– Cathode Capacitance	C_F		2			2			2		pF	V_F = 25V, f = 1 kHz

At 25°C free air temperature Electrical Characteristics		J503			J504			J505			Process NJ16	
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Unit	Test Conditions
Forward Current	I_{F1}	0.448	0.56	0.672	0.6	0.75	0.9	0.8	1	1.2	mA	V_F = 25V
			Typ			Typ			Typ			
Limiting Voltage	V_L		1.2	1.7		1.4	1.9		1.5	2.1	V	I_F = 0.9 $I_{F(MIN)}$
Peak Operating Voltage	V_{OP}	50			50			50			V	I_F = 1.1 $I_{F(MAX)}$
Dynamic Impedance	Z_{fi}	1.2	3.4		0.8	2.5		0.5	1.9		MΩ	V_F = 25V, f = 1 kHz
Anode– Cathode Capacitance	C_F		2			2			2		pF	V_F = 25V, f = 1 kHz

TO-92 Two-Lead Package

Dimensions in Inches (mm)

Pin Configuration

Modified: 1 Anode, 2 Cathode

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J506, J507, J508, J509, J510, J511

Current Regulator Diode

- Current Regulation
- Current Limiting

Absolute maximum ratings at T_A = 25°C

Peak Operating Voltage	50 V
Forward Current	20 mA
Reverse Current	50 mA
Operating & Storage Temperature Range	– 55°C to 135°C

At 25°C free air temperature Electrical Characteristics		J506			J507			J508			Process NJ16	
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Unit	Test Conditions
Forward Current	I_{F1}	1.12	1.4	1.68	1.44	1.8	2.16	1.9	2.4	2.9	mA	V_F = 25V
			Typ			Typ			Typ			
Limiting Voltage	V_L		1.8	2.5		2.0	2.8		2.2	3.1	V	I_F = 0.9 $I_{F(MIN)}$
Peak Operating Voltage	V_{OP}	50			50			50			V	I_F = 1.1 $I_{F(MAX)}$
Dynamic Impedance	Z_{fi}	0.33	1.4		0.2	1.0		0.2	0.7		MΩ	V_F = 25V, f = 1 kHz
Anode– Cathode Capacitance	C_F		2			2			2		pF	V_F = 25V, f = 1 kHz

At 25°C free air temperature Electrical Characteristics		J509			J510			J511			Process NJ16	
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Unit	Test Conditions
Forward Current	I_{F1}	2.4	3.0	3.6	2.9	3.6	4.3	3.8	4.7	5.6	mA	V_F = 25V
			Typ			Typ			Typ			
Limiting Voltage	V_L		2.5	3.5		2.8	3.9		3.0	4.2	V	I_F = 0.9 $I_{F(MIN)}$
Peak Operating Voltage	V_{OP}	50			50			50			V	I_F = 1.1 $I_{F(MAX)}$
Dynamic Impedance	Z_{fi}	0.15	0.6		0.15	0.5		0.12	0.3		MΩ	V_F = 25V, f = 1 kHz
Anode– Cathode Capacitance	C_F		2			2			2		pF	V_F = 25V, f = 1 kHz

TO-92 Two-Lead Package

Dimensions in Inches (mm)

Pin Configuration

1 Anode, 2 Cathode

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J553, J554, J555, J556, J557

Current Regulator Diode

- Current Regulation
- Current Limiting
- Biasing

Absolute maximum ratings at T_A = 25°C.

Peak Operating Voltage	50 V
Continuous Reverse Gate Current	50 mA
Continuous Device Power Dissipation	360 mW
Power Derating	2.88 mW/°C

At 25°C free air temperature Electrical Characteristics		J553			J554			J555			Process NJ16	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Regulator Current	I_F	0.18	0.5	0.75	0.6	1	1.6	1.4	2	2.6	mA	V_F = 25V
Limiting Voltage	V_L		0.75	1.3		0.55	1.75		0.75	2.15	V	I_F = 0.9 $I_{F(MIN)}$
Peak Operating Voltage	V_{OP}	50			50			50			V	I_F = 1.1 $I_{F(MAX)}$
Dynamic Impedance	'ZD		13			5			1.8		MΩ	V_F = 25V, f = 1 kHz
Knee Impedance	'ZK		1			0.4			0.17		MΩ	V_F = 25V, f = 1 kHz

At 25°C free air temperature Electrical Characteristics		J556			J556			Process NJ16	
		Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Regulator Current	I_F	2.4	3	3.8	3.6	4.5	5.3	mA	V_F = 25V
Limiting Voltage	V_L		0.75	2.6		1.5	3	V	I_F = 0.9 $I_{F(MIN)}$
Peak Operating Voltage	V_{OP}	50			50			V	I_F = 1.1 $I_{F(MAX)}$
Dynamic Impedance	'ZD		1.0			0.6		MΩ	V_F = 25V, f = 1 kHz
Knee Impedance	'ZK		0.09			0.06		MΩ	V_F = 25V, f = 1 kHz

TO-92 Two-Lead Package
Dimensions in Inches (mm)

Pin Configuration
1 Anode, 2 Cathode

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U553, U554, U555, U556, U557

Current Regulator Diode

- Current Regulation
- Current Limiting
- Biasing

Absolute maximum ratings at T_A = 25°C.

Peak Operating Voltage	50 V
Continuous Reverse Gate Current	50 mA
Continuous Device Power Dissipation	360 mW
Power Derating	2.88 mW/°C

At 25°C free air temperature Electrical Characteristics		U553			U554			U555			Process NJ16	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Regulator Current	I_F	0.18	0.5	0.75	0.6	1	1.6	1.4	2	2.6	mA	V_F = 25V
Limiting Voltage	V_L		0.75	1.3		0.55	1.75		0.75	2.15	V	I_F = 0.8 $I_{F(MIN)}$
Peak Operating Voltage	V_{OP}	50			50			50			V	I_F = 1.1 $I_{F(MAX)}$
Dynamic Impedance	'ZD		13			5			1.8		MΩ	V_F = 25V (Pulsed)
Knee Impedance	'ZK		1			0.4			0.17		MΩ	V_F = 6V

At 25°C free air temperature Electrical Characteristics		U556			U556			Process NJ16	
		Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Regulator Current	I_F	2.4	3	3.8	3.6	4.5	5.3	mA	V_F = 25V
Limiting Voltage	V_L		0.75	2.6		1.5	3	V	I_F = 0.8 $I_{F(MIN)}$
Peak Operating Voltage	V_{OP}	50			50			V	I_F = 1.1 $I_{F(MAX)}$
Dynamic Impedance	'ZD		1			0.6		MΩ	V_F = 25V (Pulsed)
Knee Impedance	'ZK		0.09			0.06		MΩ	V_F = 6V

TO-18 Package

Dimensions in Inches (mm)

Pin Configuration

1 Cathode, 2 Omitted, 3 Anode

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VCR2N, VCR4N, VCR7N

N-Channel Silicon Voltage Controlled Resistor JFET

- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

Absolute maximum ratings at T_A = 25°C.

Reverse Gate Source & Reverse Gate Drain Voltage	– 15 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	2.4 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		VCR2N NJ72 Min	VCR2N NJ72 Max	VCR4N NJ16 Min	VCR4N NJ16 Max	Process Unit	Process Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 15		– 15		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 5		– 0.2	nA	V_{GS} = – 15V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1	– 3.5	– 3.5	– 7	V	I_D = – 1 µA, V_{DS} = 10V	
Dynamic Electrical Characteristics								
Drain Source ON Resistance	$r_{ds(on)}$	20	60	200	600	Ω	V_{GS} = ØV, I_D = ØA	f = 1 kHz
Drain Gate Capacitance	C_{dg}		7.5		3	pF	V_{DG} = 10V, I_S = ØA	f = 1 MHz
Source Gate Capacitance	C_{sg}		7.5		3	pF	V_{DG} = 10V, I_D = ØA	f = 1 MHz

At 25°C free air temperature: Static Electrical Characteristics		VCR7N NJ01 Min	VCR7N NJ01 Max	Process Unit	Process Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 15		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1	nA	V_{GS} = – 15V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 2.5	– 5	V	I_D = – 1 µA, V_{DS} = 10V	
Dynamic Electrical Characteristics						
Drain Source ON Resistance	$r_{ds(on)}$	4000	8000	Ω	V_{GS} = ØV, I_D = ØA	f = 1 kHz
Drain Gate Capacitance	C_{dg}		1.5	pF	V_{DG} = 10V, I_S = ØA	f = 1 MHz
Source Gate Capacitance	C_{sg}		1.5	pF	V_{DG} = 10V, I_D = ØA	f = 1 MHz

VCR2N & VCR4N
TO-18 Package
See Section G for Outline Dimensions
Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

VCR7N
TO-72 Package
See Section G for Outline Dimensions
Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

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VCR3P

P-Channel Silicon Voltage Controlled Resistor JFET

- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

Absolute maximum ratings at T_A = 5°C.

Reverse Gate Source & Reverse Gate Drain Voltage	15 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	2.4 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		VCR3P Min	VCR3P Max	Process PJ99 Unit	Process PJ99 Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	15		V	I_G = 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		20	nA	V_{GS} = 15V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	1	5	V	I_D = – 1 µA, V_{DS} = – 10V	
Dynamic Electrical Characteristics						
Drain Source ON Resistance	$r_{ds(on)}$	70	200	Ω	V_{GS} = ØV, I_D = ØA	f = 1 kHz
Drain Gate Capacitance	C_{dg}		25	pF	V_{DG} = 10V, I_S = ØA	f = 1 MHz
Source Gate Capacitance	C_{sg}		15	pF	V_{GS} = 10V, I_D = ØA	f = 1 MHz

TO-18 Package

Dimensions in Inches (mm)

Pin Configuration

1 Source, 2 Gate & Case, 3 Drain

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VCR11N

N-Channel Silicon Voltage Controlled Resistor JFET

- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

Absolute maximum ratings at T_A = 25°C.

Reverse Gate Source & Reverse Gate Drain Voltage	– 15 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	2.4 mW/°C

At 25°C free air temperature: Static Electrical Characteristics		VCR11N Min	VCR11N Max	Process NJ26 Unit	Process NJ26 Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.2	nA	V_{GS} = – 15V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 8	– 12	V	I_D = 1 µA, V_{DS} = – 10V	
Static Drain Source ON Resistance Ratio	$r_{DS(MIN)}$	.95	1		V_{DS} = 100 mV, r_{DS1} = 200Ω	
	$r_{DS(MAX)}$	.95	1		V_{GS1} = V_{GS2}, r_{DS1} = 2 kΩ	
Dynamic Electrical Characteristics						
Drain Source ON Resistance	$r_{ds(on)}$	70	200	Ω	V_{GS} = ØV, I_D = ØA	f = 1 kHz
Drain Gate Capacitance	C_{dg}		7.5	pF	V_{DG} = 10V, I_S = ØA	f = 1 MHz
Source Gate Capacitance	C_{sg}		7.5	pF	V_{GS} = 10V, I_D = ØA	f = 1 MHz

TO-71 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source , 2 Drain 1, 3 Gate 1,
5 Source 2, 6 Drain 2, 7 Gate 2

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Section D

Japanese JFET Equivalents

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Japanese Equivalent JFET Types

Silicon Junction Field-Effect Transistors

		Japanese	2SK17	2SK40	2SK59	2SK105
		InterFET	IFN17	IFN40	IFN59	IFN105
		Process	NJ16	NJ16	NJ16	NJ16
Parameters	Conditions	Unit Limit	N Channel	N Channel	N Channel	N Channel
BV_{GSS}	I_G = – 1.0 µA	V Min	– 20	– 50	– 30	– 50
I_{GSS}	V_{GS} = ( ), V_{DS} = Ø	nA Max	0.10 (–10 V)	1.0 (–30 V)	1.0 (–10 V)	1.0 (–30 V)
$V_{GS(off)}$	V_{DS} = ( ), I_D = 1.0 nA	V Min/Max	–0.5/–6.0 (10 V)	–0.4/–5.0 (15 V)	–0.4/–5.0 (10 V)	–0.25/–4.5 (5.0 V)
I_{DSS}	V_{DS} = ( ), V_{GS} = Ø	mA Min/Max	0.3/6.5 (10 V)	0.6/6.5 (15 V)	0.3/1.4 (10 V)	0.5/12 (5.0 V)
g_{fs}	V_{DS} = ( ), V_{GS} = Ø	mS Typ	2.0 (10 V)	2.0 (15 V)	1.5 (10 V)	2.1 (5.0 V)
C_{iss}	V_{GS} = ( ), V_{DS} = ( )	pF Typ	4.0 (Ø) (Ø)	4.0 (Ø) (15 V)		4.0 (Ø) (10 V)
C_{rss}	V_{GS} = ( ), V_{DS} = ( )	pF Typ	1.2 (– 10 V) (Ø)	1.2 (Ø) (15 V)		1.0 (Ø) (10 V)
		Package Configuration	TO-226AA	TO-226AA	TO-226AA	TO-226AA
		Pin Configuration	SGD	SGD	SGD	DGS

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Japanese Equivalent JFET Types

Silicon Junction Field-Effect Transistors

2SK113	2SK152	2SK363	2SJ44	Japanese	
IFN113	IFN152	IFN363	IFP44	InterFET	
NJ132	NJ132L	NJ450	PJ99	Process	
N Channel	N Channel	N Channel	P Channel	Unit Limit	Parameters
– 50	– 20	– 40	25	V Min	BV_{GSS}
1.0 (–20 V)	0.1 (–10 V)	1.0 (–30 V)	1.0 (10 V)	nA Max	I_{GSS}
– 0.3/–10 (20 V)	– 0.5/– 2.0 (–10 V)	– 0.3/– 1.2 (10 V)	– 0.2/–1.5 (–10 V)	V Min/Max	$V_{GS(off)}$
5.0/150 (20 V)	5.0/20 (10 V)	5.0/30 (10 V)	1.0/18 (–10 V)	mA Min/Max	I_{DSS}
20 (20 V)	30 (10 V)	60 (10 V)	9 (–10 V)	mS Typ	g_{fs}
10 (Ø) (20 V)	15 (Ø) (10 V)	75 (Ø) (10 V)	15 (Ø) (–10 V)	pF Typ	C_{iss}
3.0 (Ø) (15 V)	4.0 (Ø) (10 V)	15 (Ø) (10 V)	3 (Ø) (–10 V)	pF Typ	C_{rss}
TO-18	TO-18	TO-18	TO-18	Package Configuration	
SDG	SDG	DGS	DGS	Pin Configuration	

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IFN112

N-Channel Silicon Junction Field-Effect Transistor

- Low-Noise, High Gain
- Equivalent to Japanese 2SK112

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 50 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	360 mW
Power Derating	2.88 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IFN112		Process NJ132H		
Static Electrical Characteristics		**Min**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 50		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.1	nA	V_{DS} = ØV, V_{GS} = – 30V	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.25	– 1.2	V	V_{DS} = 15V, I_D = 100 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	1.2	9.0	mA	V_{DS} = 15V, V_{GS} = ØV	
Dynamic Electrical Characteristics						
Common Source Forward Transconductance	g_{fs}	7	34	mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
		Typ				
Common Source Input Capacitance	C_{iss}	12		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}	3		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Equivalent Short Circuit Input Noise Voltage	$\bar{e}_N$	2.5		nV/√Hz	V_{DS} = 10V, I_D = 5.0 mA	f = 1 kHz

TO-18 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

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IFN146

Dual N-Channel Silicon Junction Field-Effect Transistor

- Low-Noise Audio Amplifier
- Equivalent to Japanese 2SK146

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 40 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	375 mW
Power Derating	3 mW/°C
Storage Temperature Range	– 65°C to 200°C

At 25°C free air temperature:		IFN146			Process NJ450		
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 40			V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 1	nA	V_{GS} = – 30V, V_{DS} = ØV	
				– 1	µA	V_{GS} = – 30V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.3		– 1.2	V	V_{DS} = 10V, I_D = 1 µA	
Drain Saturation Current (Pulsed)	I_{DSS}			30	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics							
Common Source Forward Transconductance	g_{fs}	30	40		mS	V_{DS} = 10V, V_{GS} = ØV I_{DSS} = 5 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}			75	pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Common Source Reverse Transfer Capacitance	C_{rss}			15	pF	V_{DS} = 10V, I_D = ØA	f = 1 kHz
Noise Figure	NF		1		dB	V_{DS} = 10V, I_D = 5 mA R_G = 100Ω	f = 1 kHz
Differential Gate Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$			20	mV	V_{DS} = 10V, I_D = 5 mA	

TO-71 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Gate, 3 Drain,
5 Source, 6 Gate, 7 Drain

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IFN147

N-Channel Silicon Junction Field-Effect Transistor

- Low-Noise Audio Amplifier
- Equivalent to Japanese 2SK147

Absolute maximum ratings at T_A = 25°C

Reverse Gate Source & Reverse Gate Drain Voltage	– 40 V
Continuous Forward Gate Current	10 mA
Continuous Device Power Dissipation	300 mW
Power Derating	2.4 mW/°C

At 25°C free air temperature:		IFN147			Process NJ450		
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 40			V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}			– 1	nA	V_{GS} = – 30V, V_{DS} = ØV	
				– 1	µA	V_{GS} = – 30V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.3		– 1.2	V	V_{DS} = 10V, I_D = 1 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	5		30	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics							
Common Source Forward Transconductance	g_{fs}	30	40		mS	V_{DS} = 10V, V_{GS} = ØV I_{DSS} = 5 mA	f = 1 kHz
Common Source Input Capacitance	C_{iss}			75	pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Common Source Reverse Transfer Capacitance	C_{rss}			15	pF	V_{DS} = 10V, I_D = Ø	f = 1 Hz
Noise Figure	NF		1		dB	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
				10	dB	R_G = 100Ω	f = 100 Hz

TO-18 Package
Dimensions in Inches (mm)

Pin Configuration
1 Source, 2 Gate & Case, 3 Drain

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Section E

Small Outline (Surface Mount) Package Devices

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Small Outline (Surface Mount) Package Devices

N-Channel Silicon Junction Field-Effect Transistors

Device Type	BV_{GSS}		I_{GSS}		V_{GS} (OFF)				I_{DSS}		
					Limits		Conditions				
	Min (V)	@I_G (µA)	Max (nA)	@V_{GS} (V)	Min (V)	Max (V)	V_{DS} (V)	I_D (nA)	Min (mA)	Max (mA)	@V_{DS} (V)
SMP3369	– 40	– 1.0	– 1.0	– 30	—	– 6.5	20	1.0	0.5	2.5	30
SMP3370	– 40	– 1.0	– 1.0	– 30	—	– 3.2	20	1.0	0.1	0.6	30
SMP3458	– 50	– 1.0	– 1.0	– 30	—	– 7.8	20	1.0	3.0	15	20
SMP3459	– 50	– 1.0	– 1.0	– 30	—	– 3.4	20	1.0	0.8	4.0	20
SMP3460	– 50	– 1.0	– 1.0	– 30	—	– 1.8	20	1.0	0.2	1.0	20
SMP3819	– 25	– 1.0	– 2.0	– 15	—	– 8.0	15	2.0	2.0	20	15
SMP3821	– 50	– 1.0	– 1.0	– 30	—	– 4.0	10	1.0	0.5	2.5	15
SMP3822	– 50	– 1.0	– 1.0	– 30	—	– 6.0	10	1.0	2.0	10	15
SMP3823	– 30	– 1.0	– 1.0	– 20	—	– 8.0	10	1.0	4.0	20	15
SMP3824	– 50	– 1.0	– 1.0	– 30	—	– 8.0	15	0.5	4.0	20	15
SMP3966	– 30	– 1.0	– 1.0	– 20	– 4.0	– 6.0	10	10	2.0	—	20
SMP3967	– 30	– 1.0	– 1.0	– 20	– 2.0	– 5.0	20	1.0	2.5	10	20
SMP3967A	– 30	– 1.0	– 1.0	– 20	– 2.0	– 5.0	20	1.0	2.5	10	20
SMP3968	– 30	– 1.0	– 1.0	– 20	—	– 3.0	20	1.0	1.0	5.0	20
SMP3968A	– 30	– 1.0	– 1.0	– 20	—	– 3.0	20	1.0	1.0	5.0	20
SMP3969	– 30	– 1.0	– 1.0	– 20	—	– 1.7	20	1.0	0.4	2.0	20
SMP3969A	– 30	– 1.0	– 1.0	– 20	—	– 1.7	20	1.0	0.4	2.0	20
SMP3970	– 40	– 1.0	– 1.0	– 20	– 4.0	– 10	20	1.0	50.0	150	20
SMP3971	– 40	– 1.0	– 1.0	– 20	– 2.0	– 5.0	20	1.0	25.0	75	20
SMP3972	– 40	– 1.0	– 1.0	– 20	– 0.5	– 3.0	20	1.0	5.0	30	20
SMP4091	– 40	– 1.0	– 1.0	– 20	– 5.0	– 10	20	1.0	30.0	—	20
SMP4092	– 40	– 1.0	– 1.0	– 20	– 2.0	– 7.0	20	1.0	15.0	—	20
SMP4093	– 40	– 1.0	– 1.0	– 20	– 1.0	– 5.0	20	1.0	8.0	—	20
SMP4117	– 40	– 1.0	– 0.01	– 20	– 0.6	– 1.8	10	1.0	0.03	0.09	10
SMP4118	– 40	– 1.0	– 0.01	– 20	– 1.0	– 3.0	10	1.0	0.08	0.24	10
SMP4119	– 40	– 1.0	– 0.01	– 20	– 2.0	– 6.0	10	1.0	0.2	0.6	10
SMP4220	– 30	– 10	– 1.0	– 15	—	– 4.0	15	1.0	0.5	3.0	15
SMP4221	– 30	– 10	– 1.0	– 15	—	– 6.3	15	1.0	2.0	6.0	15
SMP4222	– 30	– 10	– 1.0	– 15	—	– 8.0	15	1.0	5.0	15	15
SMP4223	– 30	– 10	– 1.0	– 20	—	– 8.0	15	1.0	3.0	18	15
SMP4224	– 30	– 10	– 1.0	– 20	—	– 8.0	15	1.0	2.0	20	15
SMP4302	– 30	– 1.0	– 1.0	– 15	—	– 4.0	20	10	0.5	5.0	20
SMP4303	– 30	– 1.0	– 1.0	– 15	—	– 6.0	20	10	4.0	10	20
SMP4304	– 30	– 1.0	– 1.0	– 15	—	– 10	20	10	0.5	15	20
SMP4338	– 50	– 1.0	– 1.0	– 30	– 0.3	– 1.0	15	100	0.2	0.6	15
SMP4339	– 50	– 1.0	– 1.0	– 30	– 0.6	– 1.8	15	100	0.5	1.5	15

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	g_{fs}			C_{iss}		C_{rss}		r_{ds}	Process
	Min (mS)	Max (mS)	@V_{DS} (V)	Max (pF)	@V_{DS} (V) @[V_{GS}] (V)	Max (pF)	@V_{DS} (V) @[V_{GS}] (V)	Max (Ω)	
SMP3369	0.6	2.5	30	20	8.0	3.0	30	—	NJ16
SMP3370	0.3	2.5	30	20	8.0	3.0	30	—	NJ16
SMP3458	2.5	10	20	18	[–10]	5.0	30	—	NJ32
SMP3459	1.5	6.0	20	18	[– 8.0]	5.0	30	—	NJ16
SMP3460	0.8	4.5	20	18	[– 4.0]	5.0	30	—	NJ16
SMP3819	2.0	6.5	15	8.0	15	4.0	15	—	NJ32
SMP3821	1.5	4.5	15	6.0	15	2.0	15	—	NJ32
SMP3822	3.0	6.5	15	6.0	15	2.0	15	—	NJ32
SMP3823	3.5	6.5	15	6.0	15	2.0	15	—	NJ32
SMP3824	3.5	6.5	15	6.0	15	2.0	15	250	NJ32
SMP3966	—	—	—	6.0	20	1.5	[– 7.0]	220	NJ32
SMP3967	2.5	—	20	5.0	20	1.3	20	—	NJ26
SMP3967A	2.5	—	20	5.0	20	1.3	20	—	NJ26
SMP3968	2.0	—	20	5.0	20	1.3	20	—	NJ26
SMP3968A	2.0	—	20	5.0	20	1.3	20	—	NJ26
SMP3969	1.3	—	20	5.0	20	1.3	20	—	NJ16
SMP3969A	1.3	—	20	5.0	20	1.3	20	—	NJ16
SMP3970	—	—	—	25	20	6.0	[–12]	30	NJ132
SMP3971	—	—	—	25	20	6.0	[–12]	60	NJ132
SMP3972	—	—	—	25	20	6.0	[–12]	100	NJ132
SMP4091	—	—	—	16	20	5.0	[– 20]	30	NJ132
SMP4092	—	—	—	16	20	5.0	[– 20]	50	NJ132
SMP4093	—	—	—	16	20	5.0	[– 20]	80	NJ132
SMP4117	0.07	0.21	10	3.0	10	1.5	10	—	NJ01
SMP4118	0.08	0.25	10	3.0	10	1.5	10	—	NJ01
SMP4119	0.1	0.33	10	3.0	10	1.5	10	—	NJ01
SMP4220	1.0	4.0	15	6.0	15	2.0	15	—	NJ16
SMP4221	2.0	5.0	15	6.0	15	2.0	15	—	NJ16
SMP4222	2.5	6.0	15	3.0	15	2.0	15	—	NJ32
SMP4223	3.0	7.0	15	6.0	15	2.0	15	—	NJ32
SMP4224	2.0	7.5	15	6.0	15	2.0	15	—	NJ32
SMP4302	1.0	—	20	6.0	15	2.0	15	—	NJ26
SMP4303	2.0	—	20	6.0	20	2.0	20	—	NJ26
SMP4304	1.0	—	20	6.0	20	3.0	20	—	NJ26
SMP4338	0.6	1.8	15	6.0	20	3.0	20	2500	NJ16
SMP4339	0.8	2.4	15	7.0	15	3.0	15	1700	NJ16

Electrical Characteristics at T_A = 25°C

InterFET Corporation
1000 N. Shiloh Road, Garland, TX 75042
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Small Outline (Surface Mount) Package Devices

N-Channel Silicon Junction Field-Effect Transistors

Device Type	BV_{GSS}		I_{GSS}		V_{GS} (OFF) Limits		V_{GS} (OFF) Conditions		I_{DSS}		
	Min (V)	@I_G (µA)	Max (nA)	@V_{GS} (V)	Min (V)	Max (V)	V_{DS} (V)	I_D (nA)	Min (mA)	Max (mA)	@V_{DS} (V)
SMP4340	– 50	– 1.0	– 1.0	– 30	– 1.0	– 3.0	15	100	1.2	3.6	15
SMP4341	– 50	– 1.0	– 1.0	– 30	– 2.0	– 6.0	15	100	3.0	9.0	15
SMP4391	– 40	– 1.0	– 1.0	– 20	– 4.0	– 10	20	1.0	50	150	20
SMP4392	– 40	– 1.0	– 1.0	– 20	– 2.0	– 5.0	20	1.0	25	100	20
SMP4393	– 40	– 1.0	– 1.0	– 20	– 0.5	– 3.0	20	1.0	5.0	30	20
SMP4416	– 30	– 1.0	– 1.0	– 20	—	– 6.0	15	1.0	5.0	15	15
SMP4416A	– 35	– 1.0	– 1.0	– 20	– 2.5	– 6.0	15	1.0	5.0	15	15
SMP4856	– 40	– 1.0	– 1.0	– 20	– 4.0	– 10	15	1.0	50	—	15
SMP4856A	– 40	– 1.0	– 1.0	– 20	– 4.0	– 10	15	1.0	50	—	15
SMP4857	– 40	– 1.0	– 1.0	– 20	– 2.0	– 6.0	15	1.0	20	100	15
SMP4857A	– 40	– 1.0	– 1.0	– 20	– 2.0	– 6.0	15	1.0	20	100	15
SMP4858	– 40	– 1.0	– 1.0	– 20	– 0.8	– 4.0	15	1.0	8.0	80	15
SMP4858A	– 40	– 1.0	– 1.0	– 20	– 0.8	– 4.0	15	1.0	8.0	80	15
SMP4859	– 30	– 1.0	– 1.0	– 15	– 4.0	– 10	15	1.0	50	—	15
SMP4859A	– 30	– 1.0	– 1.0	– 15	– 4.0	– 10	15	1.0	50	—	15
SMP4860	– 30	– 1.0	– 1.0	– 15	– 2.0	– 6.0	15	1.0	20	100	15
SMP4860A	– 30	– 1.0	– 1.0	– 15	– 2.0	– 6.0	15	1.0	20	100	15
SMP4861	– 30	– 1.0	– 1.0	– 15	– 0.8	– 4.0	15	1.0	8.0	80	15
SMP4861A	– 30	– 1.0	– 1.0	– 15	– 0.8	– 4.0	15	1.0	8.0	80	15
SMP4867	– 40	– 1.0	– 1.0	– 30	– 0.7	– 2.0	20	1.0	0.4	1.2	20
SMP4868	– 40	– 1.0	– 1.0	– 30	– 1.0	– 3.0	20	1.0	1.0	3.0	20
SMP4869	– 40	– 1.0	– 1.0	– 30	– 1.8	– 5.0	20	1.0	2.5	7.5	20
SMP5078	– 30	– 1.0	– 1.0	– 20	– 0.5	– 8.0	15	1.0	4.0	25	15
SMP5103	– 25	– 1.0	– 1.0	– 15	– 0.5	– 4.0	15	1.0	1.0	8.0	15
SMP5104	– 25	– 1.0	– 1.0	– 15	– 0.5	– 4.0	15	1.0	2.0	6.0	15
SMP5105	– 25	– 1.0	– 1.0	– 15	– 0.5	– 4.0	15	1.0	5.0	15	15
SMP5163	– 25	– 1.0	– 10	– 15	– 0.4	– 8.0	15	1.0	1.0	40	15
SMP5245	– 30	– 1.0	– 1.0	– 20	– 1.0	– 6.0	15	10	5.0	15	15
SMP5246	– 30	– 1.0	– 1.0	– 20	– 0.5	– 4.0	15	10	1.5	7.0	15
SMP5247	– 30	– 1.0	– 1.0	– 20	– 1.5	– 8.0	15	10	8.0	24	15
SMP5248	– 30	– 1.0	– 5.0	– 20	– 1.0	– 8.0	15	10	4.0	20	15
SMP5358	– 40	– 1.0	– 1.0	– 20	– 0.5	– 3.0	15	100	0.5	1.0	15
SMP5359	– 40	– 1.0	– 1.0	– 20	– 0.8	– 4.0	15	100	0.6	1.6	15
SMP5360	– 40	– 1.0	– 1.0	– 20	– 0.8	– 4.0	15	100	1.5	3.0	15
SMP5361	– 40	– 1.0	– 1.0	– 20	– 1.0	– 6.0	15	100	2.5	5.0	15
SMP5362	– 40	– 1.0	– 1.0	– 20	– 2.0	– 7.0	15	100	4.0	8.0	15

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	g_{fs}			C_{iss}		C_{rss}		r_{ds}	Process
	Min (mS)	Max (mS)	@V_{DS} (V)	Max (pF)	@V_{DS} (V) @[V_{GS}] (V)	Max (pF)	@V_{DS} (V) @[V_{GS}] (V)	Max (Ω)	
SMP4340	1.3	3.0	15	7.0	15	3.0	15	1500	NJ16
SMP4341	2.0	4.0	15	7.0	15	3.0	15	800	NJ16
SMP4391	—	—	—	7.0	15	3.5	– 5	30	NJ132
SMP4392	—	—	—	14	20	3.5	[– 12]	60	NJ132
SMP4393	—	—	—	14	20	3.5	[– 7.0]	100	NJ132
SMP4416	4.5	7.5	15	4.5	15	1.2	15	—	NJ26
SMP4416A	4.5	7.5	15	4.5	15	1.2	15	—	NJ26
SMP4856	—	—	—	18	[–10]	8.0	[–10]	25	NJ132
SMP4856A	—	—	—	10	[–10]	4.0	[–10]	25	NJ132
SMP4857	—	—	—	18	[–10]	8.0	[–10]	40	NJ132
SMP4857A	—	—	—	10	[–10]	3.5	[–10]	40	NJ132
SMP4858	—	—	—	18	[–10]	8.0	[–10]	60	NJ132
SMP4858A	—	—	—	10	[–10]	3.5	[–10]	60	NJ132
SMP4859	—	—	—	18	[–10]	8.0	[–10]	25	NJ132
SMP4859A	—	—	—	10	[–10]	4.0	[–10]	25	NJ132
SMP4860	—	—	—	18	[–10]	8.0	[–10]	40	NJ132
SMP4860A	—	—	—	10	[–10]	3.5	[–10]	40	NJ132
SMP4861	—	—	—	18	[–10]	8.0	[–10]	60	NJ132
SMP4861A	—	—	—	10	10	3.5	10	60	NJ132
SMP4867	0.7	2.0	20	25	20	5.0	20	—	NJ16
SMP4868	1.0	3.0	20	25	20	5.0	20	—	NJ16
SMP4869	1.3	4.0	20	25	20	5.0	20	—	NJ16
SMP5078	4.0	—	15	6.0	15	2.0	15	—	NJ26
SMP5103	2.0	8.0	15	5.0	15	1.2	15	—	NJ26
SMP5104	3.5	7.5	15	5.0	15	1.2	15	—	NJ26
SMP5105	5.0	10	15	5.0	15	1.2	15	—	NJ26
SMP5163	2.0	9.0	15	12	15	3.0	15	—	NJ26
SMP5245	4.0	—	15	4.5	15	1.5	15	—	NJ26
SMP5246	2.5	—	15	4.5	15	1.5	15	—	NJ26
SMP5247	4.0	—	15	4.5	15	1.5	15	—	NJ26
SMP5248	3.0	—	15	6.0	15	2.0	15	—	NJ26
SMP5358	1.0	3.0	15	6.0	15	2.0	15	—	NJ16
SMP5359	1.2	3.6	15	6.0	15	2.0	15	—	NJ16
SMP5360	1.4	4.2	15	6.0	15	2.0	15	—	NJ16
SMP5361	1.5	4.5	15	6.0	15	2.0	15	—	NJ16
SMP5362	2.0	5.5	15	6.0	15	2.0	15	—	NJ32

Electrical Characteristics at T_A = 25°C

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N-Channel Silicon Junction Field-Effect Transistors

Device Type	BV_{GSS}		I_{GSS}		V_{GS} (OFF)				I_{DSS}		
					Limits		Conditions				
	Min (V)	@I_G (µA)	Max (nA)	@V_{GS} (V)	Min (V)	Max (V)	V_{DS} (V)	I_D (nA)	Min (mA)	Max (mA)	@V_{DS} (V)
SMP5363	– 40	– 1.0	– 1.0	– 20	– 2.5	– 8.0	15	100	7.0	14	15
SMP5364	– 40	– 1.0	– 1.0	– 20	– 2.5	– 8.0	15	100	9.0	18	15
SMP5397	– 25	– 1.0	– 1.0	– 15	– 1.0	– 6.0	10	1.0	10	30	10
SMP5398	– 25	– 1.0	– 1.0	– 15	– 1.0	– 6.0	10	1.0	5.0	40	10
SMP5457	– 25	– 10	– 1.0	– 15	– 0.5	– 6.0	15	10	1.0	5.0	15
SMP5458	– 25	– 10	– 1.0	– 15	– 1.0	– 7.0	15	10	2.0	9.0	15
SMP5459	– 25	– 10	– 1.0	– 15	– 2.0	– 8.0	15	10	4.0	16	15
SMP5484	– 25	– 1.0	– 1.0	– 20	– 0.3	– 3.0	15	10	1.0	5.0	15
SMP5485	– 25	– 1.0	– 1.0	– 20	– 0.5	– 4.0	15	10	4.0	10	15
SMP5486	– 25	– 1.0	– 1.0	– 20	– 2.0	– 6.0	15	10	8.0	20	15
SMP5555	– 25	– 1.0	– 1.0	– 15	—	– 12	12	10	15	—	15
SMP5556	– 30	– 1.0	– 1.0	– 15	– 0.2	– 4.0	15	1.0	0.5	2.5	15
SMP5557	– 30	– 1.0	– 1.0	– 15	– 0.8	– 5.0	15	1.0	2.0	5.0	15
SMP5558	– 30	– 1.0	– 1.0	– 15	– 1.5	– 6.0	15	1.0	4.0	10	15
SMP5638	– 30	– 10	– 1.0	– 15	—	– 12	15	1.0	50	—	20
SMP5639	– 30	– 10	– 1.0	– 15	—	– 8.0	15	1.0	25	—	20
SMP5640	– 30	– 10	– 1.0	– 15	—	– 6.0	15	1.0	5.0	—	20
SMP5653	– 30	– 10	– 1.0	– 15	—	– 12	15	1.0	40	—	20
SMP5654	– 25	– 10	– 10	– 15	—	– 8.0	15	1.0	15	—	20
SMP5668	– 25	– 10	– 1.0	– 15	– 0.2	– 4.0	15	10	1.0	5.0	15
SMP5669	– 25	– 10	– 1.0	– 15	– 1.0	– 6.0	15	10	4.0	10	15
SMP5670	– 25	– 10	– 1.0	– 15	– 3.0	– 8.0	15	10	8.0	20	15
SMP5949	– 30	– 10	– 1.0	– 15	– 3.0	– 7.0	15	100	12	18	15
SMP5950	– 30	– 1.0	– 1.0	– 15	– 2.5	– 6.0	15	100	10	15	15
SMP5951	– 30	– 1.0	– 1.0	– 15	– 2.0	– 5.0	15	100	7.0	13	15
SMP5952	– 30	– 1.0	– 1.0	– 15	– 1.3	– 3.5	15	100	4.0	8.0	15
SMP5953	– 30	– 1.0	– 1.0	– 15	– 0.8	– 3.0	15	100	2.5	5.0	15
SMP6451	– 20	– 1.0	– 1.0	– 15	– 0.5	– 3.5	10	1.0	5.0	20	10
SMP6452	– 25	– 1.0	– 1.0	– 15	– 0.5	– 3.5	10	1.0	5.0	20	10
SMP6453	– 20	– 1.0	– 1.0	– 10	– 0.75	– 5.0	10	1.0	15	50	10
SMP6454	– 25	– 1.0	– 1.0	15	– 0.75	– 5.0	10	1.0	15	50	10
SMPBC264A	– 30	– 1.0	– 10	– 20	– 0.5	—	15	10	2.0	4.5	15
SMPBC264B	– 30	– 1.0	– 10	– 20	– 0.5	—	15	10	3.5	6.5	15
SMPBC264C	– 30	– 1.0	– 10	– 20	– 0.5	—	15	10	5.0	8.0	15
SMPBC264D	– 30	– 0.1	– 10	– 20	– 0.5	—	15	10	7.0	12	15
SMPBF244A	– 30	– 1.0	– 10	– 20	– 0.5	—	15	10	2.0	6.5	15
SMPBF244B	– 30	– 1.0	– 10	– 20	– 0.5	—	15	10	6.0	15	15

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	g_{fs}			C_{iss}		C_{rss}		r_{ds}	Process
	Min (mS)	Max (mS)	@V_{DS} (V)	Max (pF)	@V_{DS} (V) @[V_{GS}] (V)	Max (pF)	@V_{DS} (V) @[V_{GS}] (V)	Max (Ω)	
SMP5363	2.5	6.0	15	6.0	15	2.0	15	—	NJ32
SMP5364	2.7	6.5	15	6.0	15	2.0	15	—	NJ32
SMP5397	6.0	10	10	5.0	10	1.2	10	—	NJ26L
SMP5398	5.5	10	10	5.5	10	1.3	10	—	NJ26L
SMP5457	1.0	5.0	15	7.0	15	3.0	15	—	NJ32
SMP5458	1.5	5.5	15	7.0	15	3.0	15	—	NJ32
SMP5459	2.0	6.0	15	7.0	15	3.0	15	—	NJ32
SMP5484	3.0	6.0	15	5.0	15	1.0	15	—	NJ26
SMP5485	3.5	7.0	15	5.0	15	1.0	15	—	NJ26
SMP5486	4.0	8.0	15	5.0	15	1.2	15	—	NJ26
SMP5555	—	—	—	5.0	15	1.2	[–10]	—	NJ26
SMP5556	1.5	6.5	15	6.0	15	3.0	15	—	NJ16
SMP5557	1.5	6.5	15	6.0	15	3.0	15	—	NJ16
SMP5558	1.5	6.5	15	6.0	15	3.0	15	—	NJ16
SMP5638	—	—	—	10	[– 12]	4.0	[– 12]	30	NJ132
SMP5639	—	—	—	10	[– 12]	4.0	[– 12]	60	NJ72
SMP5640	—	—	—	10	[– 12]	4.0	[– 12]	100	NJ72
SMP5653	—	—	—	10	[– 12]	3.5	[– 12]	50	NJ72
SMP5654	—	—	—	10	[– 8.0]	3.5	[– 8.0]	100	NJ72
SMP5668	1.0	—	15	7.0	15	3.0	15	—	NJ32
SMP5669	1.6	—	15	7.0	15	3.0	15	—	NJ32
SMP5670	2.0	—	15	7.0	15	3.0	15	—	NJ32
SMP5949	3.0	—	15	6.0	15	2.0	15	—	NJ32
SMP5950	3.0	—	15	6.0	15	2.0	15	—	NJ32
SMP5951	3.0	—	15	6.0	15	2.0	15	—	NJ32
SMP5952	1.0	—	15	6.0	15	2.0	15	—	NJ32
SMP5953	1.0	—	15	6.0	15	2.0	15	—	NJ32
SMP6451	—	—	—	25	10	5.0	10	—	NJ132L
SMP6452	—	—	—	25	10	5.0	10	—	NJ132L
SMP6453	—	—	—	25	10	5.0	10	—	NJ132L
SMP6454	—	—	—	25	10	5.0	10	—	NJ132L
SMPBC264A	2.5	—	15	4.0	15	1.2	15	—	NJ26
SMPBC264B	3.0	—	15	4.0	15	1.2	15	—	NJ26
SMPBC264C	3.5	—	15	4.0	15	1.2	15	—	NJ26
SMPBC264D	4.0	—	15	4.0	15	1.2	15	—	NJ26
SMPBF244A	3.0	6.5	15	—	—	—	—	—	NJ26
SMPBF244B	3.0	6.5	15	—	—	—	—	—	NJ26

Electrical Characteristics at T_A = 25°C

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Device Type	BV_{GSS}		I_{GSS}		V_{GS} (OFF)				I_{DSS}		
					Limits		Conditions				
	Min (V)	@I_G (μA)	Max (nA)	@V_{GS} (V)	Min (V)	Max (V)	V_{DS} (V)	I_D(nA) [I_D](μA)	Min (mA)	Max (mA)	@V_{DS} (V)
SMPBF244C	– 30	– 1.0	– 5.0	– 20	– 0.5	– 8.0	15	10	12	25	15
SMPBF246A	– 25	– 1.0	– 5.0	– 15	– 0.6	– 14.5	15	10	30	80	15
SMPBF246B	– 25	– 1.0	– 5.0	– 15	– 0.6	– 14.5	15	10	60	140	15
SMPBF246C	– 25	– 1.0	– 5.0	– 15	– 0.6	– 14.5	15	10	110	250	15
SMPBF256A	– 30	– 1.0	– 5.0	– 20	– 0.5	– 7.5	15	10	3.0	7.0	15
SMPBF256B	– 30	– 1.0	– 5.0	– 20	– 0.5	– 7.5	15	10	6.0	13	15
SMPBF256C	– 30	– 1.0	– 5.0	– 20	– 0.5	– 7.5	15	10	11	18	15
SMPJ108	– 25	– 1.0	– 3.0	– 15	– 3.0	– 10.0	5.0	[1.0]	80	—	15
SMPJ109	– 25	– 1.0	– 3.0	– 15	– 2.0	– 6.0	5.0	[1.0]	40	—	15
SMPJ110	– 25	– 1.0	– 3.0	– 15	– 0.5	– 4.0	5.0	[1.0]	10	—	15
SMPJ110A	– 25	– 1.0	– 3.0	– 15	– 0.5	– 4.0	5.0	[1.0]	10	—	15
SMPJ111	– 35	– 1.0	– 1.0	– 15	– 3.0	– 10	5.0	1.0	20	—	15
SMPJ111A	– 40	– 1.0	– 2.0	– 1.0	– 5.0	– 10	5.0	1.0	30	—	15
SMPJ112	– 35	– 1.0	– 1.0	– 15	– 1.0	– 5.0	5.0	1.0	5.0	—	15
SMPJ112A	– 40	– 1.0	– 2.0	– 1.0	– 2.0	– 7.0	5.0	1.0	15	—	15
SMPJ113	– 35	– 1.0	– 1.0	– 15	—	– 3.0	5.0	1.0	2.0	—	15
SMPJ113A	– 40	– 1.0	– 2.0	– 1.0	– 1.0	– 5.0	5.0	1.0	8.0	—	15
SMPJ201	– 40	– 1.0	– 1.0	– 20	– 0.3	– 1.5	20	10	0.2	1.0	20
SMPJ202	– 40	– 1.0	– 1.0	– 20	– 0.8	– 4.0	20	10	0.9	4.5	20
SMPJ203	– 40	– 1.0	– 1.0	– 20	– 2.0	– 10	20	10	4.0	20	20
SMPJ210	– 25	– 1.0	– 1.0	– 15	– 1.0	– 3.0	15	1.0	2.0	15	15
SMPJ211	– 25	– 1.0	– 1.0	– 15	– 25	– 4.5	15	1.0	7.0	20	15
SMPJ212	– 25	– 1.0	– 1.0	– 15	– 4.0	– 6.0	15	1.0	15	40	15
SMPJ230	– 40	– 1.0	– 1.0	– 30	– 0.5	– 3.0	20	1.0	0.7	3.0	20
SMPJ231	– 40	– 1.0	– 1.0	– 30	– 1.5	– 5.0	20	1.0	2.0	6.0	20
SMPJ232	– 40	– 1.0	– 1.0	– 30	– 3.0	– 6.0	20	1.0	5.0	10	20
SMPJ300A	– 25	– 1.0	– 1.0	– 15	– 1.5	– 3.0	10	1.0	4.0	9.0	10
SMPJ300B	– 25	– 1.0	– 1.0	– 15	– 2.0	– 4.0	10	1.0	7.0	15	10
SMPJ300C	– 25	– 1.0	– 1.0	– 15	– 2.5	– 5.0	10	1.0	12	25	10
SMPJ304	– 30	– 1.0	– 1.0	– 20	– 2.0	– 6.0	15	1.0	5.0	15	15
SMPJ305	– 30	– 1.0	– 1.0	– 20	– 0.5	– 3.0	15	1.0	1.0	8.0	15
SMPJ308	– 25	– 1.0	– 1.0	– 15	– 1.0	– 6.5	10	1.0	12	60	10
SMPJ309	– 25	– 1.0	– 1.0	– 15	– 1.0	– 4.0	10	1.0	12	30	10
SMPJ310	– 25	– 1.0	– 1.0	– 15	– 2.0	– 6.5	10	1.0	24	60	10
SMPU1897	– 40	– 1.0	– 1.0	– 20	– 5.0	– 10	20	1.0	30	—	20
SMPU1898	– 40	– 1.0	– 1.0	– 20	– 2.0	– 7.0	20	1.0	15	—	20
SMPU1899	– 40	– 1.0	– 1.0	– 20	– 1.0	– 5.0	20	1.0	8.0	—	20

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	g_{fs}			C_{iss}		C_{rss}		r_{ds}	Process
	Min (mS)	Max (mS)	@V_{DS} (V)	Max (pF)	@V_{DS} (V) @[V_{GS}] (V)	Max (pF)	@V_{DS} (V) @[V_{GS}] (V)	Max (Ω)	
SMPBF244C	3.5	6.5	15	—	—	—	—	—	NJ26
SMPBF246A	—	—	—	—	—	—	—	—	NJ132
SMPBF246B	—	—	—	—	—	—	—	—	NJ132
SMPBF246C	—	—	—	—	—	—	—	—	NJ132
SMPBF256A	4.5	—	15	4.5	15	1.2	15	—	NJ26
SMPBF256B	4.5	—	15	4.5	15	1.2	15	—	NJ26
SMPBF256C	4.5	—	15	4.5	15	1.2	15	—	NJ26
SMPJ108				85		15	[–10]	8	NJ450
SMPJ109				85		15	[–10]	12	NJ450
SMPJ110				85		15	[–10]	18	NJ450
SMPJ110A				85		15	[–10]	25	NJ450
SMPJ111	—	—	—	28	15	5.0	[–10]	30	NJ132
SMPJ111A	—	—	—	28	15	5.0	[–10]	30	NJ132
SMPJ112	—	—	—	28	15	5.0	[–10]	50	NJ132
SMPJ112A	—	—	—	28	15	5.0	[–10]	50	NJ72
SMPJ113	—	—	—	28	15	5.0	[–10]	100	NJ72
SMPJ113A	—	—	—	28	15	5.0	[–10]	80	NJ72
SMPJ201	0.5	—	20	4.0	20	1.0	20	—	NJ16
SMPJ202	1.0	—	20	4.0	20	1.0	20	—	NJ16
SMPJ203	1.5	—	20	6.0	20	1.2	20	—	NJ16
SMPJ210	4.0	12	15	—	—	—	—	—	NJ26L
SMPJ211	6.0	12	15	—	—	—	—	—	NJ26L
SMPJ212	7.0	12	15	—	—	—	—	—	NJ26L
SMPJ230	1.0	3.5	20	—	—	—	—	—	NJ16
SMPJ231	1.5	4.0	20	—	—	—	—	—	NJ16
SMPJ232	2.5	5.0	20	—	—	—	—	—	NJ16
SMPJ300A	4.5	9.0	10	5.5	10	1.7	10	—	NJ26L
SMPJ300B	4.5	9.0	10	5.5	10	1.7	10	—	NJ26L
SMPJ300C	4.5	9.0	10	5.5	10	1.7	10	—	NJ26L
SMPJ304	4.5	7.5	15	—	—	—	—	—	NJ26
SMPJ305	3.0	—	15	—	—	—	—	—	NJ26
SMPJ308	8.0	—	10	7.5	[–10]	3.5	[–10]	—	NJ72
SMPJ309	10	—	10	7.5	[–10]	3.5	[–10]	—	NJ72
SMPJ310	8.0	—	10	7.5	[–10]	3.5	[–10]	—	NJ72L
SMPU1897	—	—	—	16	20	3.5	20	30	NJ132
SMPU1898	—	—	—	16	20	3.5	20	50	NJ132
SMPU1899	—	—	—	16	20	3.5	20	80	NJ132

Electrical Characteristics at T_A = 25°C

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Small Outline (Surface Mount) Package Devices

P-Channel Silicon Junction Field-Effect Transistors

Device Type	BV_{GSS}		I_{GSS}		V_{GS} (OFF)				I_{DSS}		
					Limits		Conditions				
	Min (V)	@I_G (µA)	Max (nA)	@V_{GS} (V)	Min (V)	Max (V)	V_{DS} (V)	I_D (nA)	Min (mA)	Max (mA)	@V_{DS} (V)
SMP2608	30	1.0	10	5	1.0	4.0	– 5	– 1.0	– 0.9	– 4.5	– 5.0
SMP2609	30	1.0	10	5	1.0	4.0	– 5	– 1.0	– 2.0	– 10	– 5.0
SMP3329	20	10	10	10	—	6.0	– 15	– 10	– 1.0	– 3.0	– 10
SMP3330	20	10	10	10	—	6.0	– 15	– 10	– 2.0	– 6.0	– 10
SMP3331	20	10	10	10	—	8.0	– 15	– 10	– 5.0	– 15	– 10
SMP3332	20	10	10	10	—	6.0	– 15	– 10	– 1.0	– 6.0	– 10
SMP3820	20	10	20	10	—	8.0	– 10	– 10	– 0.3	– 15	– 10
SMP3993	25	1.0	1.0	15	4.0	9.5	– 10	– 1.0	– 10	—	– 10
SMP3994	25	1.0	1.0	15	1.0	5.5	– 10	– 1.0	– 2.0	—	– 10
SMP4381	25	1.0	1.0	15	1.0	5.0	– 15	– 1.0	– 3.0	– 12	– 15
SMP5018	30	1.0	2.0	15	—	10	– 15	– 1.0	– 10	—	– 20
SMP5019	30	1.0	2.0	15	—	5.0	– 15	– 1.0	– 5.0	—	– 20
SMP5020	25	1.0	1.0	15	0.3	1.5	– 15	– 1.0	– 0.3	– 1.2	– 15
SMP5021	25	1.0	1.0	15	0.5	2.5	– 15	– 1.0	– 1.0	– 3.5	– 15
SMP5033	20	10	10	15	0.3	2.5	– 15	– 1.0	– 0.3	– 3.5	– 15
SMP5114	30	1.0	0.5	20	5.0	10	– 15	– 1.0	– 30	– 90	– 18
SMP5115	30	1.0	0.5	20	3.0	6.0	– 15	– 1.0	—	– 60	– 15
SMP5116	30	1.0	0.5	20	1.0	4.0	– 15	– 1.0	– 5.0	– 25	– 15
SMP5460	40	10	5.0	20	0.75	6.0	– 15	– 1.0	– 1.0	– 5.0	– 15
SMP5461	40	10	5.0	20	1.0	7.5	– 15	– 1.0	– 2.0	– 9.0	– 15
SMP5462	40	10	5.0	20	1.8	9.0	– 15	– 1.0	– 4.0	– 16	– 15
SMPJ174	30	1.0	1.0	20	5.0	10	– 15	– 10	– 20	– 135	– 15
SMPJ175	30	1.0	1.0	20	3.0	6.0	– 15	– 10	– 7.0	– 70	– 15
SMPJ176	30	1.0	1.0	20	1.0	4.0	– 15	– 10	– 2.0	– 35	– 15
SMPJ177	30	1.0	1.0	20	0.8	2.25	– 15	– 10	– 1.5	– 20	– 15
SMPJ270	30	1.0	1.0	20	0.5	2.0	– 15	– 1.0	– 2.0	– 15	– 15
SMPJ271	30	1.0	1.0	20	1.5	4.5	– 15	– 1.0	– 6.0	– 50	– 15
SMPP1086	30	1.0	2.0	15	—	10	– 15	– 1.0	– 10	—	– 20
SMPP1087	30	1.0	2.0	15	—	5.0	– 15	– 1.0	– 5.0	—	– 20

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	g_{fs}			C_{iss}		C_{rss}		r_{ds}	Process
	Min (mS)	Max (mS)	@V_{DS} (V)	Max (pF)	@V_{DS} (V) @[V_{GS}] (V)	Max (pF)	@V_{DS} (V) @[V_{GS}] (V)	Max (Ω)	
SMP2608	1.0	—	– 5.0	17	– 5.4	—	—	—	PJ32
SMP2609	2.5	—	– 5.0	30	– 5.4	—	—	—	PJ32
SMP3329	—	—	—	20	– 10	—	—	—	PJ32
SMP3330	—	—	—	20	– 10	—	—	—	PJ32
SMP3331	—	—	—	20	– 10	—	—	—	PJ32
SMP3332	—	—	—	20	– 10	—	—	—	PJ32
SMP3820	0.8	5.0	10	32	– 10	16	– 10	—	PJ32
SMP3993	6.0	12	10	16	– 10	4.5	[10]	150	PJ99
SMP3994	4.0	10	10	16	– 10	4.5	[10]	300	PJ99
SMP4381	2.0	6.0	15	20	– 15	5.0	– 15	—	PJ32
SMP5018	—	—	—	45	– 15	10	[12]	75	PJ99
SMP5019	—	—	—	45	– 15	10	[7]	150	PJ99
SMP5020	1.0	3.5	15	25	– 15	7.0	15	—	PJ32
SMP5021	1.5	6.0	15	25	– 15	7.0	15	—	PJ32
SMP5033	1.0	5.0	10	25	– 15	7.0	15	—	PJ32
SMP5114	—	—	—	25	– 15	7.0	[12]	75	PJ99
SMP5115	—	—	—	25	– 15	7.0	[7.0]	100	PJ99
SMP5116	—	—	—	25	– 15	7.0	[5.0]	150	PJ99
SMP5460	1.0	5.0	15	7.0	– 15	3.0	15	—	PJ32
SMP5461	1.5	5.5	15	7.0	– 15	3.0	15	—	PJ32
SMP5462	2.0	6.0	15	7.0	– 15	3.0	15	—	PJ32
SMPJ174	—	—	—	—	—	—	—	85	PJ99
SMPJ175	—	—	—	—	—	—	—	125	PJ99
SMPJ176	—	—	—	—	—	—	—	250	PJ99
SMPJ177	—	—	—	—	—	—	—	300	PJ99
SMPJ270	6.0	15	–15	—	—	—	—	—	PJ99
SMPJ271	8.0	18	–15	—	—	—	—	—	PJ99
SMPP1086	—	—	—	45	– 15	10	[12]	75	PJ99
SMPP1087	—	—	—	45	– 15	10	[7.0]	150	PJ99

Electrical Characteristics at T_A = 25°C

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Semiconductor Databook

Section F

Geometry & Process Information

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NJ01 Process

Silicon Junction Field-Effect Transistor

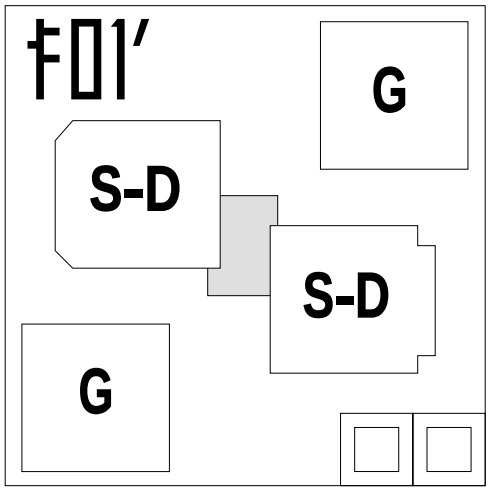
- Low-Current
- Low Gate Leakage Current
- High Input Impedance

Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ01 Process.

Datasheet	Datasheet
2N4117, 2N4117A	DPAD1, DPAD2
2N4118, 2N4118A	DPAD5, DPAD10
2N4119, 2N4119A	PAD1, PAD2
IFN421, IFN422	PAD5
IFN423, IFN424	VCR7N
IFN425, IFN426	



Die Size = 0.016" X 0.016"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		NJ01 Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 40	– 50		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 0.5	– 10	pA	V_{GS} = – 20V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.5		– 6	V	V_{DS} = 10V, I_D = 1 µA	
Drain Saturation Current (Pulsed)	I_{DSS}	0.03		0.6	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics							
Common Source Forward Transconductance	g_{fs}		175		µS	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		2		pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		0.9		pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 MHz

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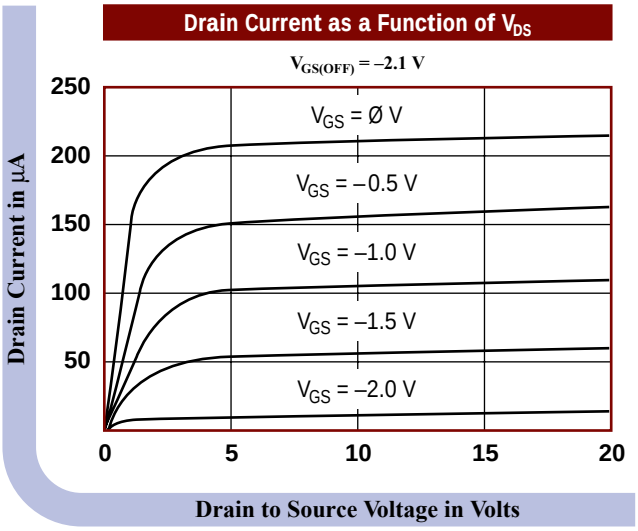
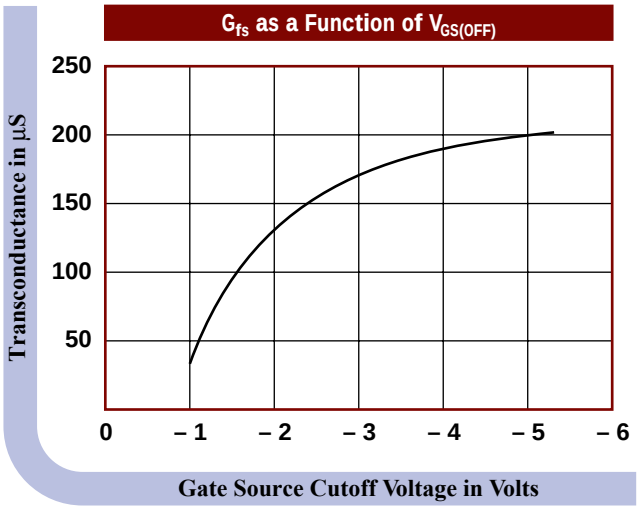
NJ01 Process

Silicon Junction Field-Effect Transistor

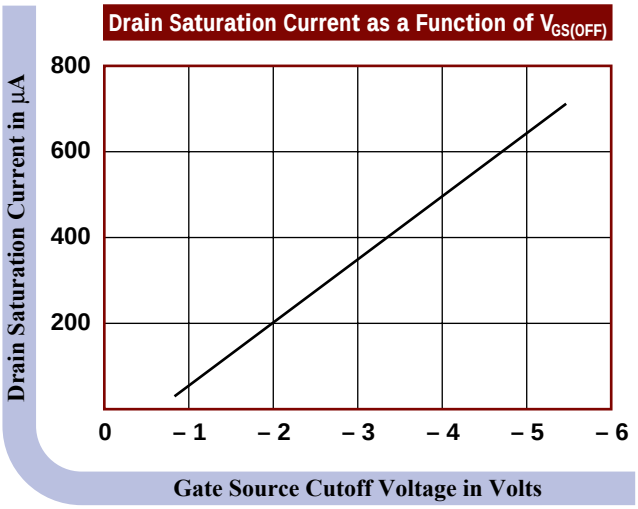
Drain Current as a Function of V_{DS}



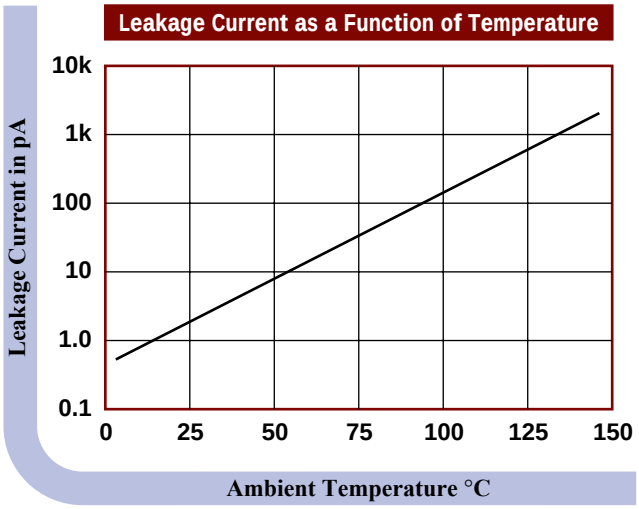
G_{fs} as a Function of $V_{GS(OFF)}$



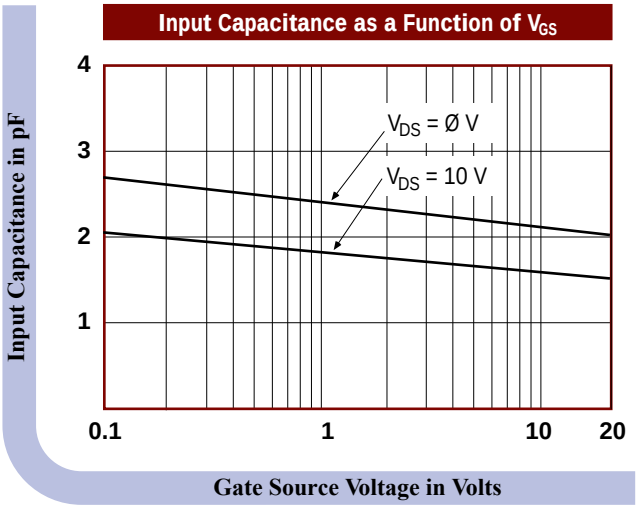
Drain Saturation Current as a Function of $V_{GS(OFF)}$



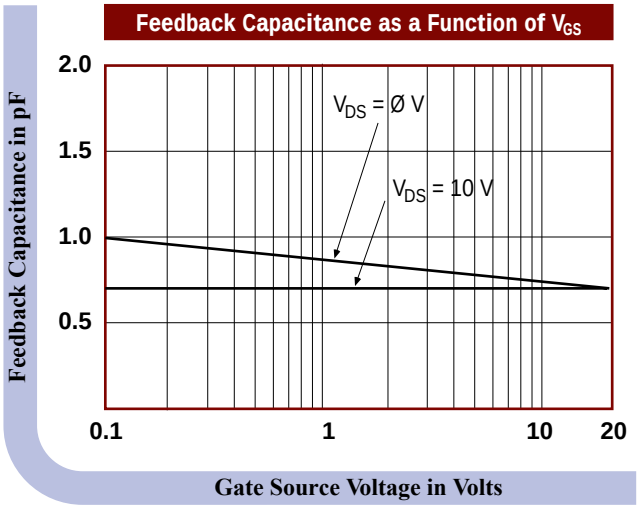
Leakage Current as a Function of Temperature



Input Capacitance as a Function of V_{GS}



Feedback Capacitance as a Function of V_{GS}



NJ14AL Process

Silicon Junction Field-Effect Transistor

- Low-Noise, High Gain Amplifier
- Rf AMP to 1.0 Ghz

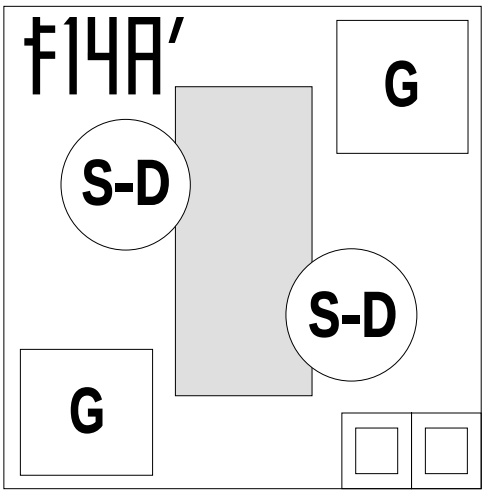
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ14AL Process.

Datasheet

IF140, IF140A
IF142



Die Size = 0.016" X 0.016"
All Round Bond Pads = 0.0028"
All Square Bond Pads = 0.004"
Substrate is also Gate.

At 25°C free air temperature:		NJ14AL Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 15	– 22		V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current	I_{GSS}		– 2.0	– 100	pA	V_{GS} = – 10V, V_{DS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.5		– 7	V	V_{GS} = 10V, I_D = 1 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	0.5	10	20	mA	V_{DS} = 10V, V_{GS} = ØV	
Dynamic Electrical Characteristics							
Common Source Forward Transconductance	g_{fs}		5.5		mS	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Common Source Input Capacitance	C_{iss}		2.3		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		0.5		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		4		nV/√HZ	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz

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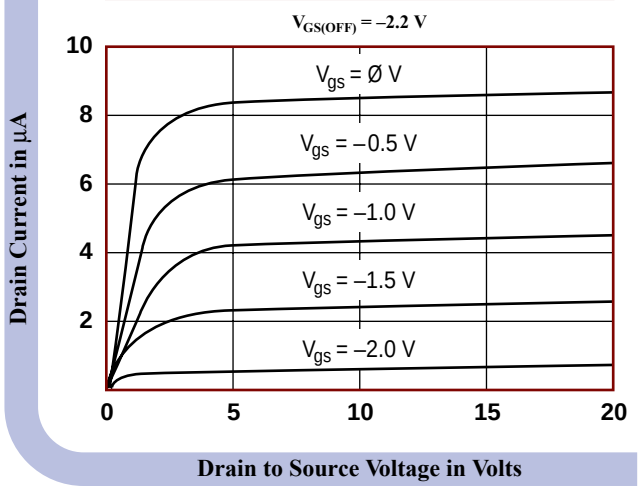
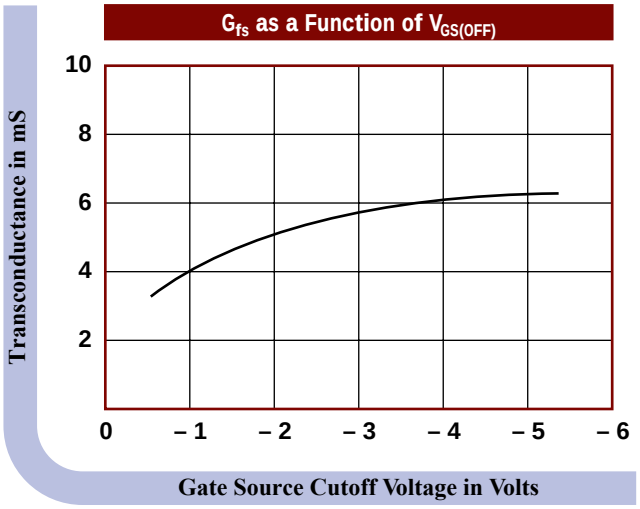
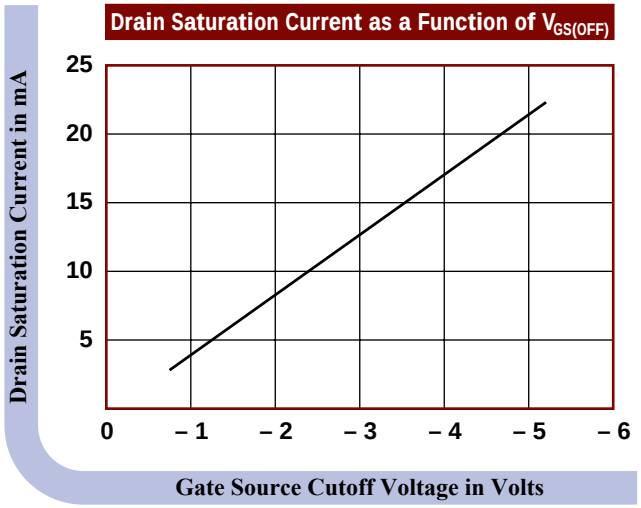
Drain Current as a Function of V_{DS}



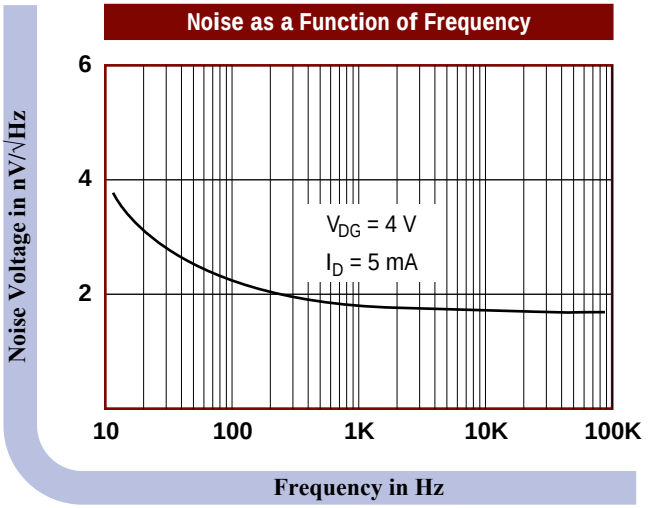
G_{fs} as a Function of $V_{GS(OFF)}$



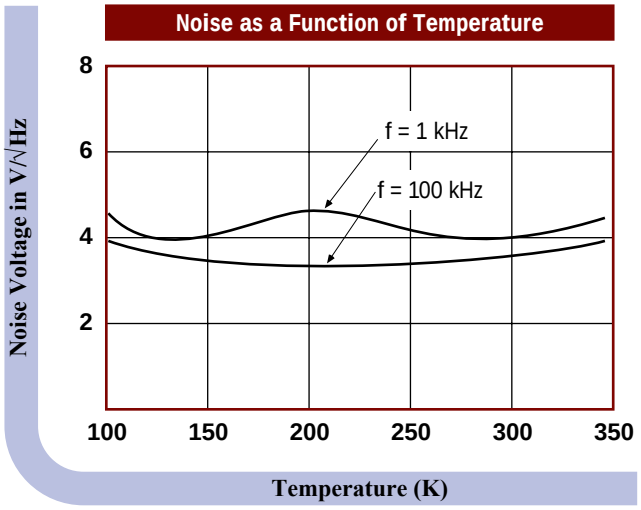
Drain Saturation Current as a Function of $V_{GS(OFF)}$



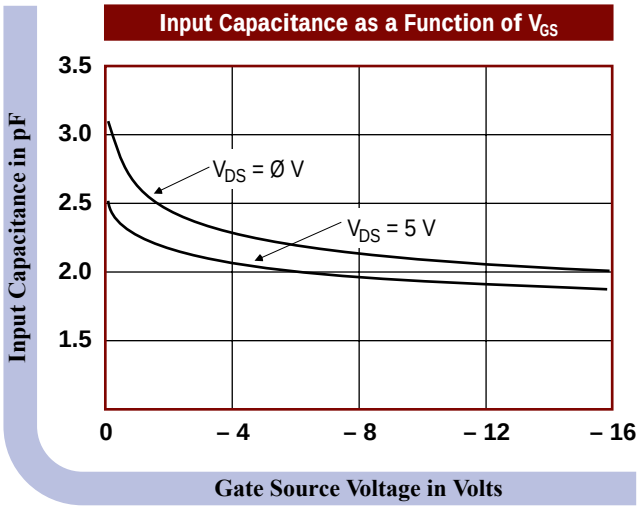
Noise as a Function of Frequency



Noise as a Function of Temperature



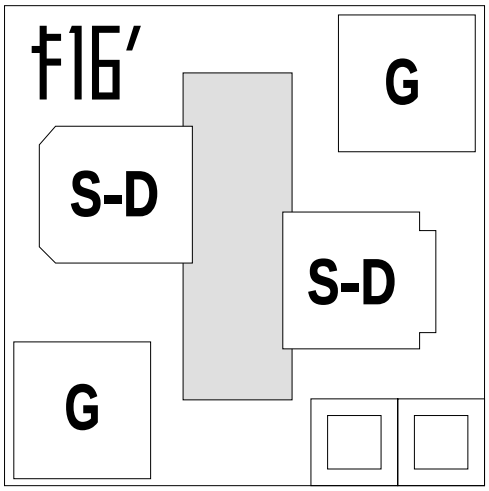
Input Capacitance as a Function of V_{GS}



NJ16 Process

Silicon Junction Field-Effect Transistor

- Low Current Switch
- General Purpose Amplifier
- High Breakdown Voltage



Die Size = 0.017" X 0.017"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ16 Process.

Datasheet	Datasheet	Datasheet
2N3954, 2N3955	2SK17, 2SK40	J504, J505
2N3956	2SK59, 2SK105	J506, J507
2N3957, 2N3958	IFN17, IFN40	J508, J509
2N4220, 2N4220A	IFN59, IFN105	J510, J511
2N4221, 2N4221A	J201, J202	J553, J554
2N4338, 2N4339	J203, J204	J555, J556
2N4340, 2N4341	J230, J231	J557
2N4867, 2N4867A	J232	U553, U554
2N4868, 2N4868A	J500, J501	U555, U556
2N4869, 2N4869A	J502, J503	U557
		VCR4N

At 25°C free air temperature:		NJ16 Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 50	– 60		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 10	– 100	pA	V_{GS} = – 30V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	0.2		9	mA	V_{DS} = 15V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.8		– 5.5	V	V_{DS} = 15V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance	g_{fs}		2.2		mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		3.5		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{rss}		1.2		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		6		nV/√HZ	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz

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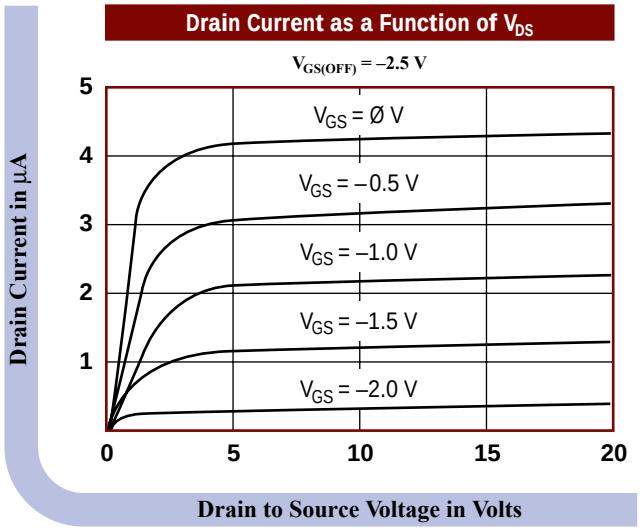
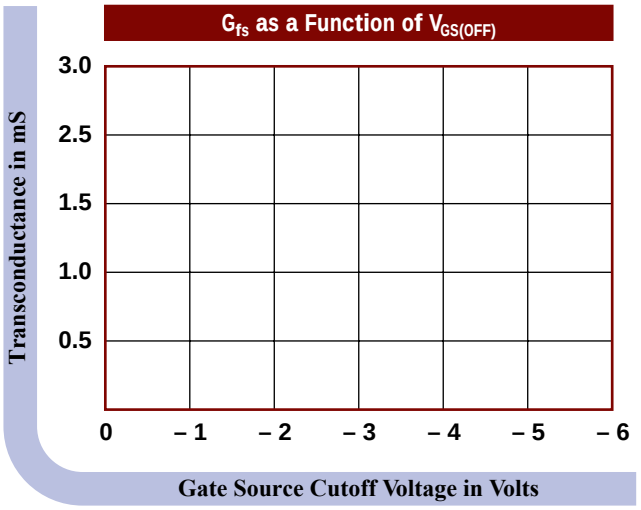
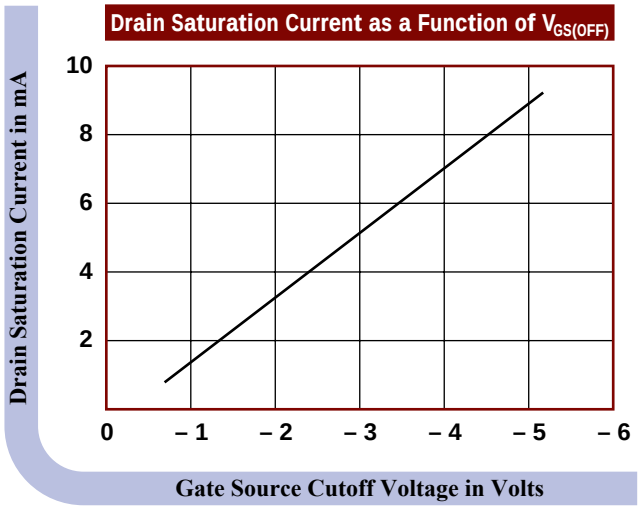
Drain Current as a Function of V_{DS}



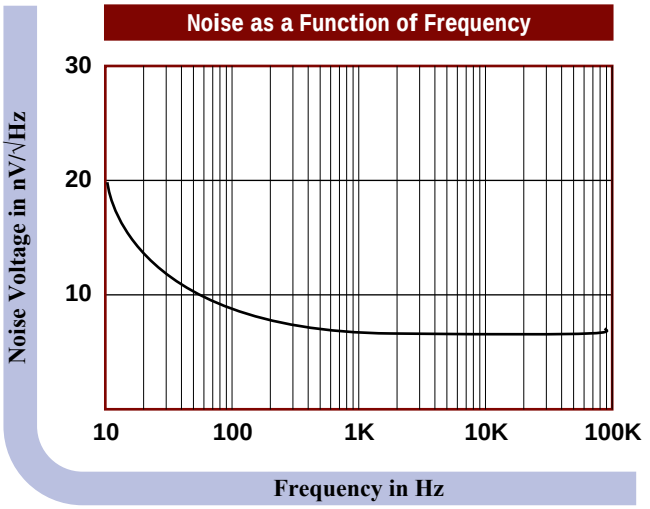
G_{fs} as a Function of $V_{GS(OFF)}$



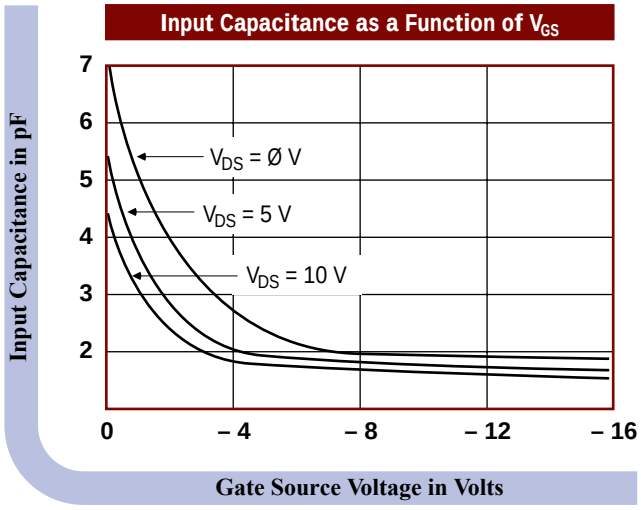
Drain Saturation Current as a Function of $V_{GS(OFF)}$



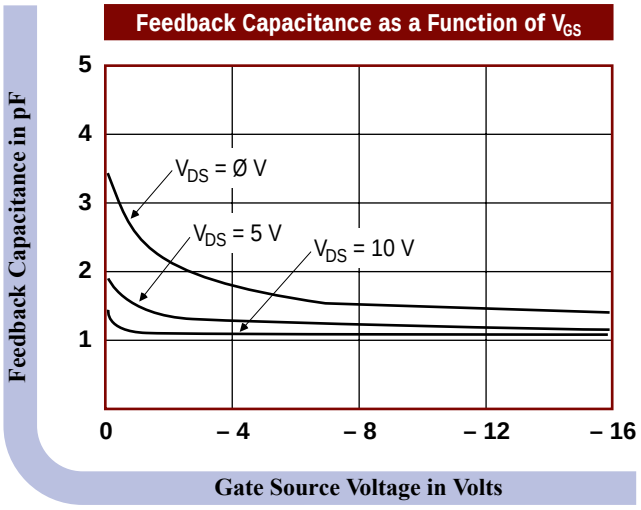
Noise as a Function of Frequency



Input Capacitance as a Function of V_{GS}



Feedback Capacitance as a Function of V_{GS}



NJ26 Process

Silicon Junction Field-Effect Transistor

- Low-Noise, High Gain Amplifier

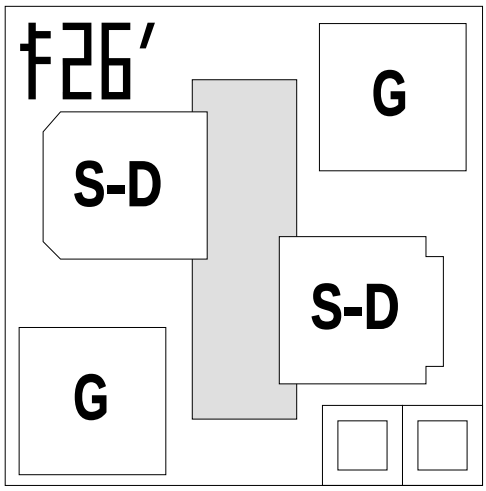
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ26A Process.

Datasheet

2N4416, 2N4416A
2N5484, 2N5485
2N5486
J304, J305
VCR11N



Die Size = 0.016" X 0.016"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		NJ26 Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 30	– 40		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 10	– 100	pA	V_{GS} = – 20V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	2		22	mA	V_{DS} = 15V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1		– 5	V	V_{DS} = 15V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance	g_{fs}		6		mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		4.3	5.0	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{rss}		1	1.5	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		4		nV/√HZ	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz

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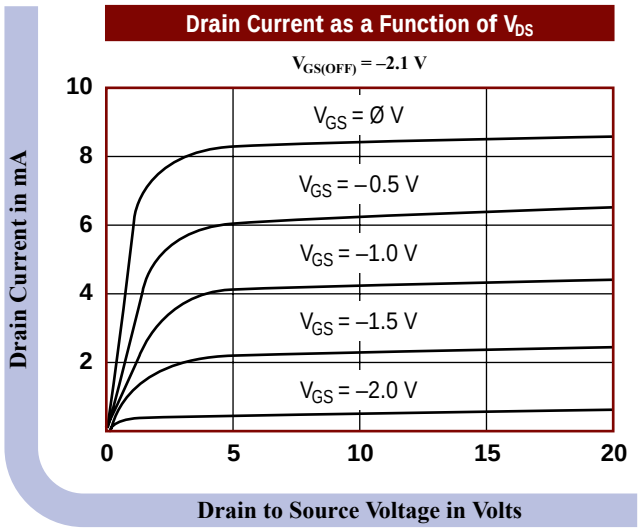
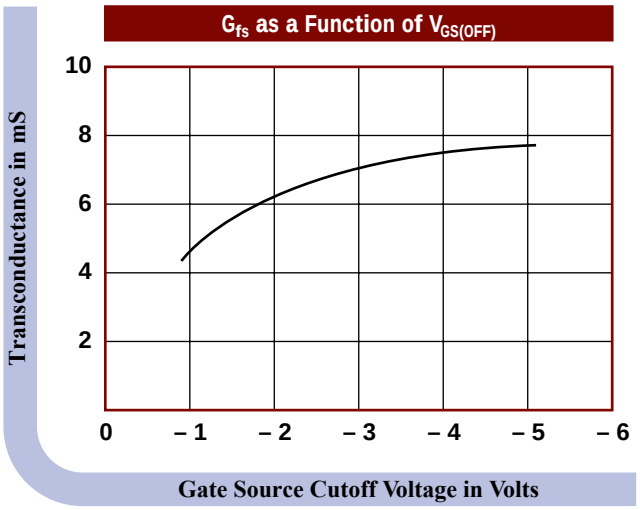
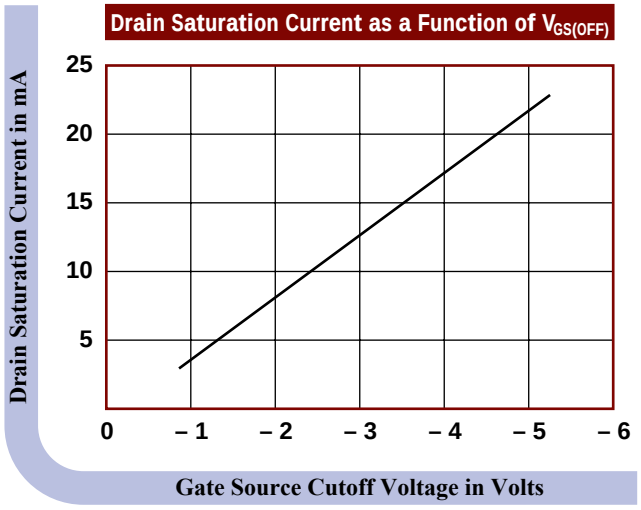
Drain Current as a Function of V_{DS}



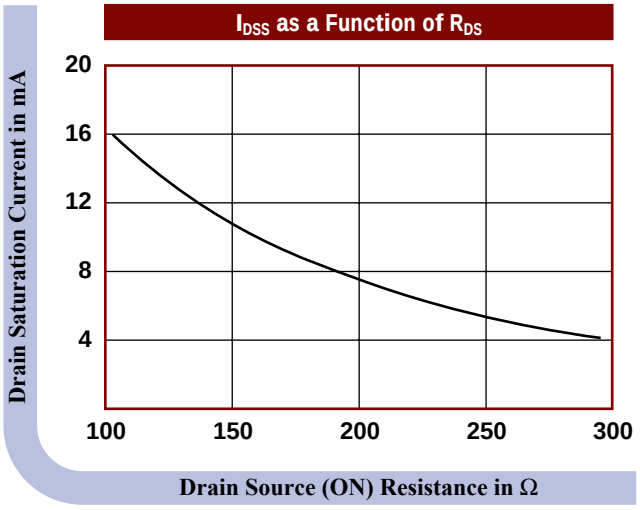
G_{fs} as a Function of $V_{GS(OFF)}$



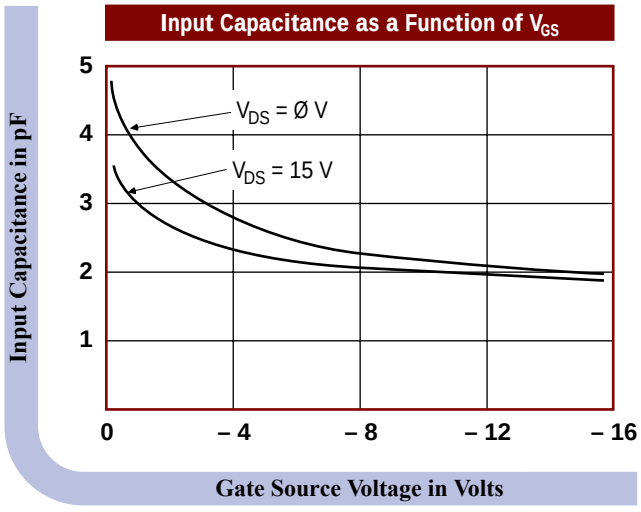
Drain Saturation Current as a Function of $V_{GS(OFF)}$



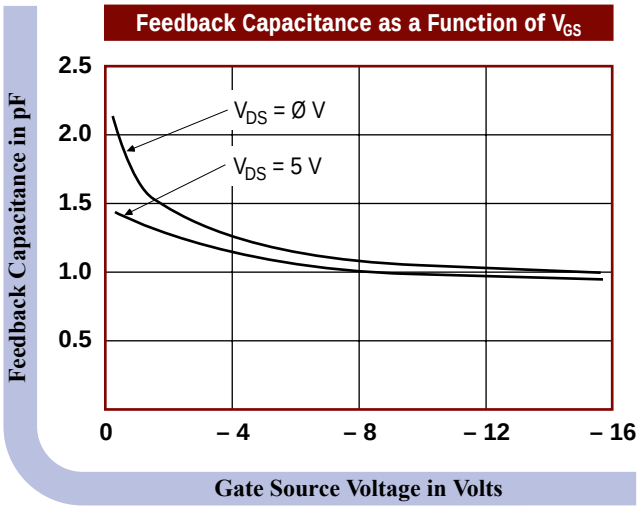
I_{DSS} as a Function of R_{DS}



Input Capacitance as a Function of V_{GS}



Feedback Capacitance as a Function of V_{GS}



NJ26A Process

Silicon Junction Field-Effect Transistor

- Low-Noise, High Gain Amplifier

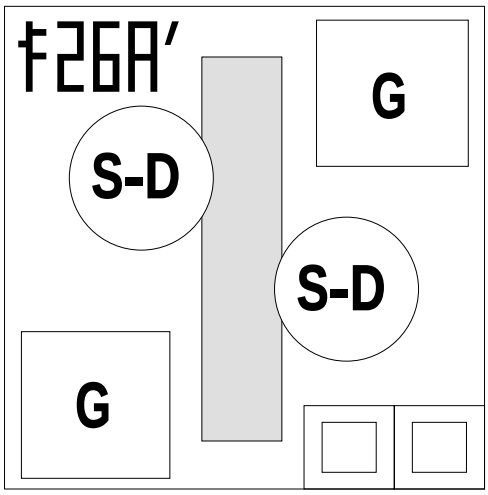
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ26A Process.

Datasheet

2N4416, 2N4416A



Die Size = 0.016" X 0.016"
All Round Bond Pads = 0.0028"
All Square Bond Pads = 0.004"
Substrate is also Gate.

At 25°C free air temperature:		NJ26A Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 30	– 40		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 10	– 100	pA	V_{GS} = – 20V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	2		22	mA	V_{DS} = 15V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1		– 5	V	V_{DS} = 15V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance	g_{fs}		6		mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		4	4.5	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{rss}		1	1.2	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		4		nV/√HZ	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz

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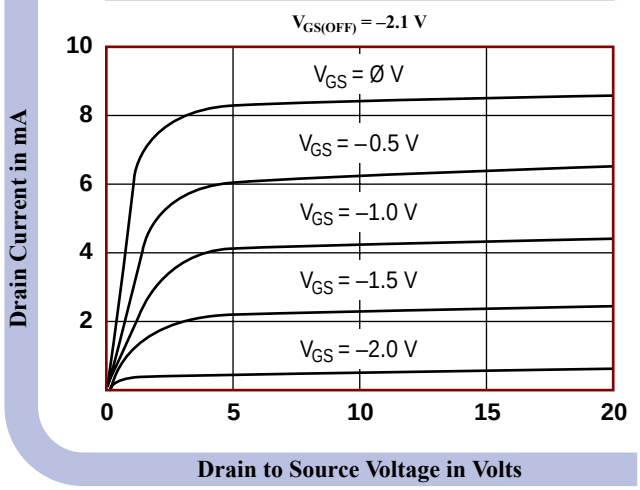
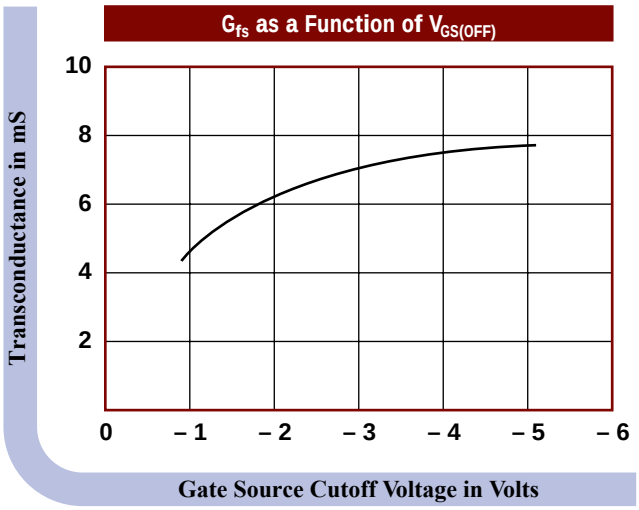
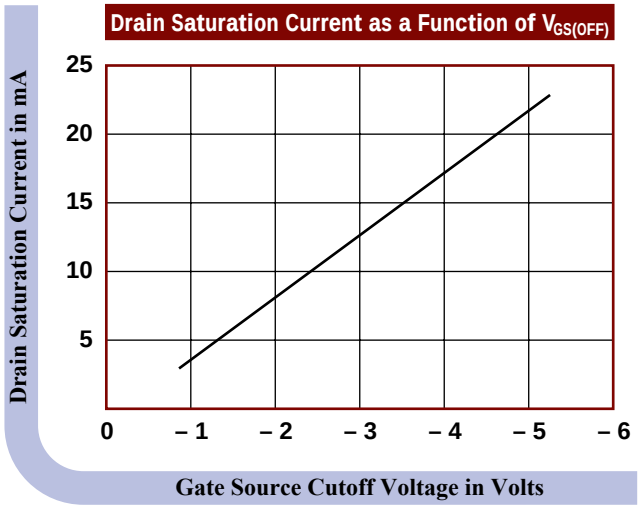
Drain Current as a Function of V_{DS}



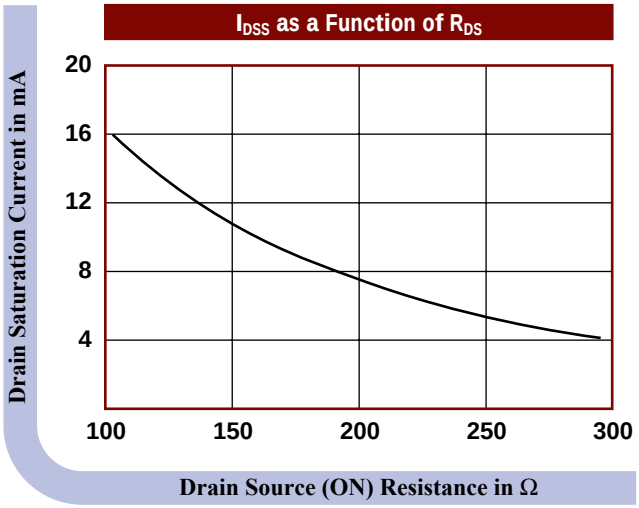
G_{fs} as a Function of $V_{GS(OFF)}$



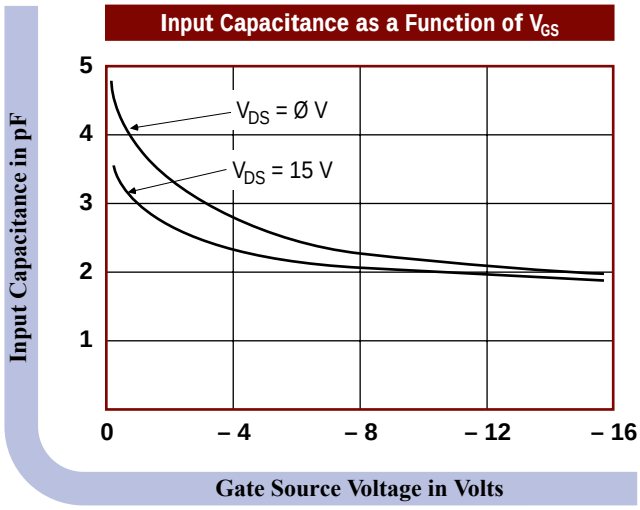
Drain Saturation Current as a Function of $V_{GS(OFF)}$



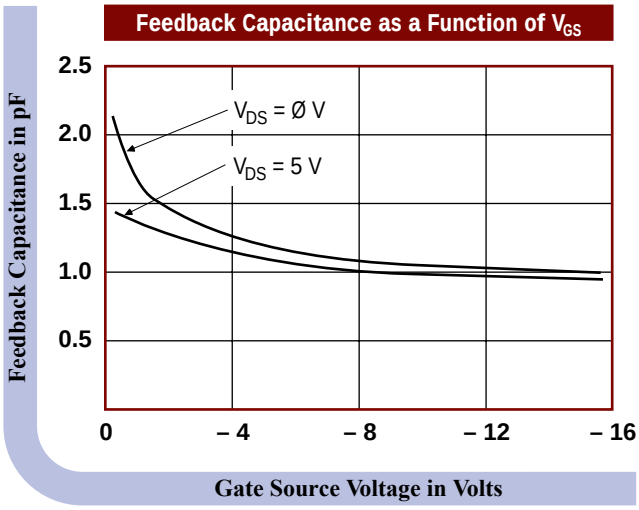
I_{DSS} as a Function of R_{DS}



Input Capacitance as a Function of V_{GS}



Feedback Capacitance as a Function of V_{GS}



NJ26L Process

Silicon Junction Field-Effect Transistor

- Low-Noise, High Gain Amplifier

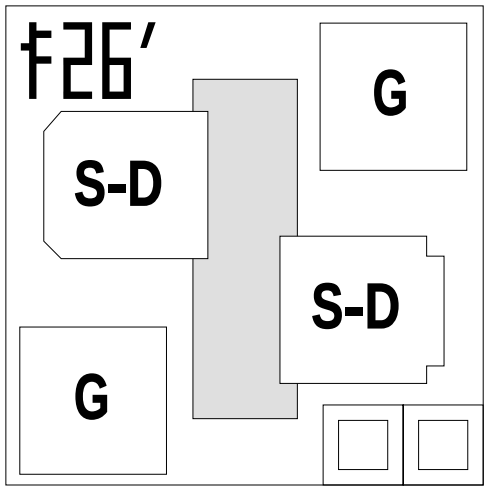
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ26L Process.

Datasheet

2N5397, 2N5398
J210, J211, J212



Die Size = 0.016" X 0.016"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		NJ26L Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25	– 30		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 10	– 100	pA	V_{GS} = – 15V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	2		40	mA	V_{DS} = 15V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.5		– 6	V	V_{DS} = 15V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance	g_{fs}		8		mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		5		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{rss}		1.5		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		2.5		nV/√HZ	V_{DS} = 15V, I_D = 5 mA	f = 1 kHz

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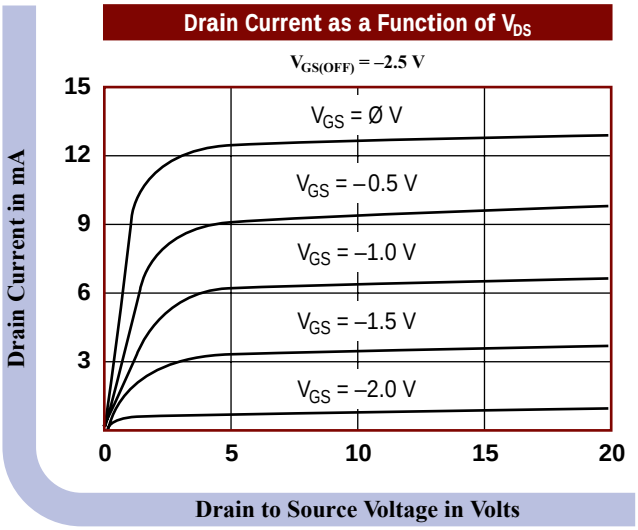
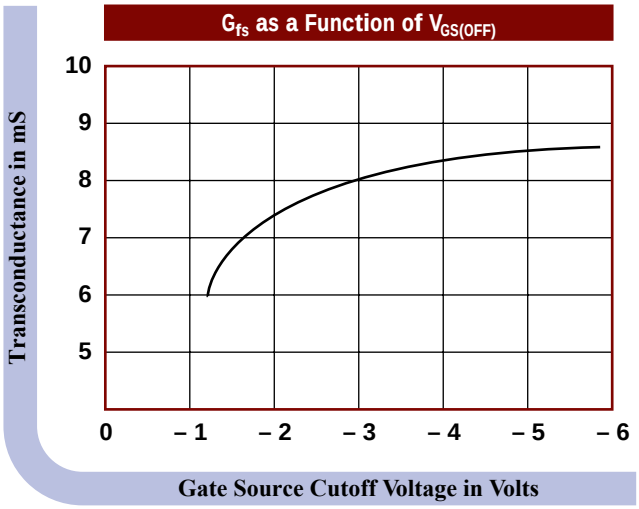
NJ26L Process

Silicon Junction Field-Effect Transistor

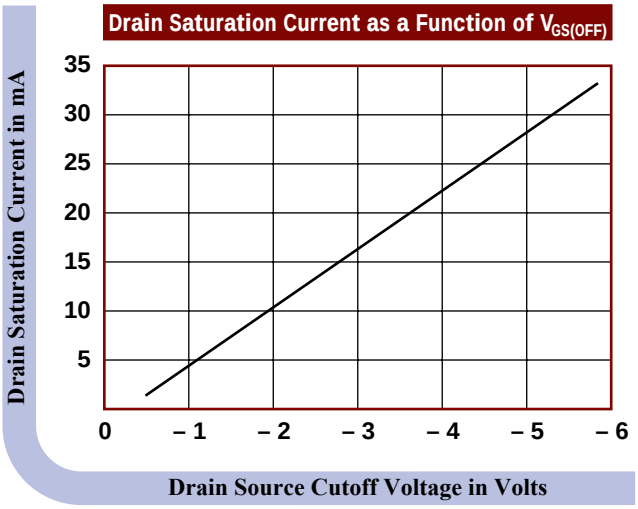
Drain Current as a Function of V_{DS}



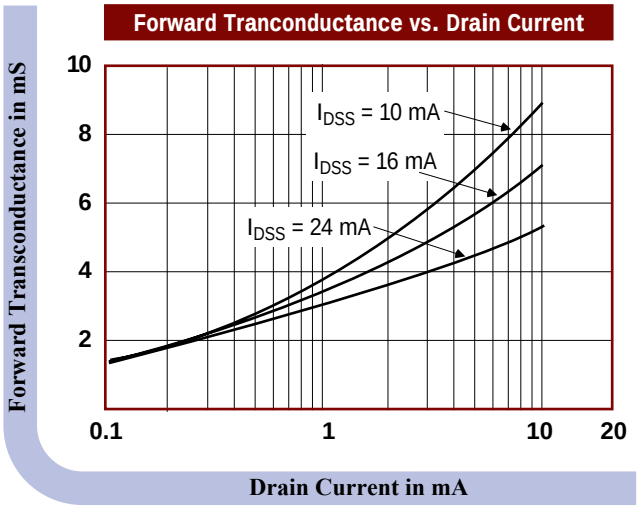
G_{fs} as a Function of $V_{GS(OFF)}$



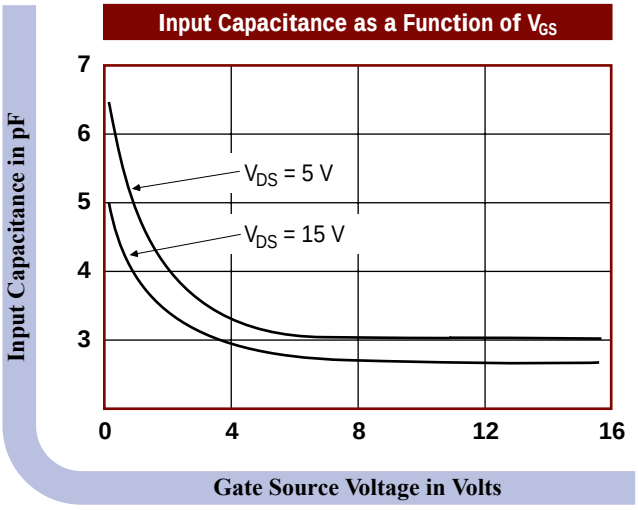
Drain Saturation Current as a Function of $V_{GS(OFF)}$



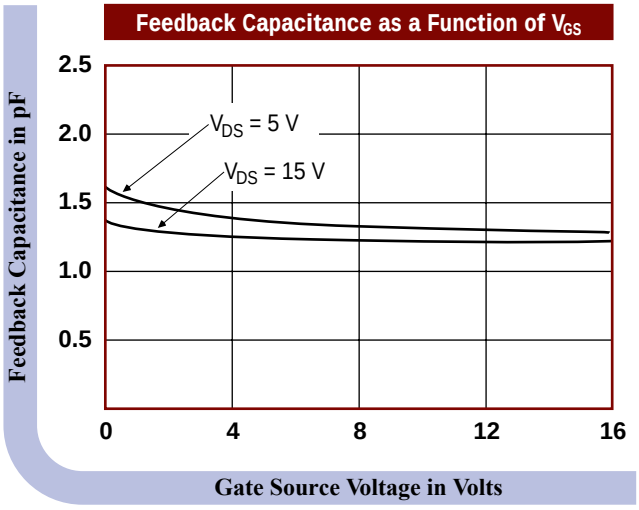
Forward Tranconductance vs. Drain Current



Input Capacitance as a Function of V_{GS}



Feedback Capacitance as a Function of V_{GS}



NJ30 Process

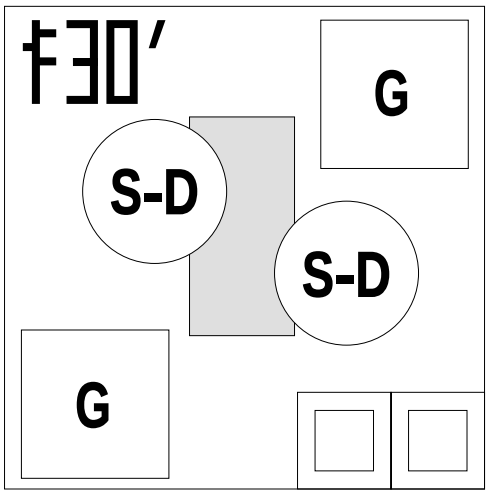
Silicon Junction Field-Effect Transistor

- Low-Noise, High Gain Amplifier

Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

This process available for customer-specified applications.



Die Size = 0.016" X 0.016"
All Round Bond Pads = 0.0028"
All Square Bond Pads = 0.004"
Substrate is also Gate.

At 25°C free air temperature:		NJ30 Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 30	– 40		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 10	– 100	pA	V_{GS} = – 20V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	2		22	mA	V_{DS} = 15V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1		– 5	V	V_{DS} = 15V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance	g_{fs}		6		mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		4.3	5	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{rss}		1	1.5	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		4		nV/√HZ	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz

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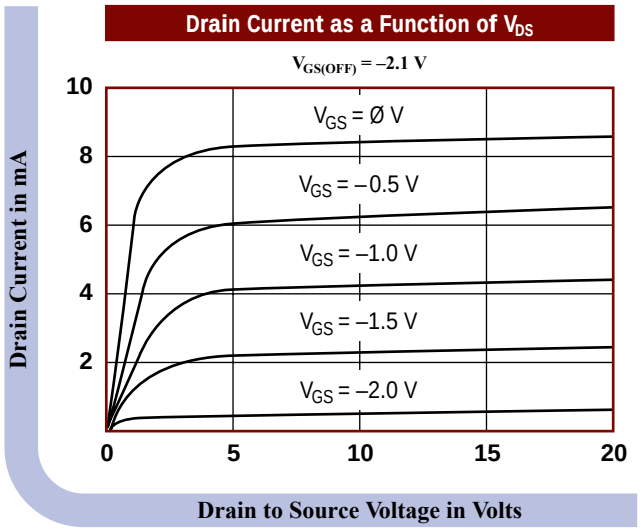
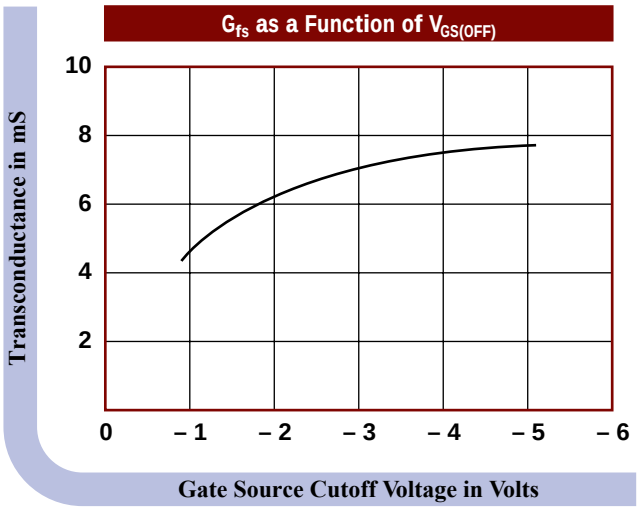
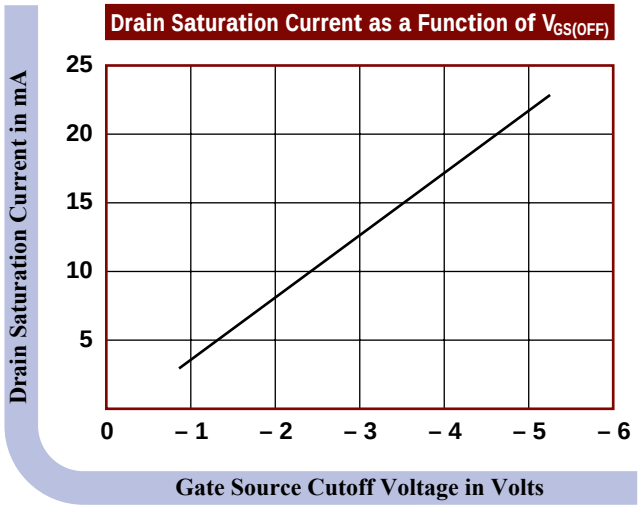
Drain Current as a Function of V_{DS}



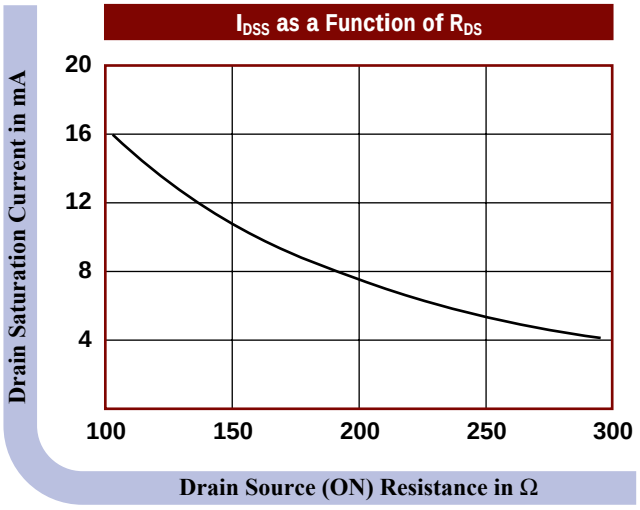
G_{fs} as a Function of $V_{GS(OFF)}$



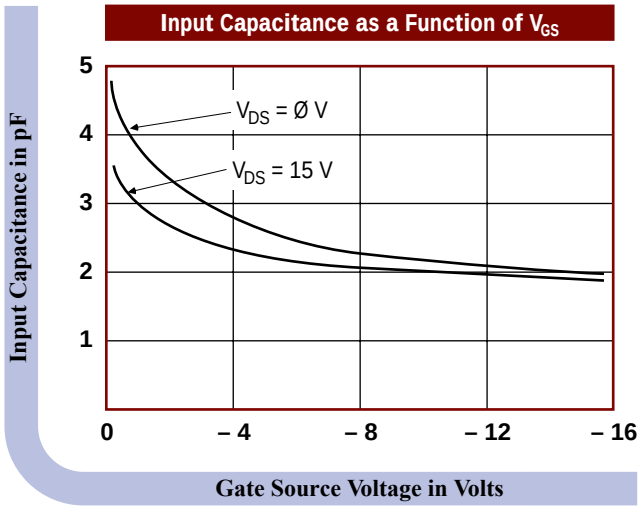
Drain Saturation Current as a Function of $V_{GS(OFF)}$



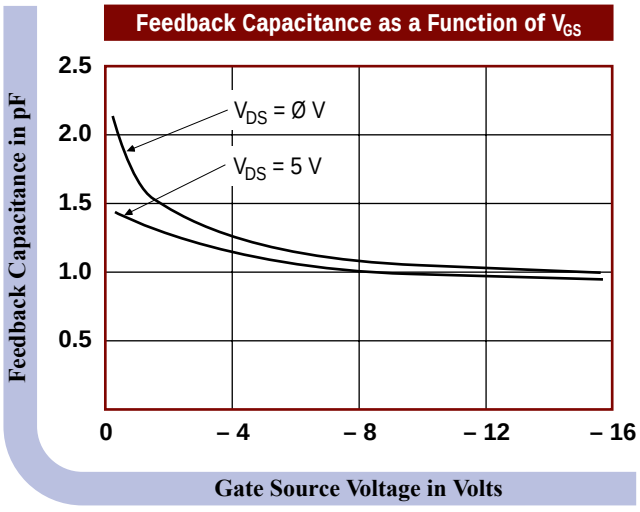
I_{DSS} as a Function of R_{DS}



Input Capacitance as a Function of V_{GS}



Feedback Capacitance as a Function of V_{GS}



NJ30L Process

Silicon Junction Field-Effect Transistor

- Low-Noise, High Gain Amplifier

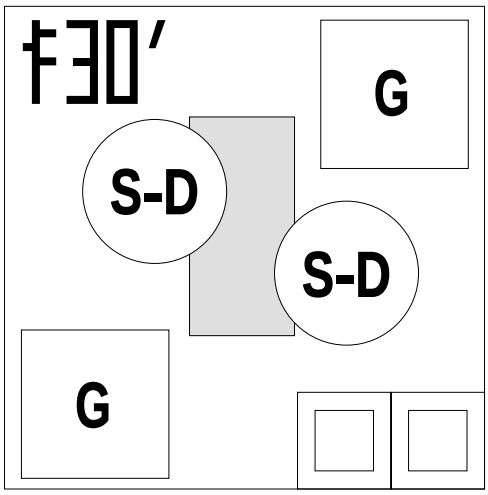
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ30L Process.

Datasheet

2N5911, 2N5912
IFN5911, IFN5912
SMP5911
SMP5912



Die Size = 0.016" X 0.016"
All Round Bond Pads = 0.0028"
All Square Bond Pads = 0.004"
Substrate is also Gate.

At 25°C free air temperature:		NJ30L Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25	– 30		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 10	– 100	pA	V_{GS} = – 15V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	2		40	mA	V_{DS} = 15V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.5		– 6	V	V_{DS} = 15V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance	g_{fs}		8		mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		5		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{rss}		1.5		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		2.5		nV/√HZ	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz

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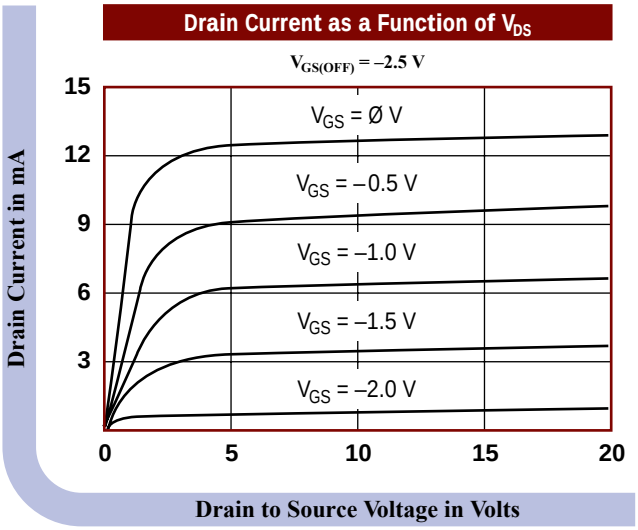
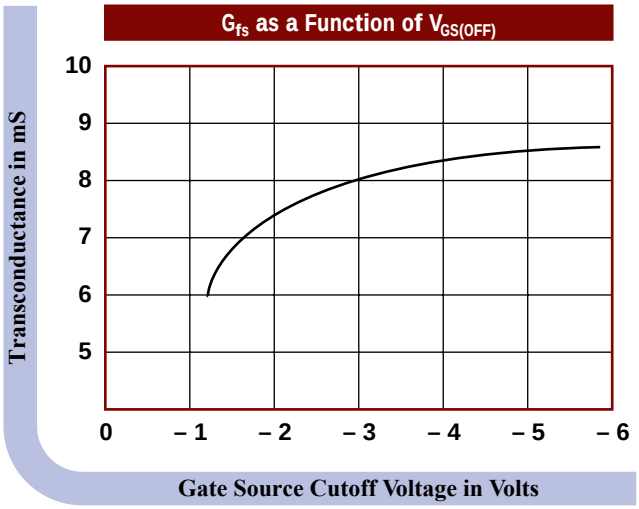
NJ30L Process

Silicon Junction Field-Effect Transistor

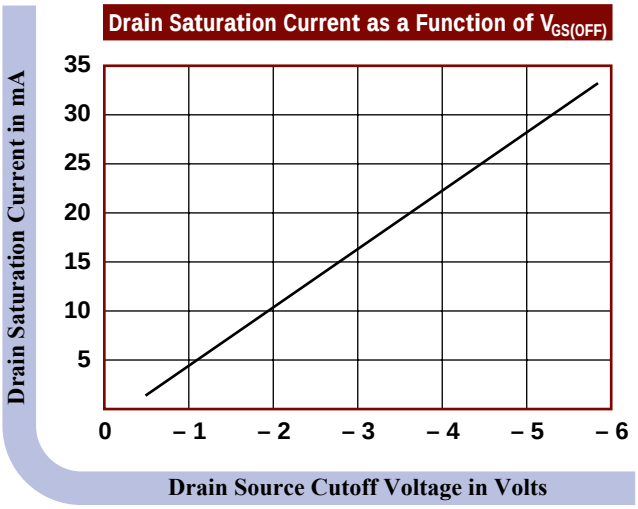
Drain Current as a Function of V_{DS}



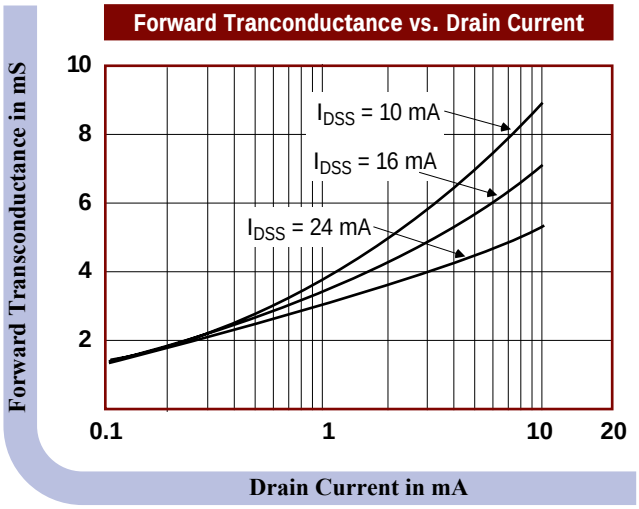
G_{fs} as a Function of $V_{GS(OFF)}$



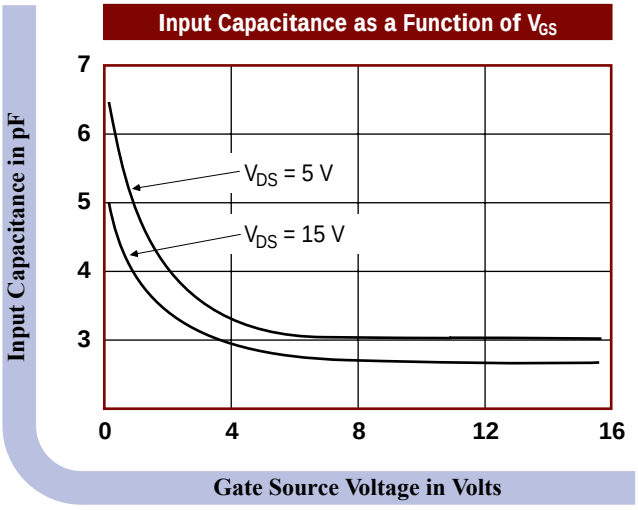
Drain Saturation Current as a Function of $V_{GS(OFF)}$



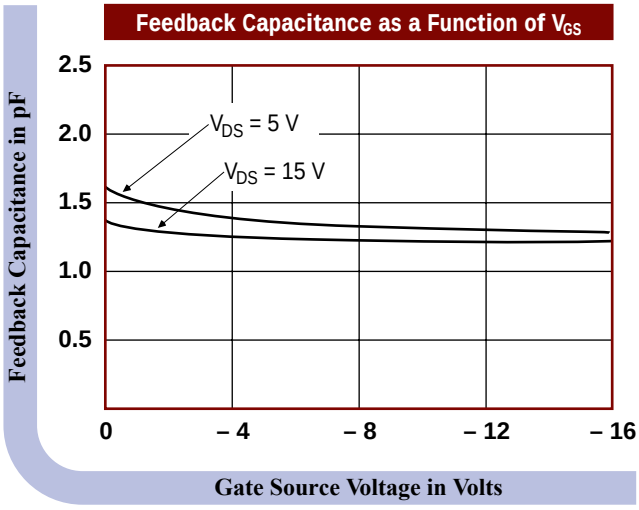
Forward Tranconductance vs. Drain Current



Input Capacitance as a Function of V_{GS}



Feedback Capacitance as a Function of V_{GS}



NJ32 Process

Silicon Junction Field-Effect Transistor

- General Purpose Amplifier

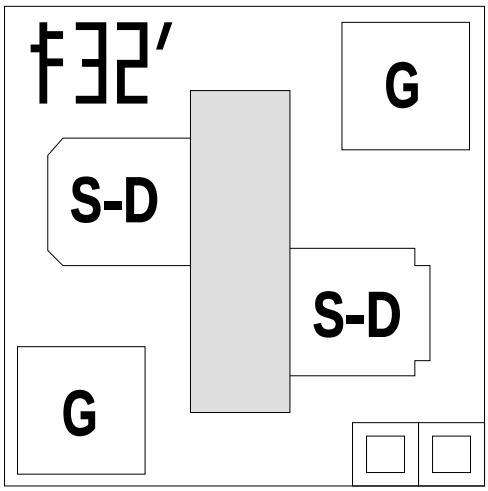
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ32 Process.

Datasheet

2N3821, 2N3822
2N3823, 2N3824
2N4222, 2N4222A



Die Size = 0.018" X 0.018"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		NJ32 Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25	– 50		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 10	– 100	pA	V_{GS} = – 15V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	1		22	mA	V_{DS} = 15V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.5		– 6	V	V_{DS} = 15V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance	g_{fs}		4		mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		6	7.0	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{rss}		1.3	3	pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		7		nV/√HZ	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz

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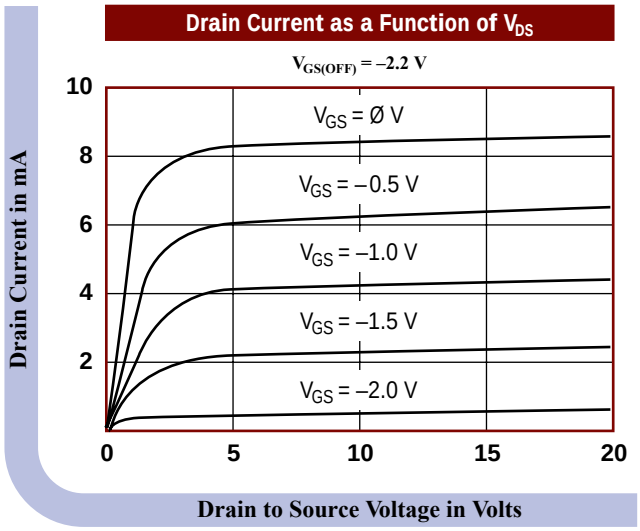
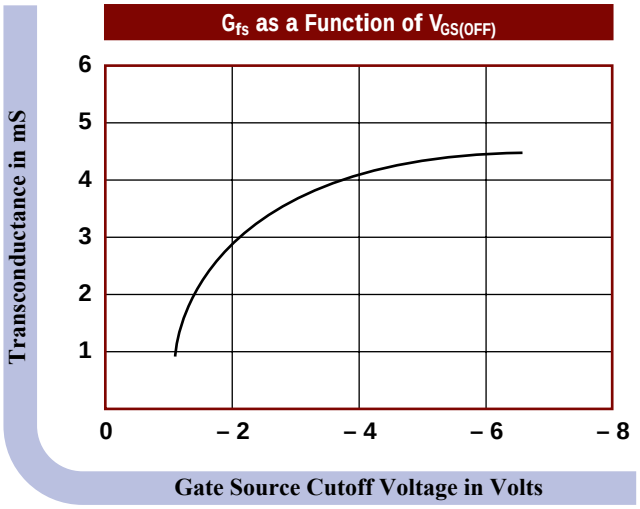
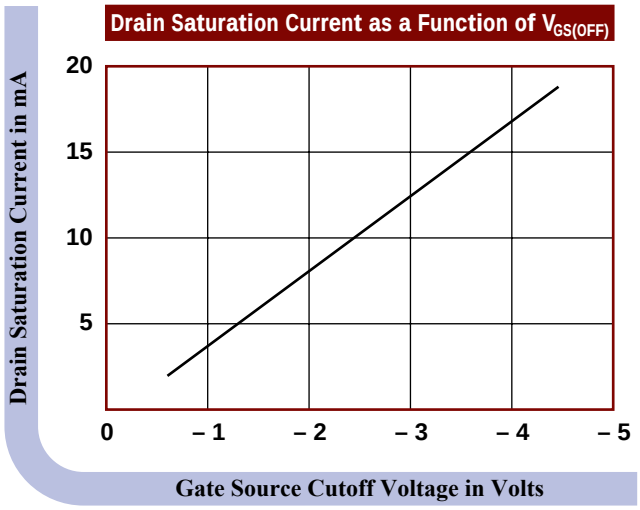
Drain Current as a Function of V_{DS}



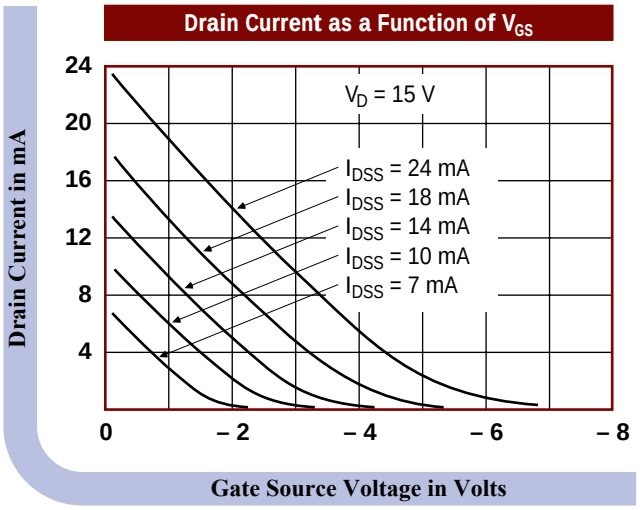
G_{fs} as a Function of $V_{GS(OFF)}$



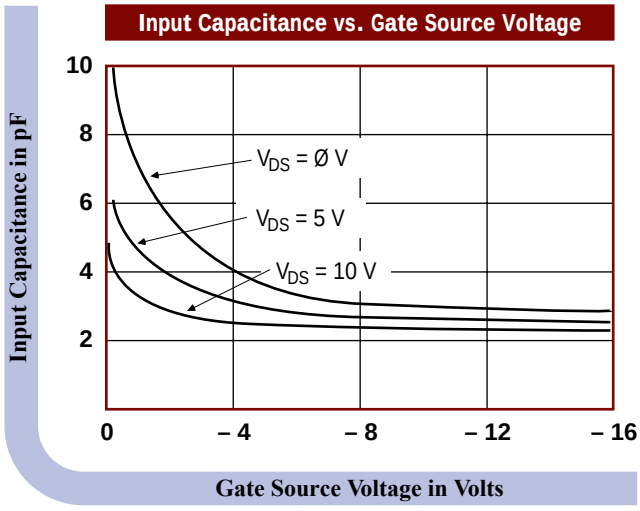
Drain Saturation Current as a Function of $V_{GS(OFF)}$



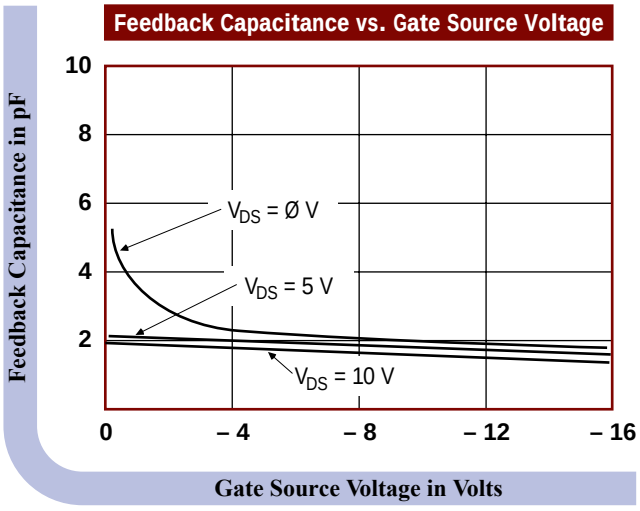
Drain Current as a Function of V_{GS}



Input Capacitance vs. Gate Source Voltage



Feedback Capacitance vs. Gate Source Voltage



PJ32 Process

Silicon Junction Field-Effect Transistor

- General Purpose Amplifier

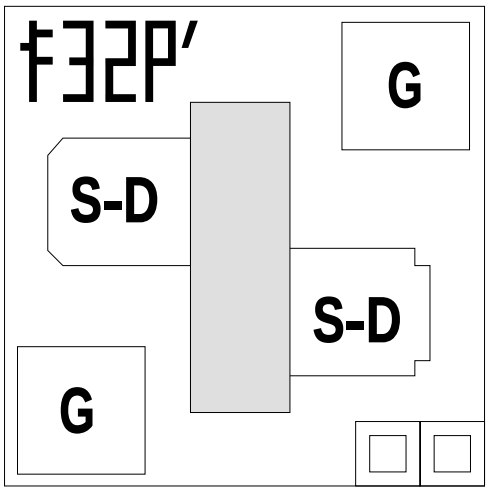
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the PJ32 Process.

Datasheet

2N5020, 2N5021
2N5460, 2N5461
2N5462



Die Size = 0.018" X 0.018"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		PJ32 Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	30	50		V	I_G = 1 µA, V_{DS} = Ø	
Reverse Gate Leakage Current	I_{GSS}		1	2	nA	V_{GS} = 15V, V_{DS} = Ø	
Drain Saturation Current (Pulsed)	I_{DSS}	– 1		– 15	mA	V_{DS} = – 15V, V_{GS} = Ø	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	0.5		7	V	V_{DS} = – 15V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance	g_{fs}		2.5		mS	V_{DS} = – 15V, V_{GS} = Ø	f = 1 kHz
Input Capacitance	C_{iss}		3.2		pF	V_{DS} = Ø, V_{GS} = 10	f = 1 MHz
Feedback Capacitance	C_{rss}		1.7		pF	V_{DS} = Ø, V_{GS} = 10	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		10		nV/√HZ	V_{DS} = 10V, V_{GS} = Ø	f = 1 Hz

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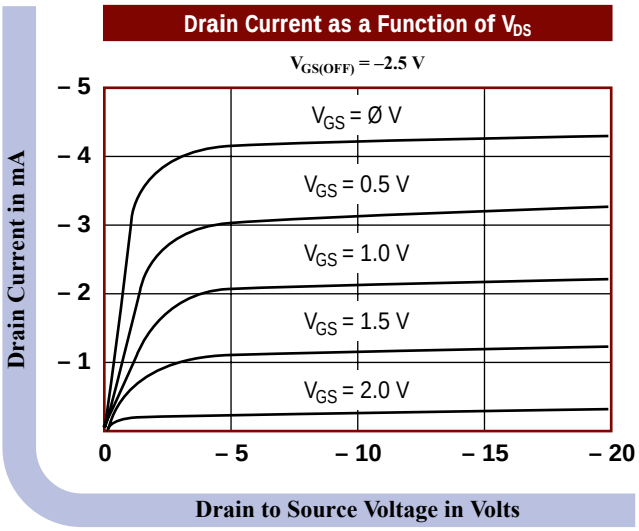
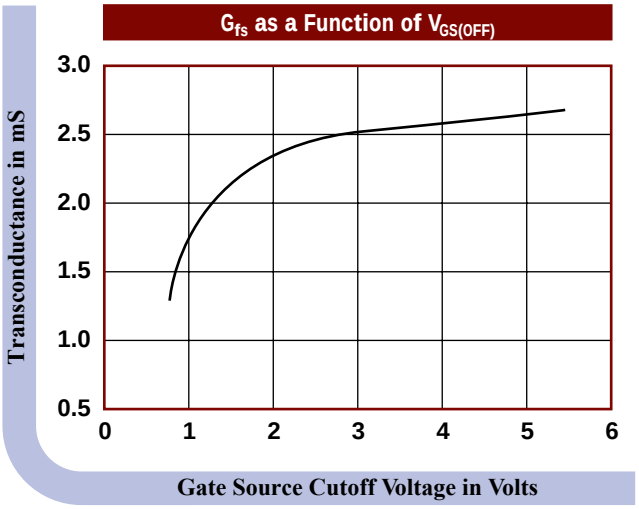
PJ32 Process

Silicon Junction Field-Effect Transistor

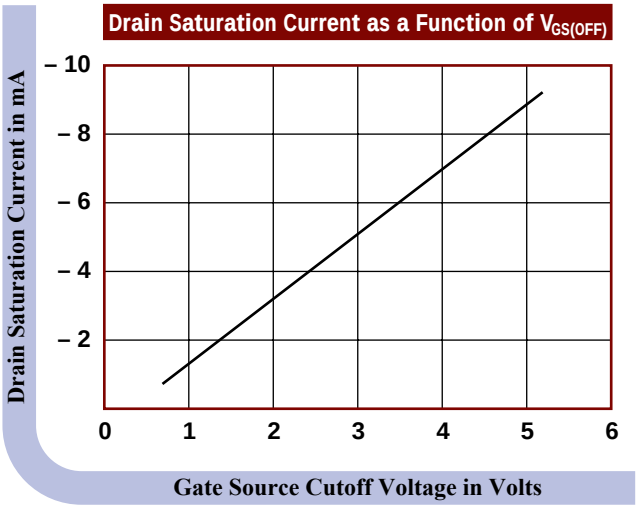
Drain Current as a Function of V_{DS}



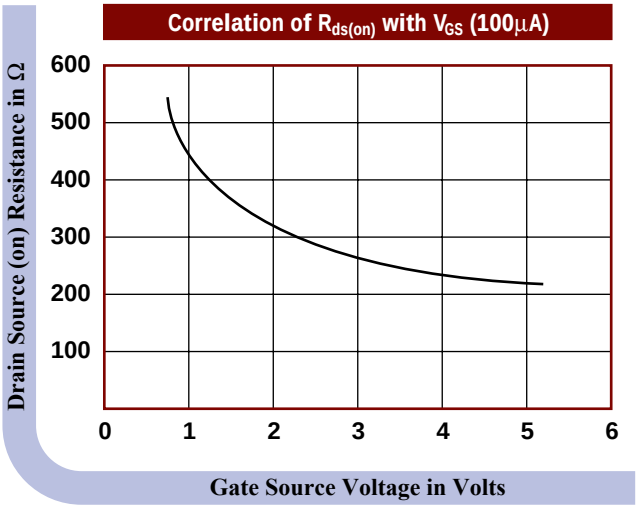
G_{fs} as a Function of $V_{GS(OFF)}$



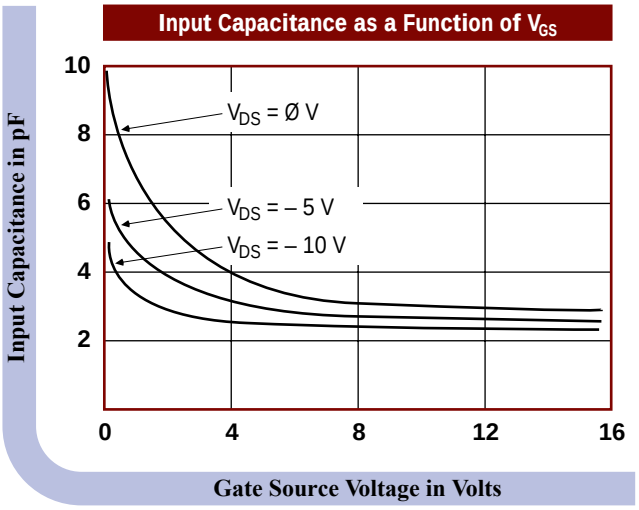
Drain Saturation Current as a Function of $V_{GS(OFF)}$



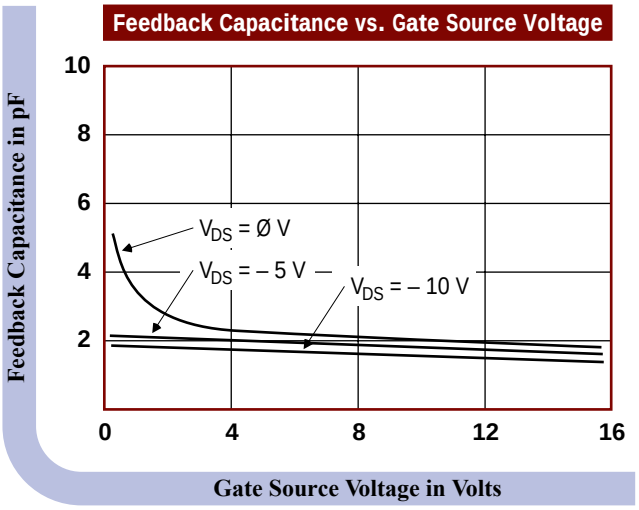
Correlation of $R_{ds(on)}$ with V_{GS} (100µA)



Input Capacitance as a Function of V_{GS}



Feedback Capacitance vs. Gate Source Voltage



NJ36D Process

Silicon Junction Field-Effect Transistor

- Monolithic Dual Construction
- High Frequency Amplifier
- Low-Noise Amplifier

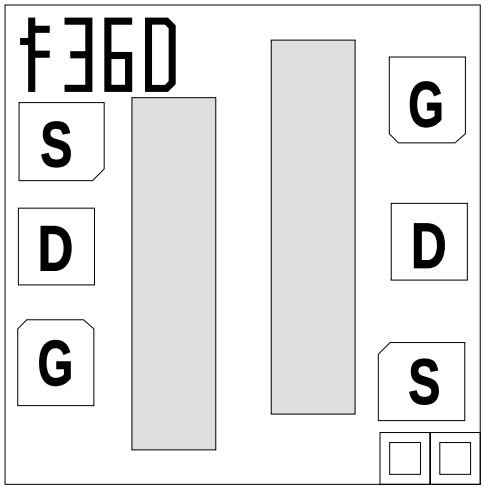
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ36D Process.

Datasheet

2N5911, 2N5912
IFN5911, IFN5912



Die Size = 0.026" X 0.026"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		NJ36D Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25	– 35		V	I_G = – 1 mA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		0.05	0.1	nA	V_{GS} = – 15V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	1		40	mA	V_{DS} = 15V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.5		– 8	V	V_{DS} = 15V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Drain Source ON Resistance	$r_{ds(on)}$	90		250	Ω	I_D = Ø mA, V_{GS} = ØV	f = 1 kHz
Forward Transconductance	g_{fs}		8.5		mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		5.5	7.0	pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{rss}		1.5	3	pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		5		nV/√HZ	V_{DS} = 15V, I_D = 5 mA	f = 1 kHz
Differential Gate Source Voltage	$V_{GS1} - V_{GS2}$	5	20	100	mV	V_{DG} = 15V, I_D = 5 mA	

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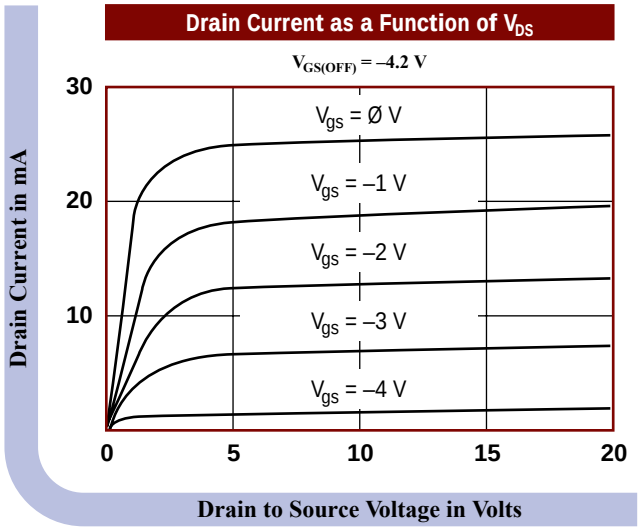
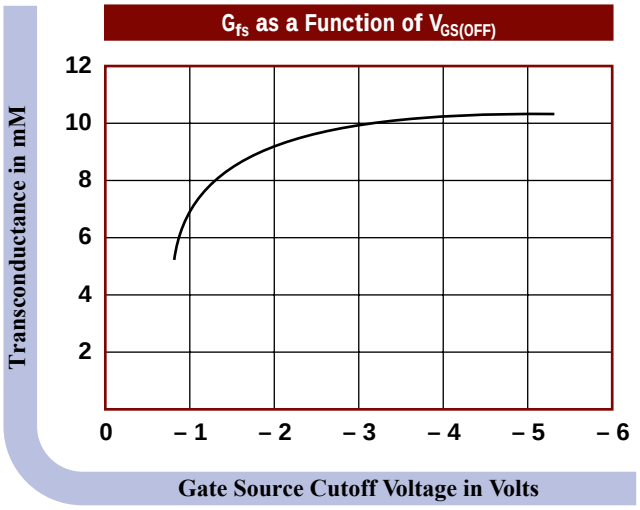
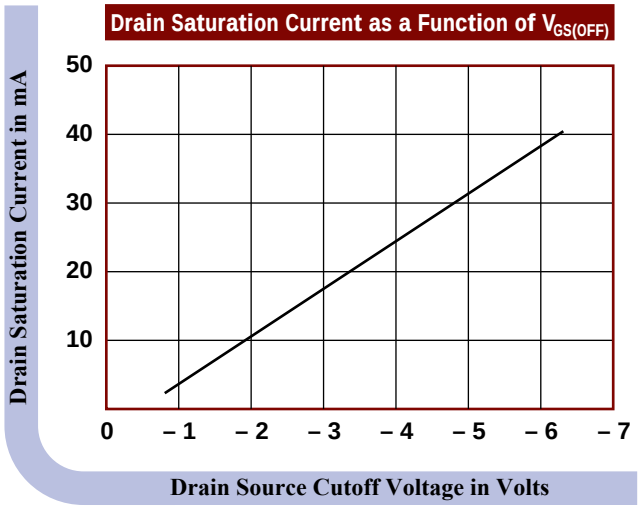
Drain Current as a Function of V_{DS}



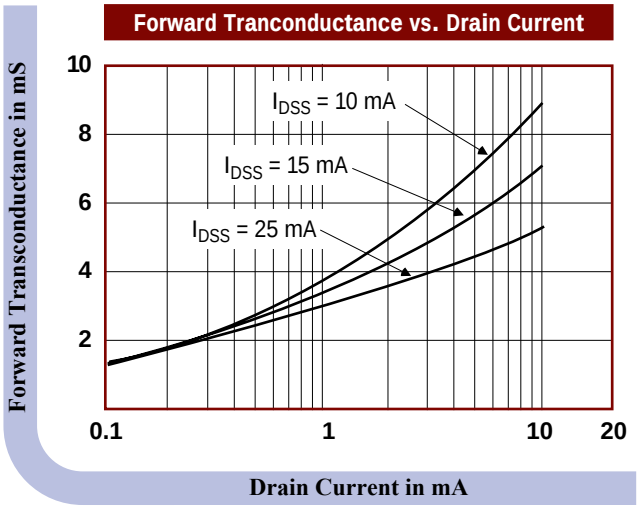
G_{fs} as a Function of $V_{GS(OFF)}$



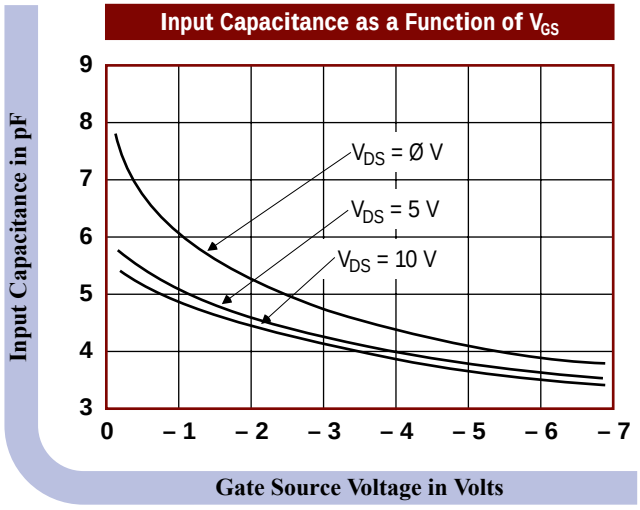
Drain Saturation Current as a Function of $V_{GS(OFF)}$



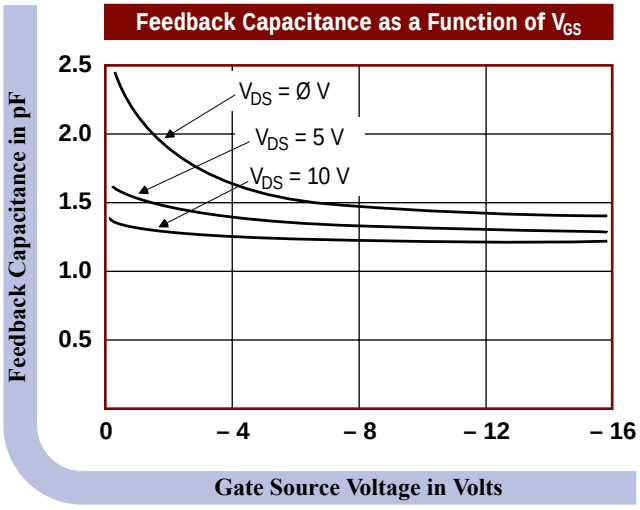
Forward Tranconductance vs. Drain Current



Input Capacitance as a Function of V_{GS}



Feedback Capacitance as a Function of V_{GS}



NJ42 Process

Silicon Junction Field-Effect Transistor

- General Purpose Amplifier
- High Breakdown Voltage

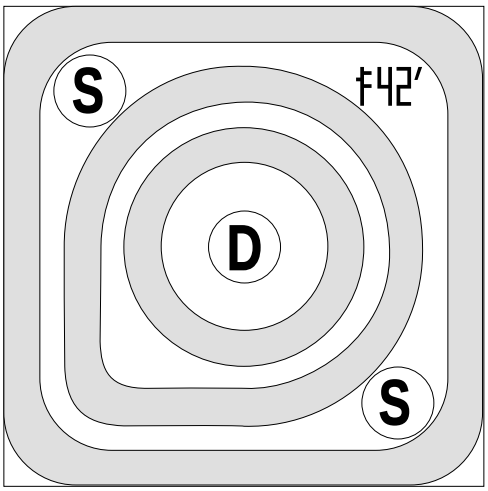
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ42 Process.

Datasheet

2N6449, 2N6450
IFN6449, IFN6450



Die Size = 0.032" X 0.032"
All Bond Pads = 0.004", Dia.
Substrate is also Gate.

At 25°C free air temperature:		NJ42 Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 300	– 400		V	I_G = 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 1	– 10	nA	V_{GS} = – 150V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	2		10	mA	V_{DS} = 30V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 2		– 12	V	V_{DS} = 30V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance	g_{fs}		800		µS	V_{DS} = 30V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		6	10	pF	V_{DS} = 30V, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{rss}		2	5	pF	V_{DS} = 30V, V_{GS} = ØV	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		10		nV/√HZ	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz

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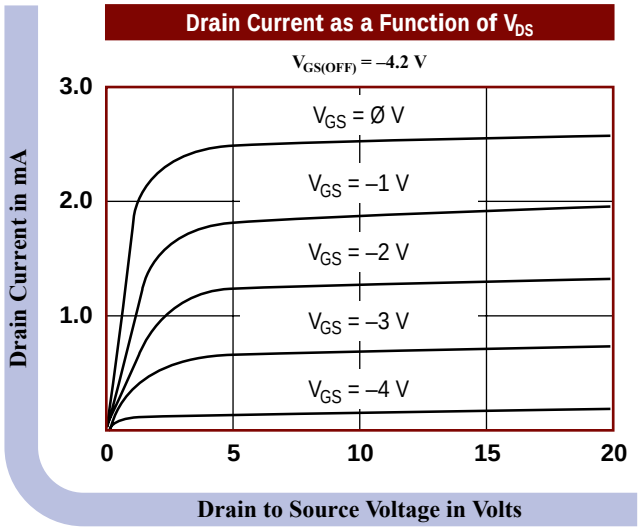
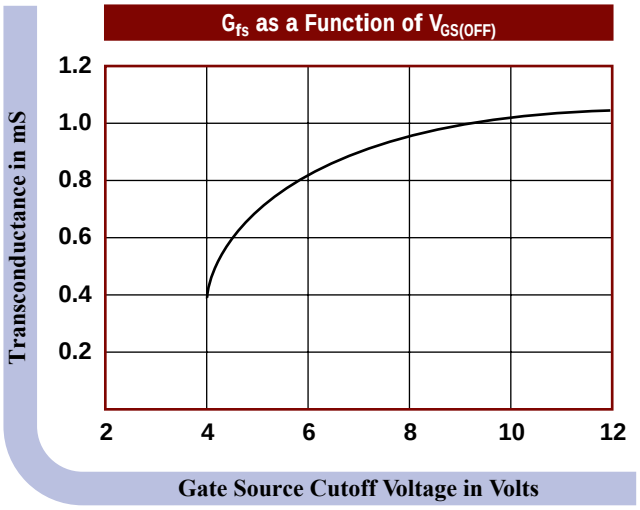
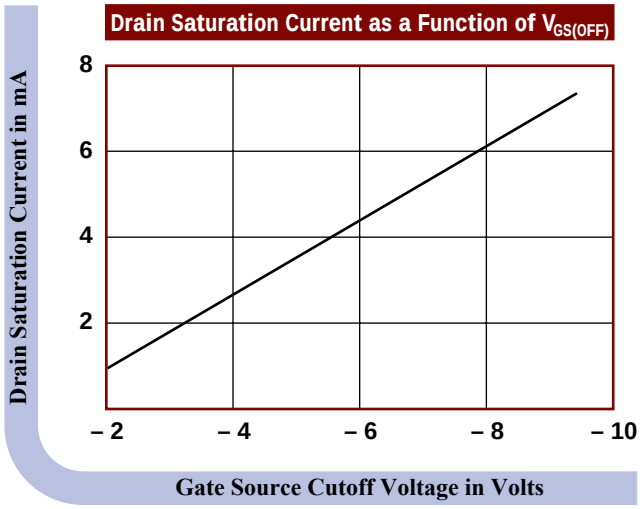
Drain Current as a Function of V_{DS}



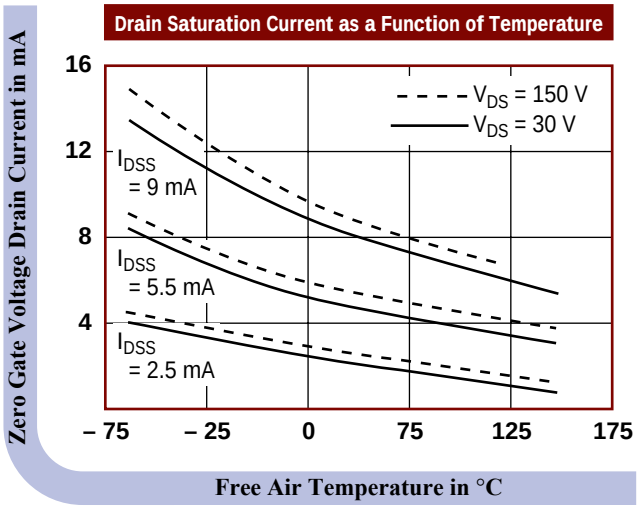
G_{fs} as a Function of $V_{GS(OFF)}$



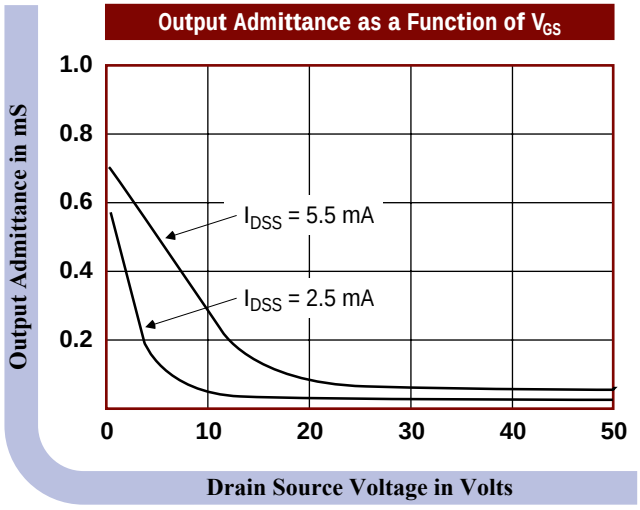
Drain Saturation Current as a Function of $V_{GS(OFF)}$



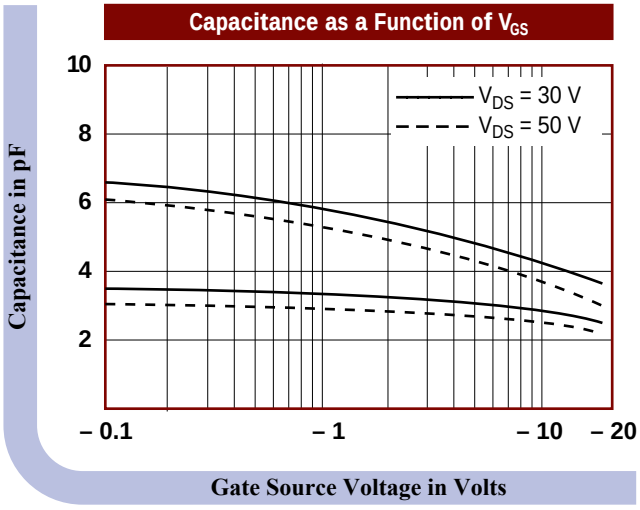
Drain Saturation Current as a Function of Temperature



Output Admittance as a Function of V_{GS}



Capacitance as a Function of V_{GS}



NJ72 Process

Silicon Junction Field-Effect Transistor

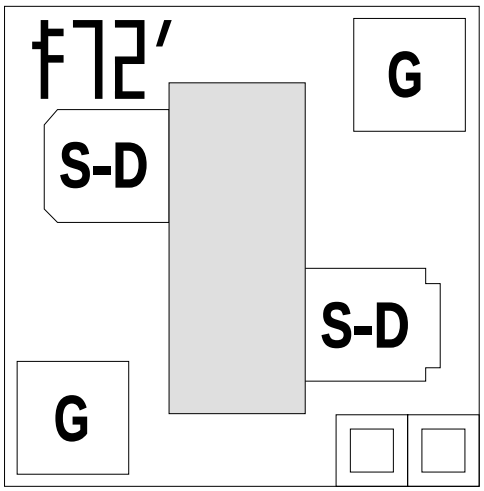
- VHF/UHF Amplifier

Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ72 Process.

Datasheet	Datasheet
IFN5564, IFN5565	U308, U309
IFN5566	U430, U431
J308, J309	VCR2N
J308, J309	
J310	



Die Size = 0.020" X 0.020"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		NJ72 Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25	– 40		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 10	– 100	pA	V_{GS} = – 15V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	5		90	mA	V_{DS} = 15V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1		– 5.5	V	V_{DS} = 15V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance	g_{fs}		22		mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Drain Source ON Resistance	$r_{ds(on)}$		40		Ω	I_D = 1 mA, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		6.5		pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Feedback Capacitance	C_{rss}		2.5		pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz

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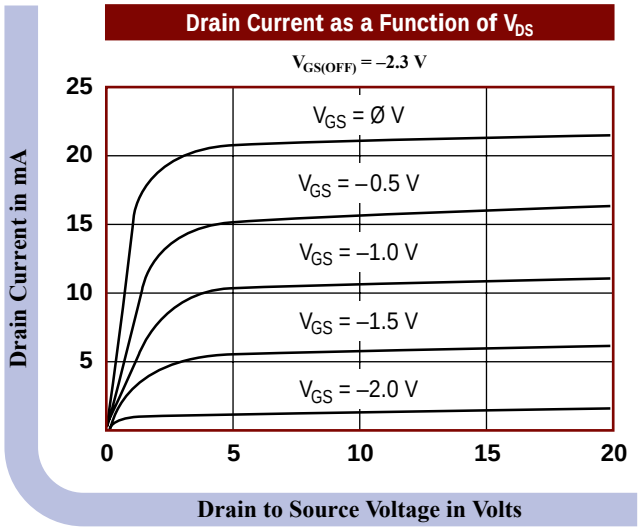
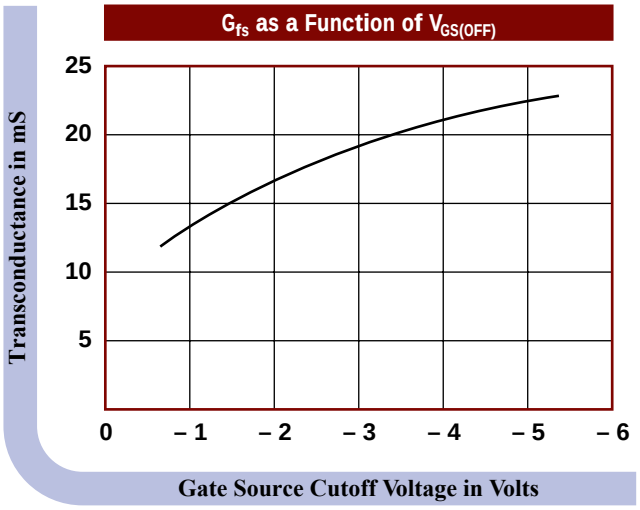
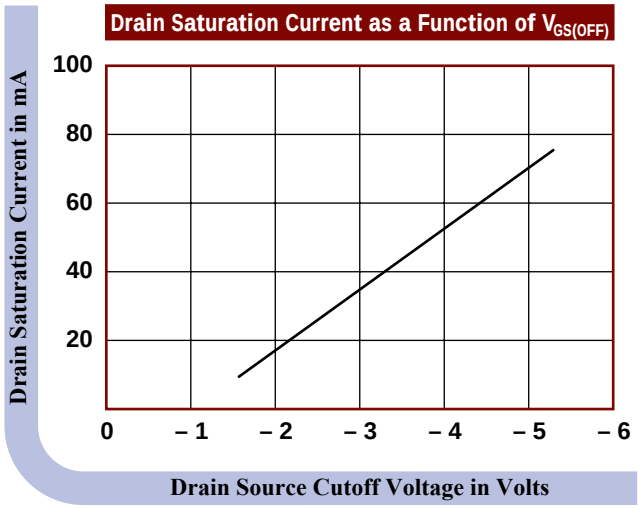
Drain Current as a Function of V_{DS}



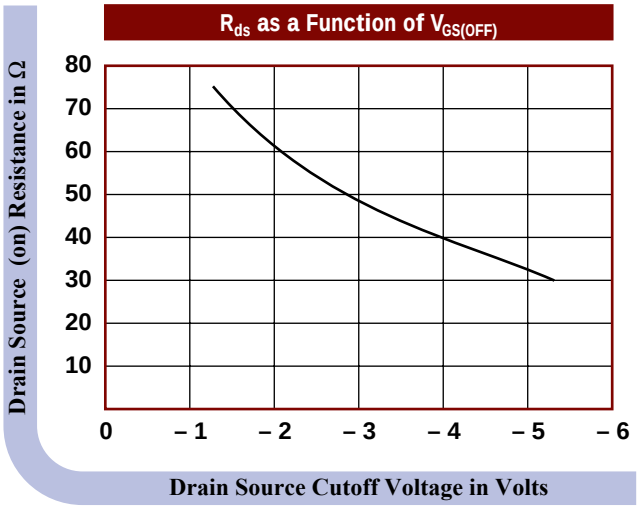
G_{fs} as a Function of $V_{GS(OFF)}$



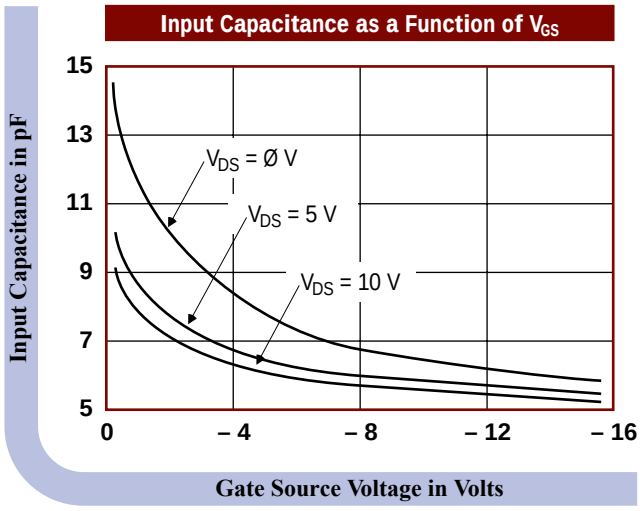
Drain Saturation Current as a Function of $V_{GS(OFF)}$



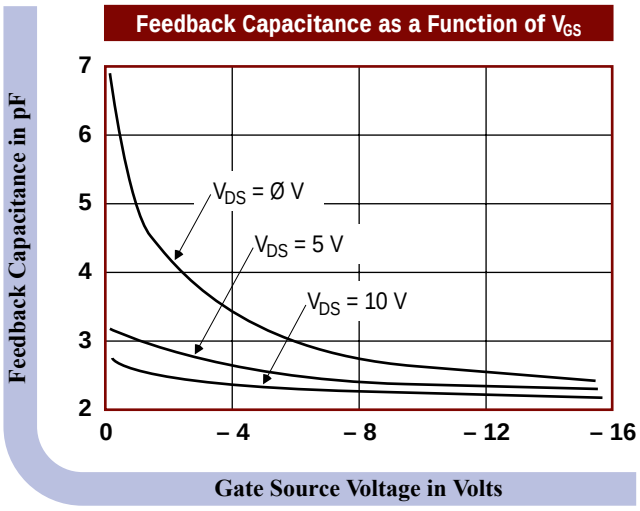
R_{ds} as a Function of $V_{GS(OFF)}$



Input Capacitance as a Function of V_{GS}



Feedback Capacitance as a Function of V_{GS}



NJ72L Process

Silicon Junction Field-Effect Transistor

- VHF/UHF Amplifier

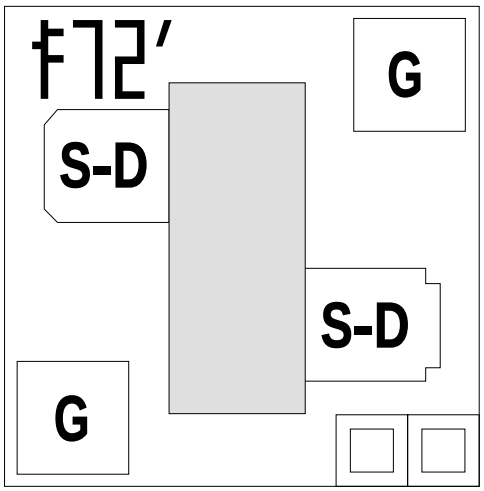
Absolute maximum ratings at 25°C free-air temperature.

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ72L Process.

Datasheet

U310
U311
U350



Die Size = 0.020" X 0.020"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		NJ72L Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20	– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 10	– 100	pA	V_{GS} = – 15V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	5		90	mA	V_{DS} = 15V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 1		– 5.5	V	V_{DS} = 15V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance	g_{fs}		22		mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Drain Source ON Resistance	$r_{ds(on)}$		40		Ω	I_D = 1 mA, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		7		pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Feedback Capacitance	C_{rss}		2.5		pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz

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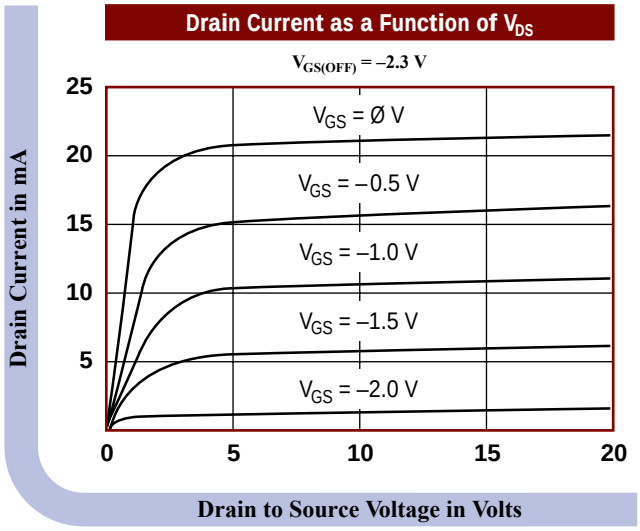
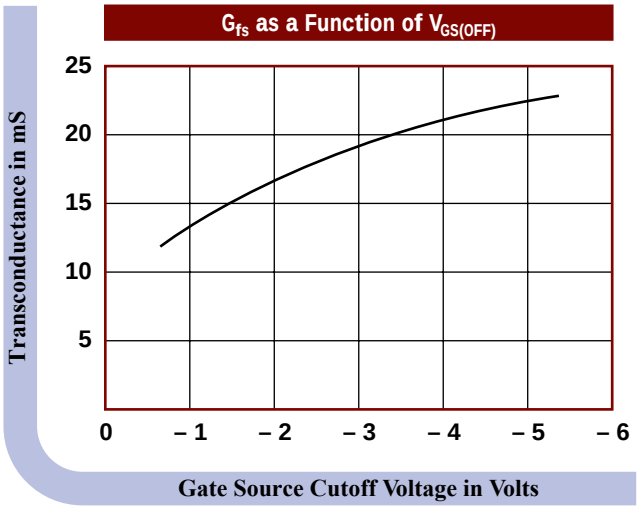
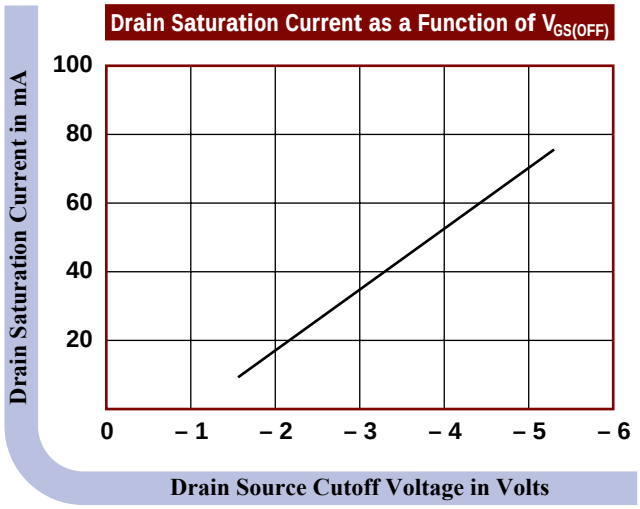
Drain Current as a Function of V_{DS}



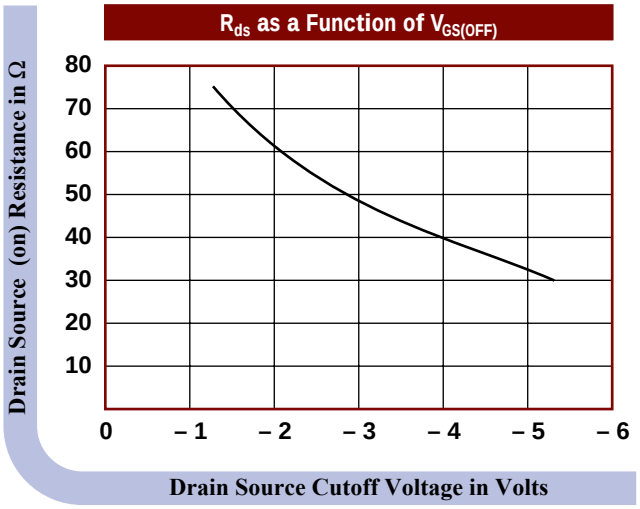
G_{fs} as a Function of $V_{GS(OFF)}$



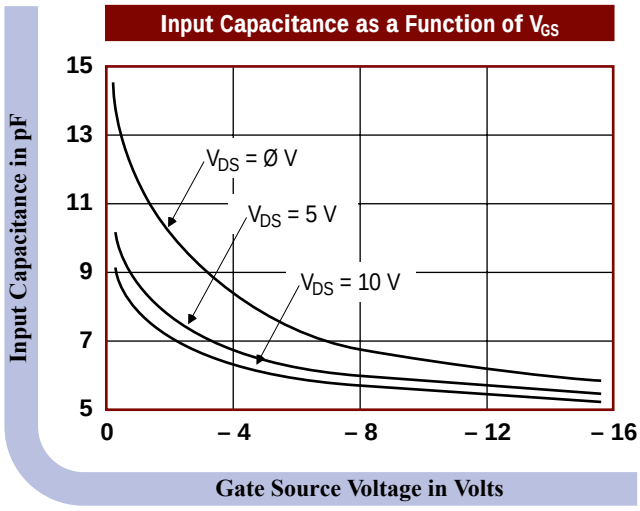
Drain Saturation Current as a Function of $V_{GS(OFF)}$



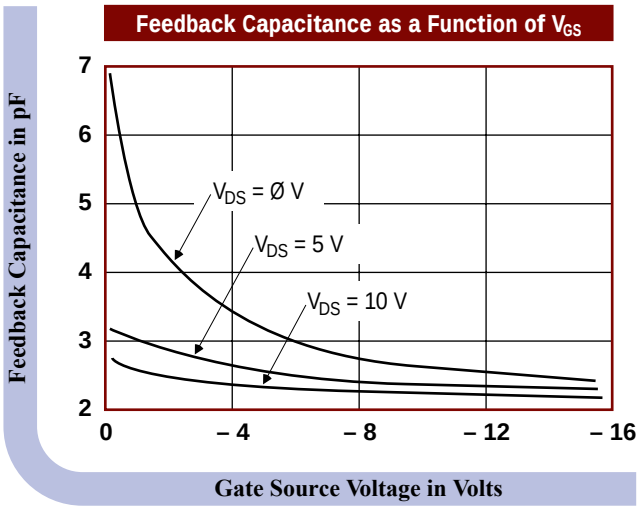
R_{ds} as a Function of $V_{GS(OFF)}$



Input Capacitance as a Function of V_{GS}



Feedback Capacitance as a Function of V_{GS}



PJ99 Process

Silicon Junction Field-Effect Transistor

- General Purpose Amplifier
- Analog Switch

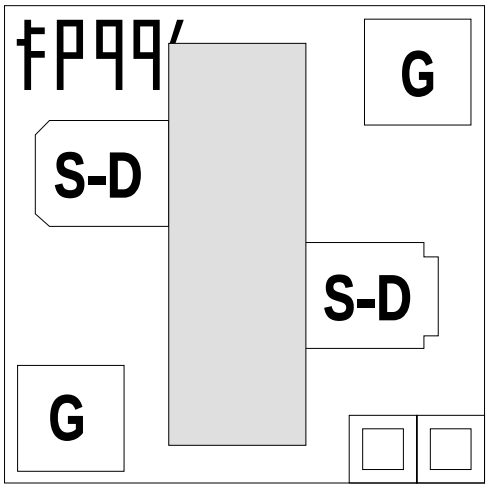
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the PJ99 Process.

Datasheet
2N3993, 2N3993A
2N3994, 2N3994A
2N5114, 2N5115
2N5116
2SJ44
IFN5114, IFN5115
IFN5116

Datasheet
IFP44
J174, J175
J176, J177
P1086, P1087
VCR3P



Die Size = 0.021" X 0.021"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		PJ99 Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	30	40		V	I_G = 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		0.5	1	nA	V_{GS} = 20V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	– 5		– 60	mA	V_{DS} = – 15V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	1		8	V	V_{DS} = – 15V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Drain Source ON Resistance	$r_{ds(on)}$		75		Ω	I_D = 1 mA, V_{GS} = ØV	f = 1 kHz
Forward Transconductance	g_{fs}		15		mS	V_{DS} = – 15V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		18		pF	V_{DS} = 15V, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{iss}		4.5		pF	V_{DS} = ØV, V_{GS} = 10V	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		8		nV/√HZ	V_{DS} = – 10V, V_{GS} = ØV	f = 1 kHz
Turn On Delay Time	$t_{d(on)}$		5		ns	V_{DD} = – 10V, $I_{D(ON)}$ = – 15 mA R_L = 580Ω, $V_{GS(ON)}$ = ØV $V_{GS(OFF)}$ = 12V	
Rise Time	t_r		10		ns		
Turn Off Delay Time	$t_{d(off)}$		6		ns		
Fall Time	t_f		5		ns		

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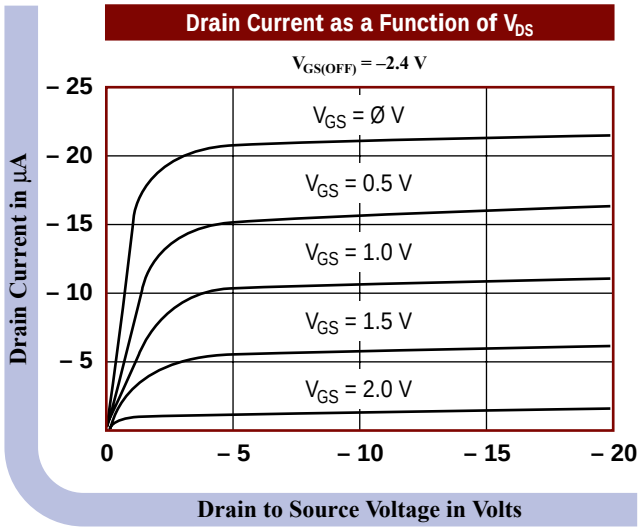
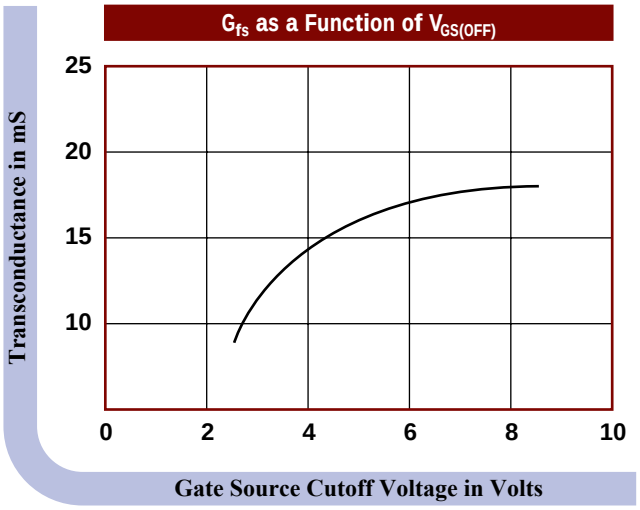
PJ99 Process

Silicon Junction Field-Effect Transistor

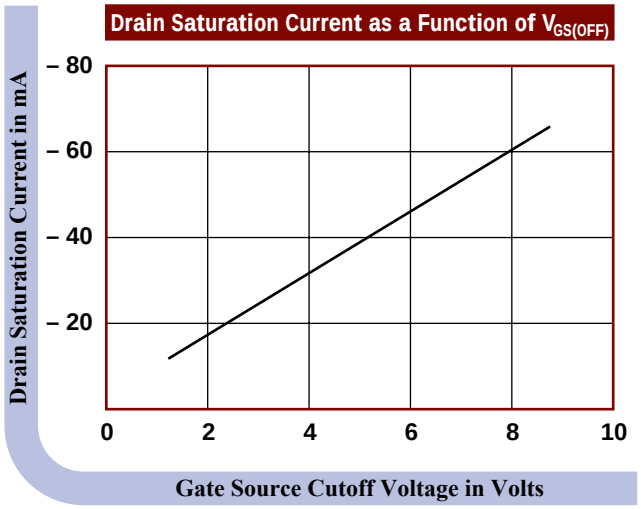
Drain Current as a Function of V_{DS}



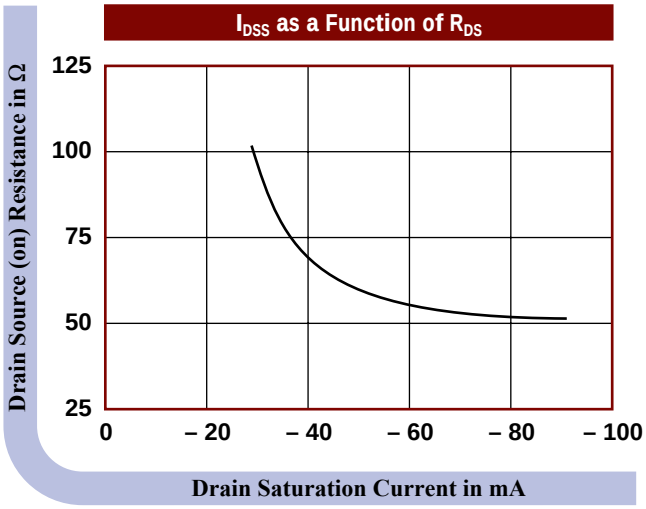
G_{fs} as a Function of $V_{GS(OFF)}$



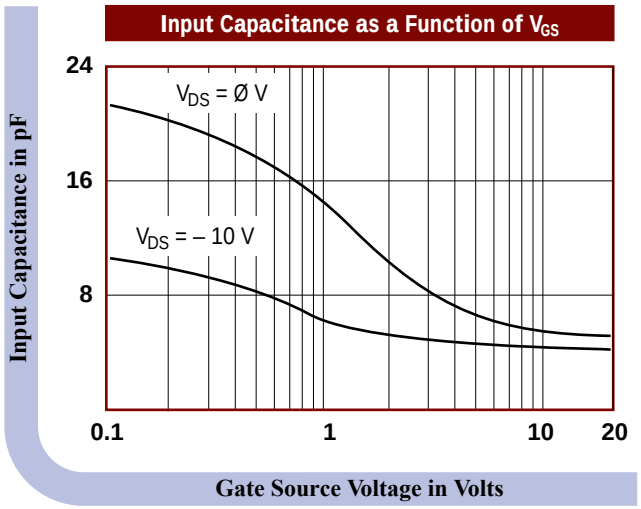
Drain Saturation Current as a Function of $V_{GS(OFF)}$



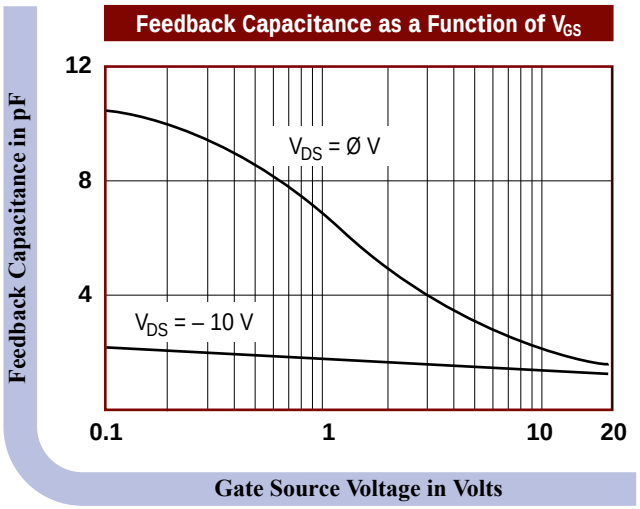
I_{DSS} as a Function of R_{DS}



Input Capacitance as a Function of V_{GS}



Feedback Capacitance as a Function of V_{GS}



NJ132 Process

Silicon Junction Field-Effect Transistor

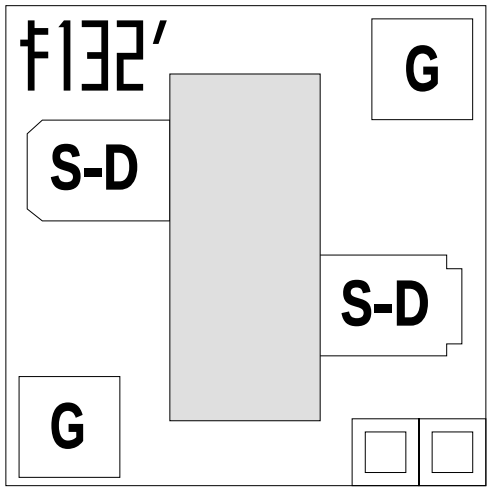
- High Speed Switch
- Low-Noise Amplifier

Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ132 Process.

Datasheet	Datasheet
2N4391, 2N4392	2SK113
2N4393	IFN113
2N4856, 2N4857	2N4860A, 2N4861A
2N4858, 2N4859	J111, J112
2N4860, 2N4861	J113
2N4856A, 2N4857A	
2N4858A, 2N4859A	



Die Size = 0.022" X 0.022"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		NJ132 Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 30	– 45		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 10	– 100	pA	V_{GS} = – 20V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	10		150	mA	V_{DS} = 20V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.5		– 7	V	V_{DS} = 20V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Drain Source ON Resistance	$r_{ds(on)}$		25		Ω	I_D = 1 mA, V_{GSS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		12		pF	V_{DS} = 20V, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{iss}		2.5		pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Turn On Delay Time	$t_{d(on)}$		6		ns	V_{DD} = – 10V, I_D = 10 mA R_L = 10V, $V_{GS(ON)}$ = ØV $V_{GS(OFF)}$ = – 6V	
Rise Time	t_r		5		ns		
Turn Off Delay Time	$t_{d(off)}$		50		ns		

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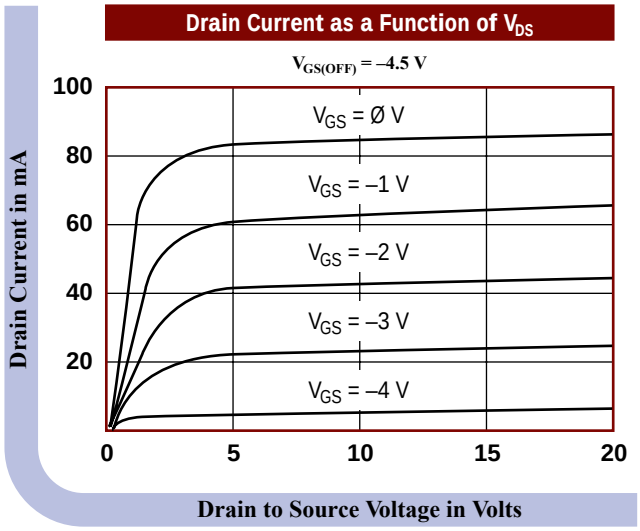
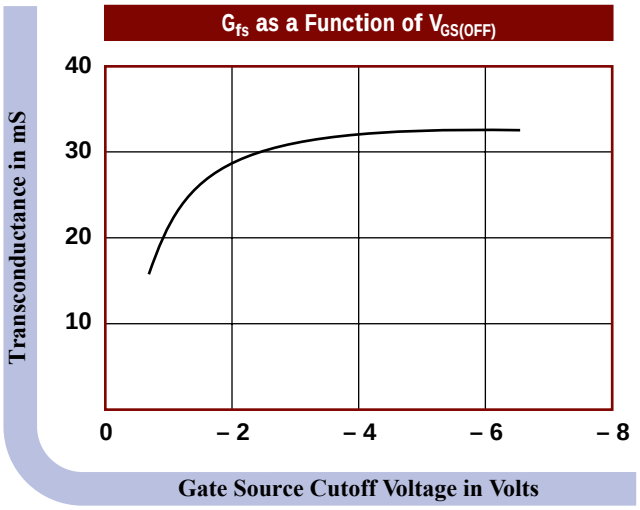
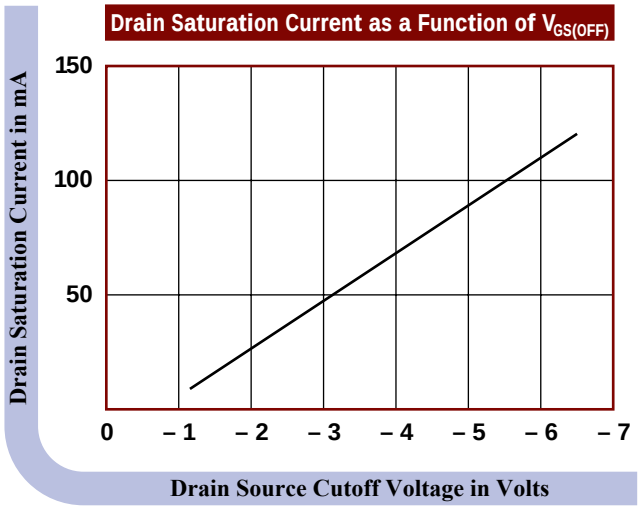
Drain Current as a Function of V_{DS}



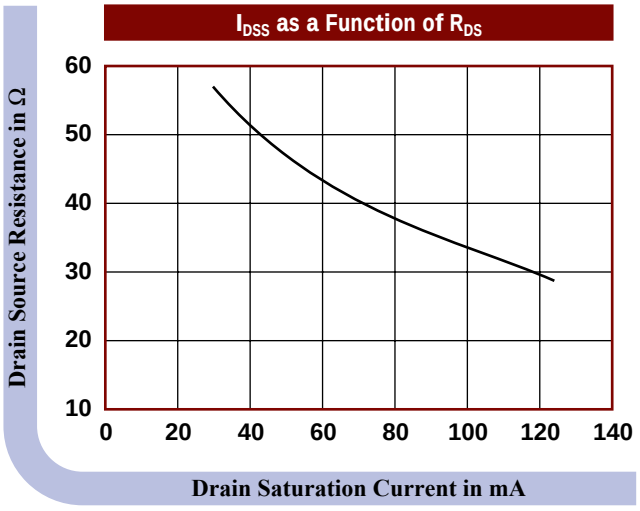
G_{fs} as a Function of $V_{GS(OFF)}$



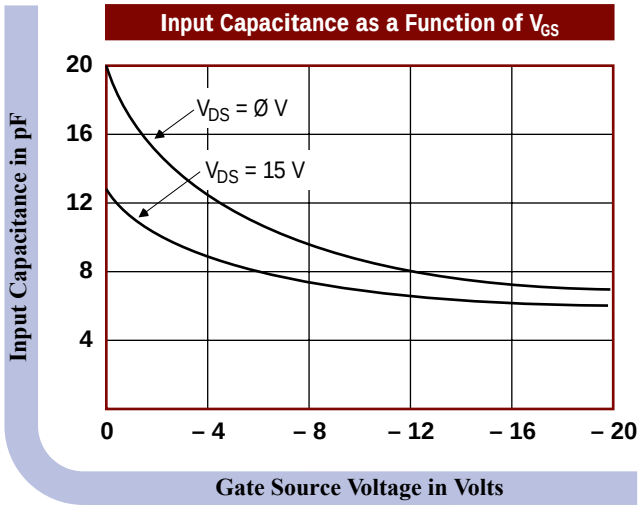
Drain Saturation Current as a Function of $V_{GS(OFF)}$



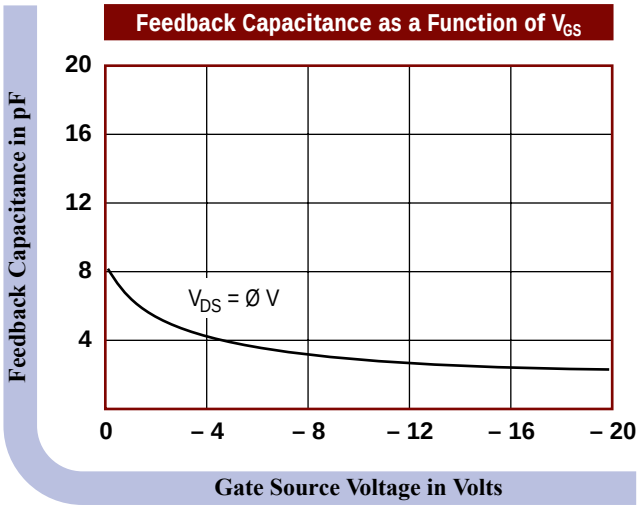
I_{DSS} as a Function of R_{DS}



Input Capacitance as a Function of V_{GS}



Feedback Capacitance as a Function of V_{GS}



NJ132L Process

Silicon Junction Field-Effect Transistor

- Low-Noise Amplifier

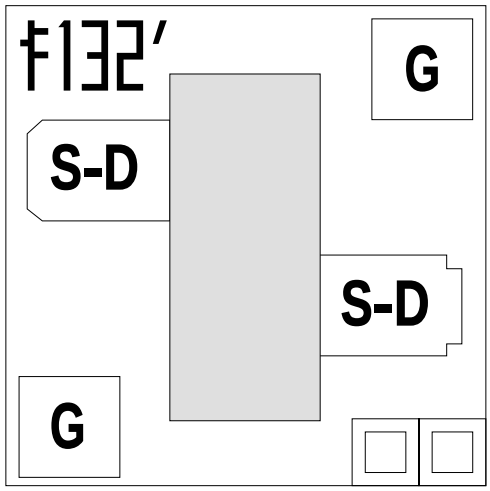
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ132L Process.

Datasheet

2N6451, 2N6452
2N6453, 2N6454
IF1320
IFN152
2SK152



Die Size = 0.022" X 0.022"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:

Static Electrical Characteristics		NJ132L Process Min	Typ	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 15	– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 50	– 100	nA	V_{GS} = – 10V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	5		100	mA	V_{DS} = 10V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.5		– 7	V	V_{DS} = 10V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance (pulsed)	g_{fs}	15			mS	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
	g_{fs}		15		mS	V_{DS} = 10V, I_D = 5 mA	f = 1 kHz
Input Capacitance	C_{iss}		15		pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{iss}		3.5		pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		1		nV/√HZ	V_{DS} = 4V, I_D = 5 mA	f = 1 kHz

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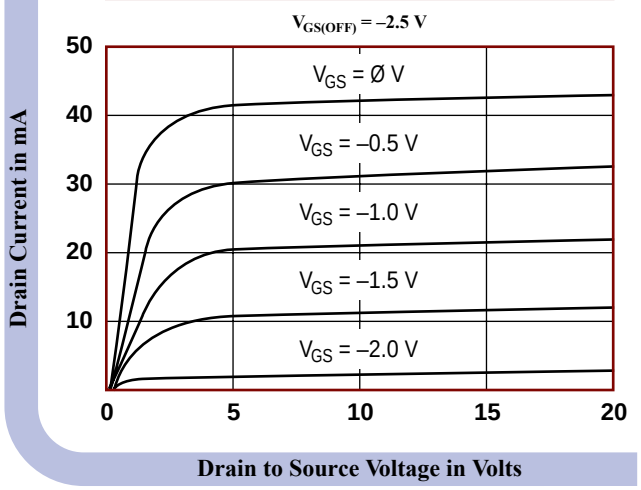
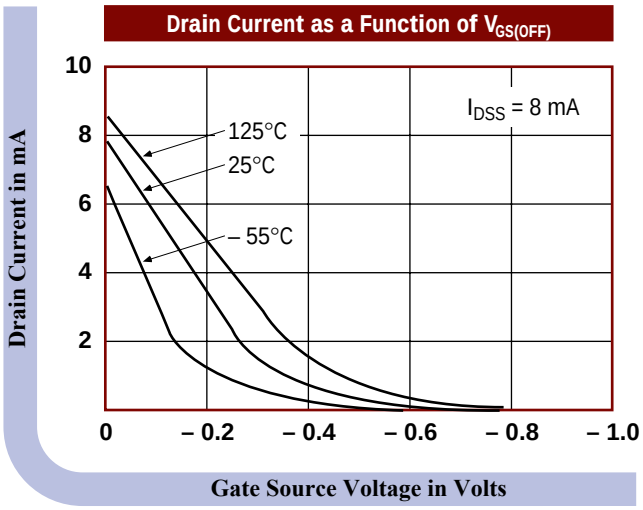
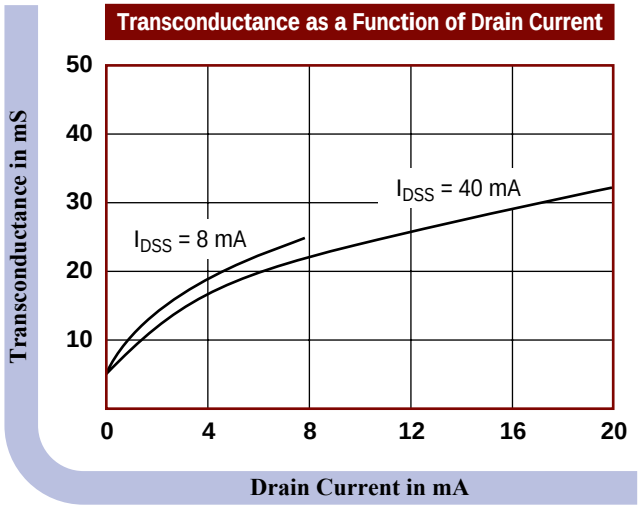
Drain Current as a Function of V_{DS}



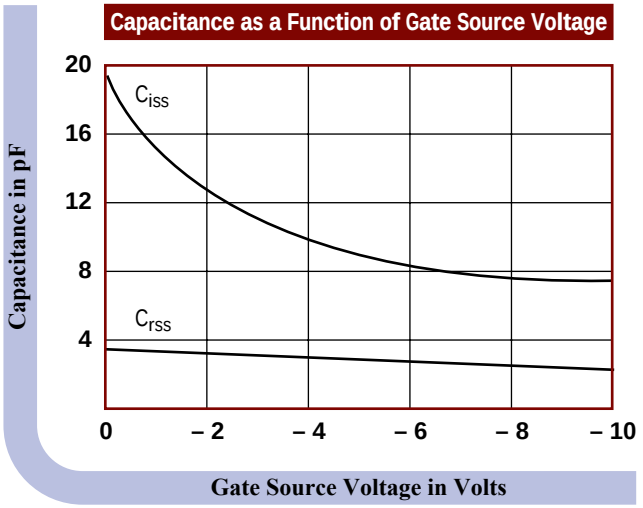
Drain Current as a Function of $V_{GS(OFF)}$



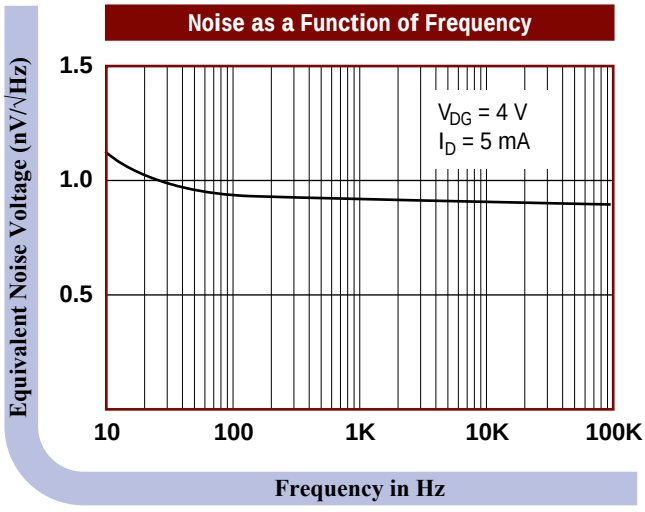
Transconductance as a Function of Drain Current



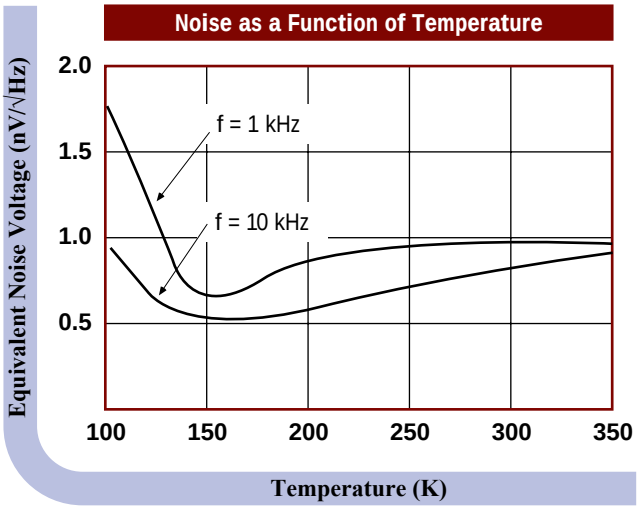
Capacitance as a Function of Gate Source Voltage



Noise as a Function of Frequency



Noise as a Function of Temperature



NJ450 Process

Silicon Junction Field-Effect Transistor

- LOW R(on) Switch
- Low-Noise, High Gain Amplifier

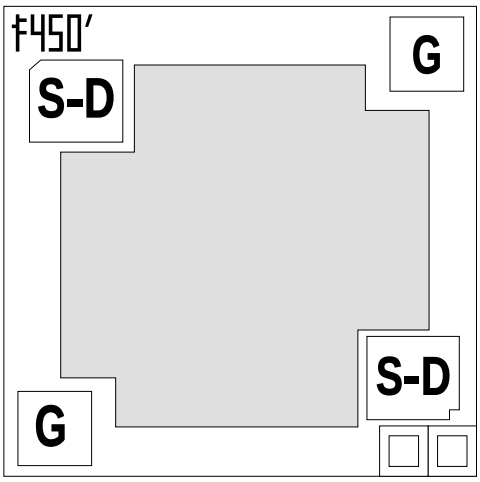
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ450 Process.

Datasheet

2SK363
IFN146, IFN147
IFN363
J108, J109
J110, J110A



Die Size = 0.028" X 0.028"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		NJ450 Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25	– 30		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 50	– 1000	pA	V_{GS} = – 15V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	5		600	mA	V_{DS} = 15V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.1		– 10	V	V_{DS} = 15V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Drain Source ON Resistance	$r_{ds(on)}$		7		Ω	I_D = 1 mA, V_{GS} = ØV	f = 1 kHz
Forward Transconductance	g_{fs}		250		mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		20		pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Feedback Capacitance	C_{rss}		10		pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz

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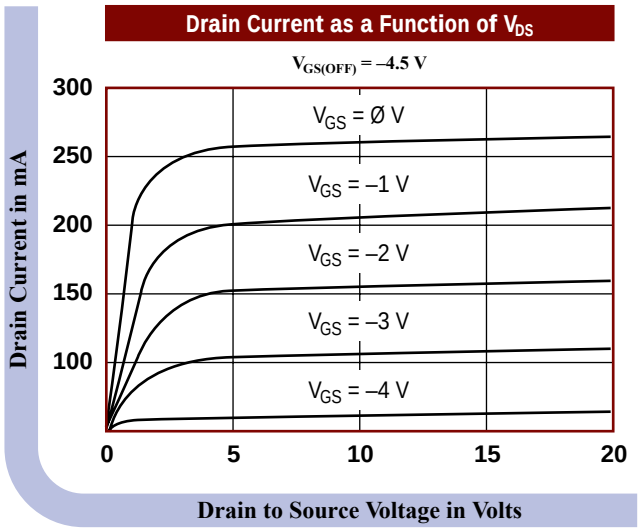
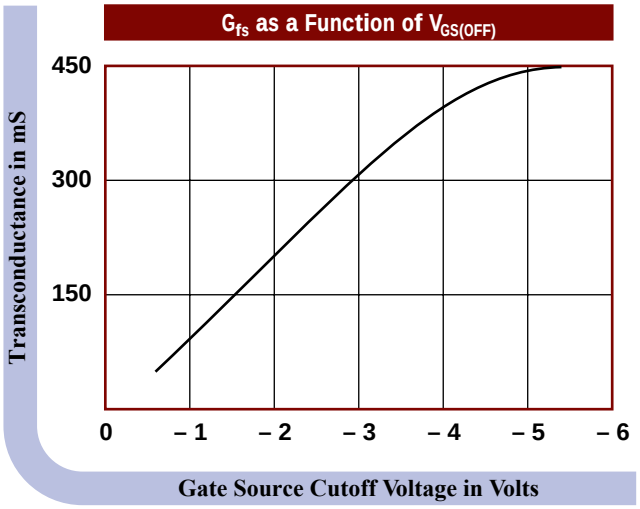
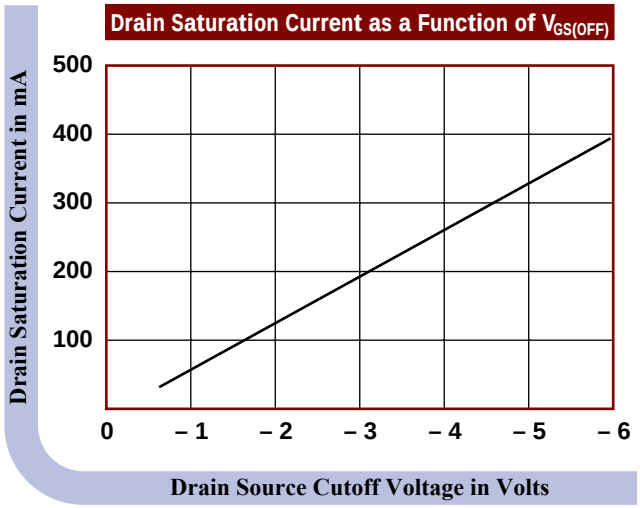
Drain Current as a Function of V_{DS}



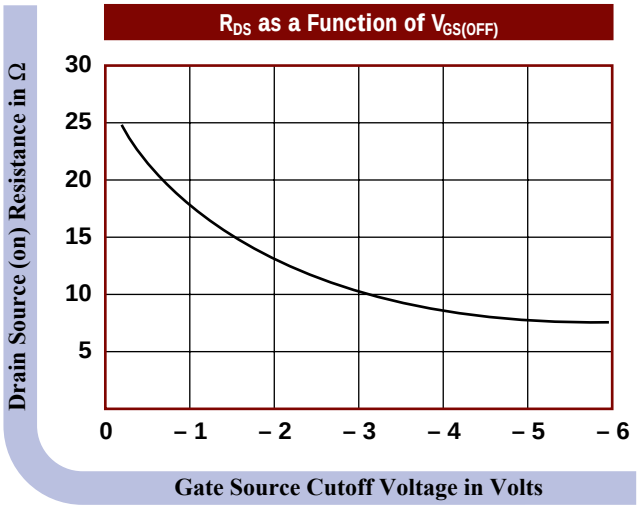
G_{fs} as a Function of $V_{GS(OFF)}$



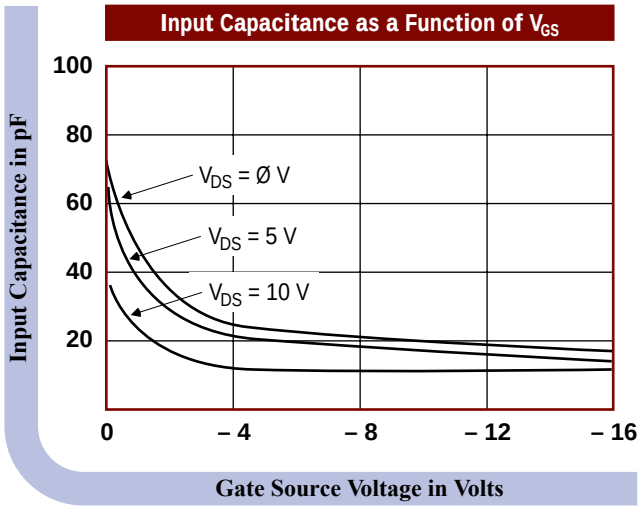
Drain Saturation Current as a Function of $V_{GS(OFF)}$



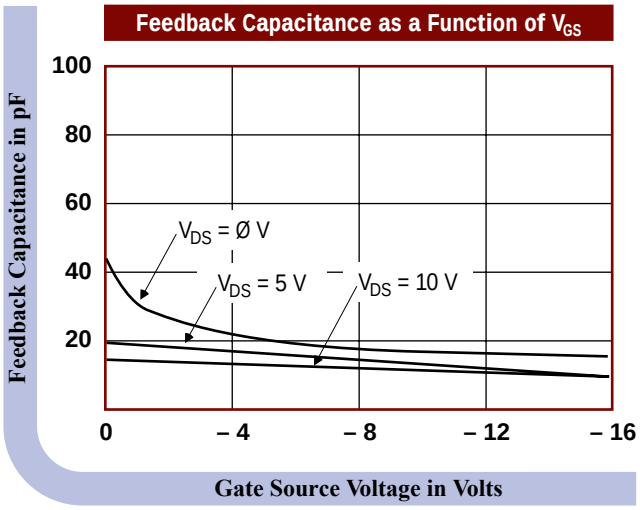
R_{DS} as a Function of $V_{GS(OFF)}$



Input Capacitance as a Function of V_{GS}



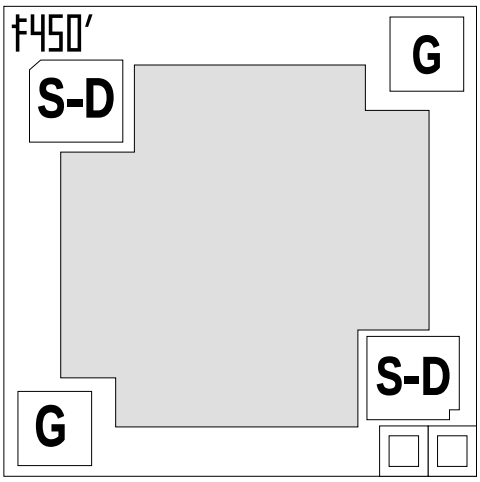
Feedback Capacitance as a Function of V_{GS}



NJ450L Process

Silicon Junction Field-Effect Transistor

- Low-Current
- Low Gate Leakage Current
- High Input Impedance



Die Size = 0.028" X 0.028"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

Absolute maximum ratings at 25°C free-air temperature.

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ450L Process.

Datasheet

2N6550
IF4500
IF4501
IFN860

At 25°C free air temperature:		NJ450L Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25	– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 50		pA	V_{GS} = – 15V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	5			mA	V_{DS} = 15V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.1		– 4	V	V_{DS} = 15V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance (Pulsed)	g_{fs}		100		mS	V_{DS} = 15V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		35		pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Feedback Capacitance	C_{rss}		10		pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		0.9		nV/√HZ	V_{DG} = 4V, I_D = 5 mA	f = 1 kHz

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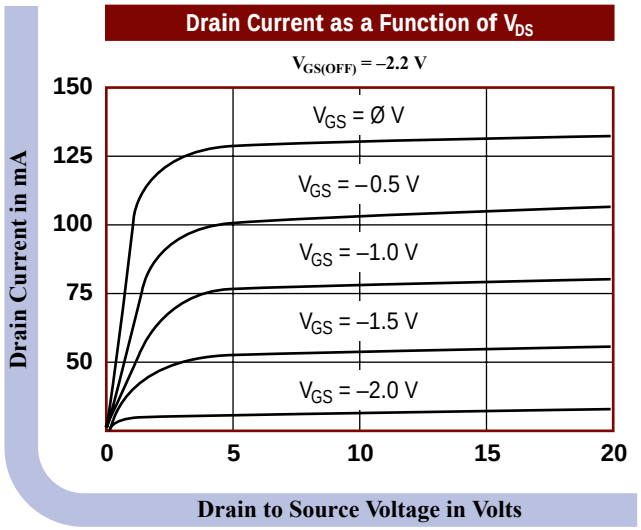
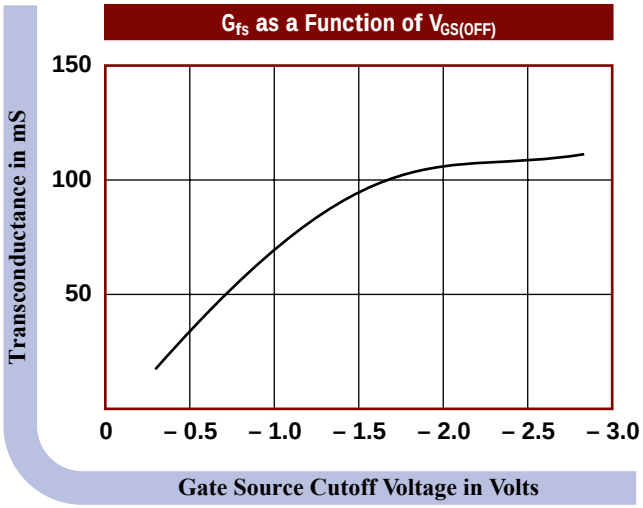
NJ450L Process

Silicon Junction Field-Effect Transistor

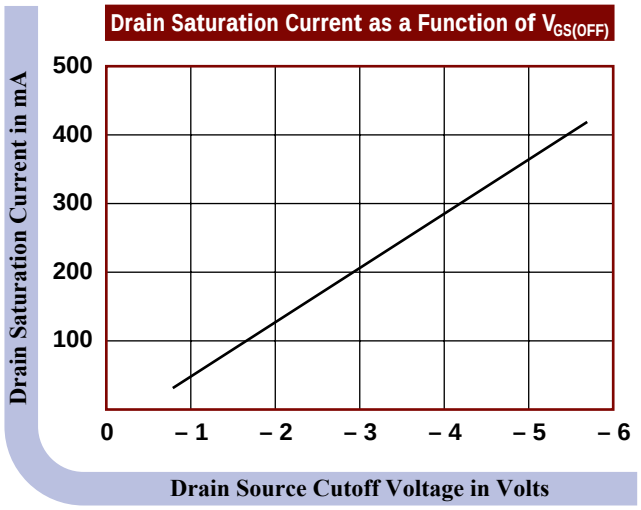
Drain Current as a Function of V_{DS}



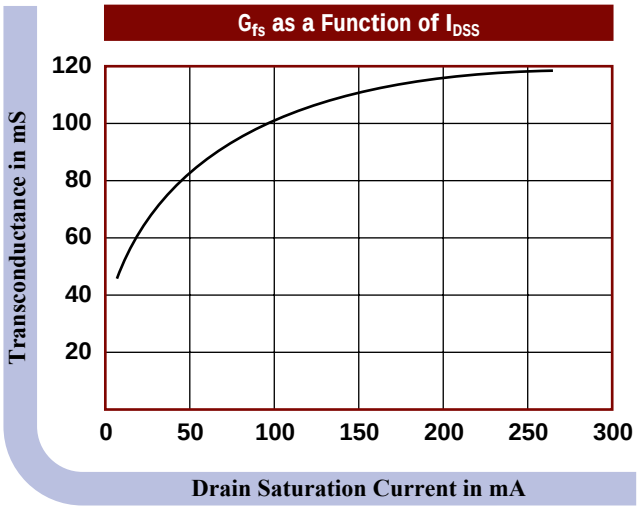
G_{fs} as a Function of $V_{GS(OFF)}$



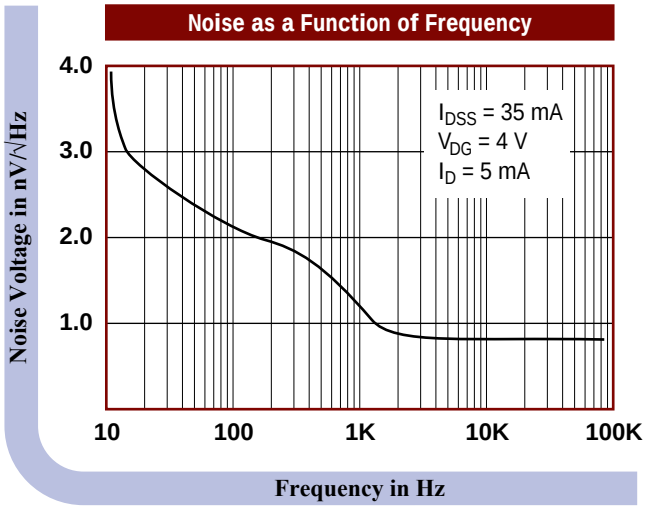
Drain Saturation Current as a Function of $V_{GS(OFF)}$



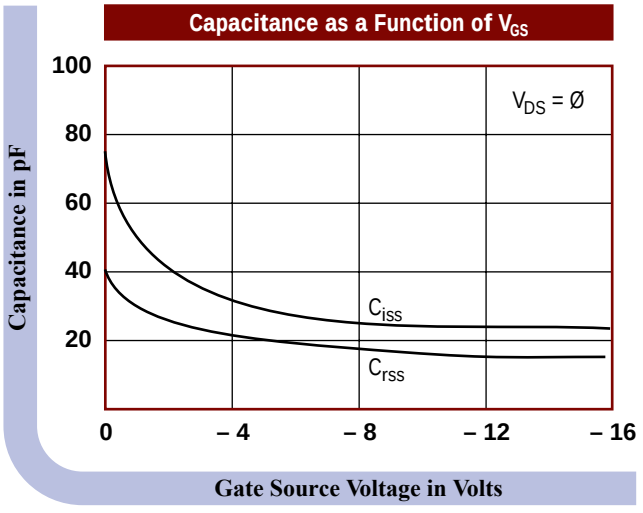
G_{fs} as a Function of I_{DSS}



Noise as a Function of Frequency



Capacitance as a Function of V_{GS}



NJ903 Process

Silicon Junction Field-Effect Transistor

- Analog Switch
- Digital Switch
- Low-Noise Amplifier

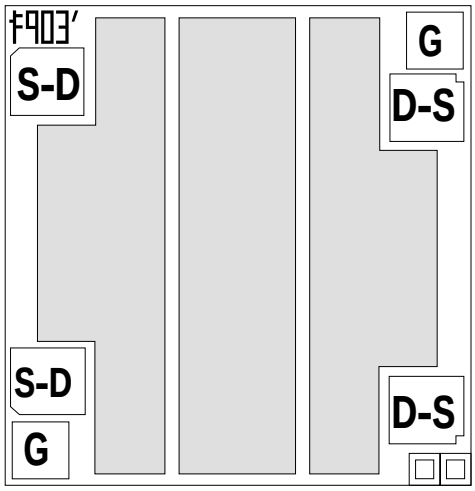
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ903 Process.

Datasheet

IFN5432
IFN5433
IFN5434



Die Size = 0.040" X 0.040"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		NJ903 Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25	– 40		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 0.1	– 1	nA	V_{GS} = – 15V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	100		900	mA	V_{DS} = 10V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 2		– 7	V	V_{DS} = 10V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Drain Source ON Resistance	$r_{ds(on)}$		5		Ω	I_D = 1 mA, V_{GS} = Ø	f = 1 kHz
Input Capacitance	C_{iss}		45		pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Feedback Capacitance	C_{iss}		22		pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Turn On Delay Time	$t_{d(on)}$		7		ns	V_{DD} = 1.5V, $I_{D(ON)}$ = 30 mA R_L = 50Ω, $V_{GS(ON)}$ = ØV $V_{GS(OFF)}$ = – 7V	
Rise Time	t_r		1		ns		
Turn Off Delay Time	$t_{d(off)}$		12		ns		
Fall Time	t_f		2		ns		

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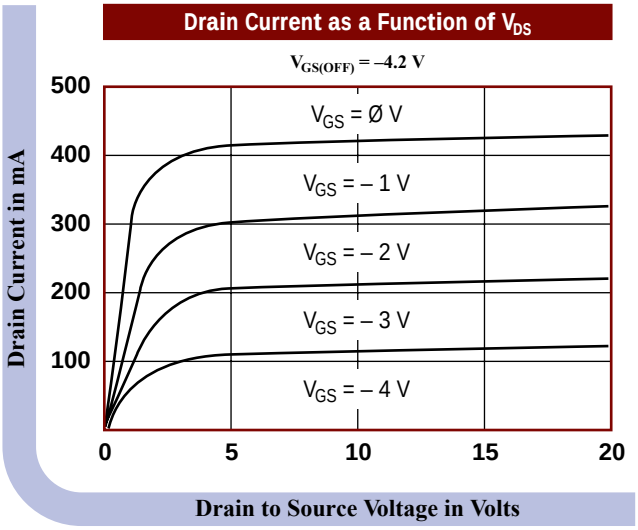
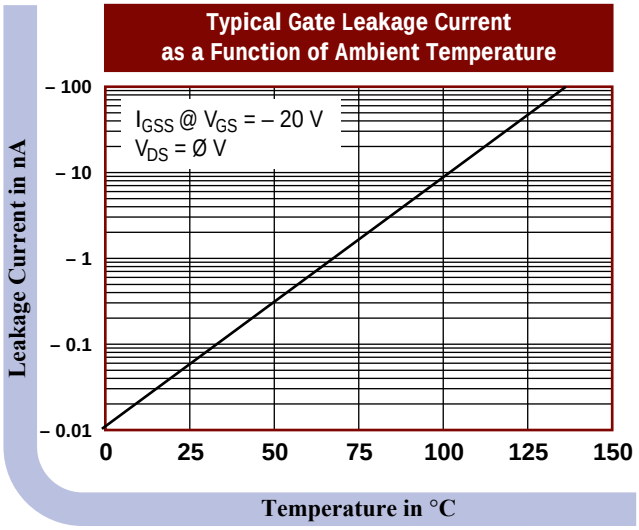
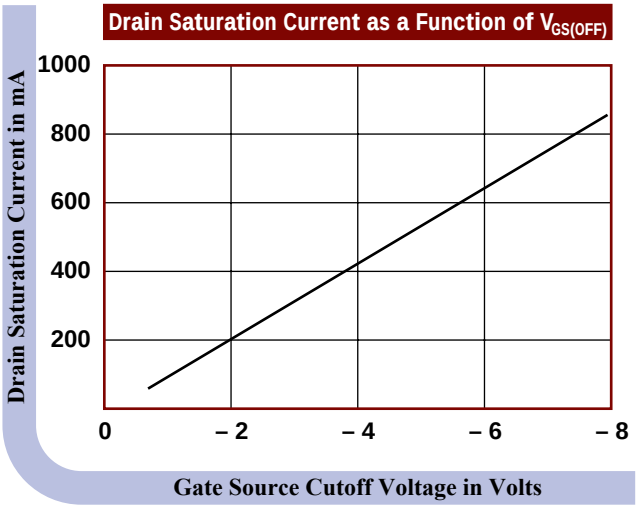
Drain Current as a Function of V_{DS}



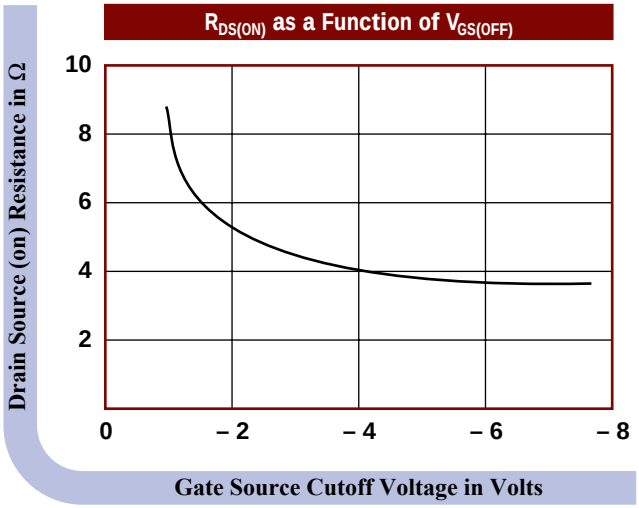
Typical Gate Leakage Current as a Function of Ambient Temperature



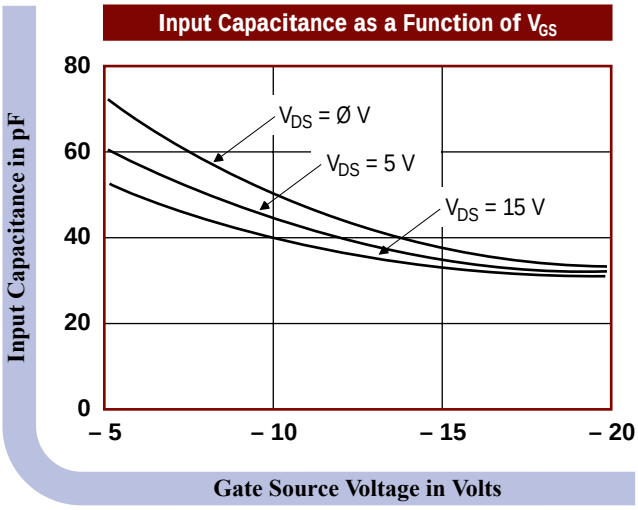
Drain Saturation Current as a Function of $V_{GS(OFF)}$



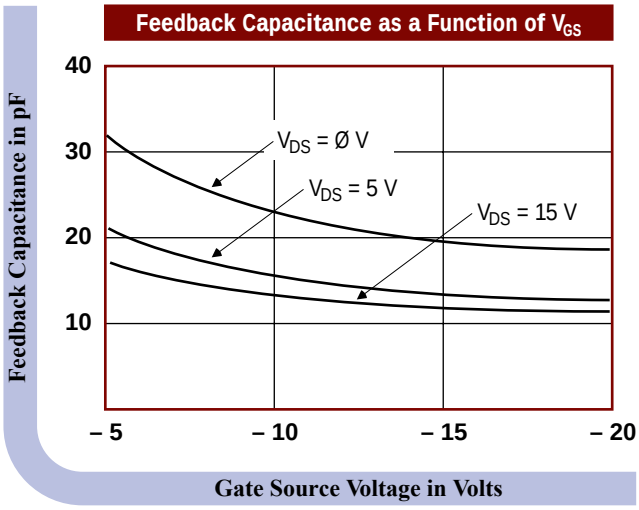
$R_{DS(ON)}$ as a Function of $V_{GS(OFF)}$



Input Capacitance as a Function of V_{GS}



Feedback Capacitance as a Function of V_{GS}



NJ903L Process

Silicon Junction Field-Effect Transistor

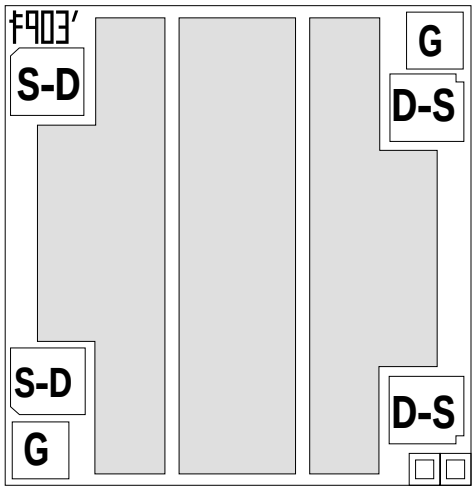
- Low-Current
- Low Gate Leakage Current
- High Input Impedance

Absolute maximum ratings at 25°C free-air temperature.

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Device in this Databook based on the NJ903L Process.

Datasheet
IF9030



Die Size = 0.040" X 0.040"
All Bond Pads = 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		NJ903L Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20	– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 5	– 500	pA	V_{GS} = – 15V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	5		500	mA	V_{DS} = 10V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.1		– 3	V	V_{DS} = 10V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Input Capacitance	C_{iss}		50		pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Feedback Capacitance	C_{rss}		18		pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		0.5		nV/√HZ	V_{DG} = 4V, I_D = 5 mA	f = 1 kHz

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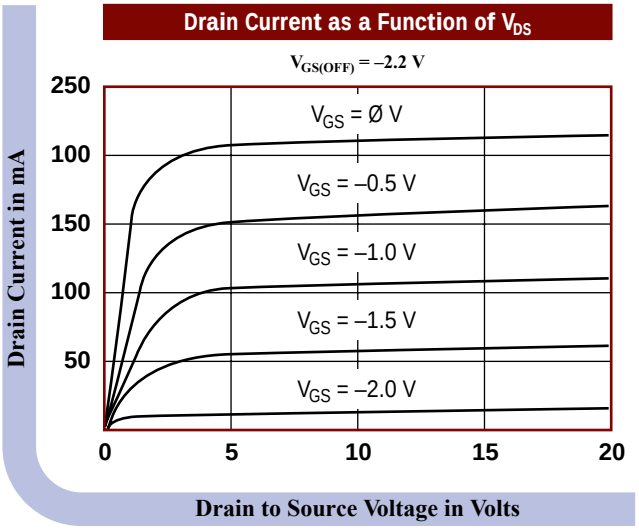
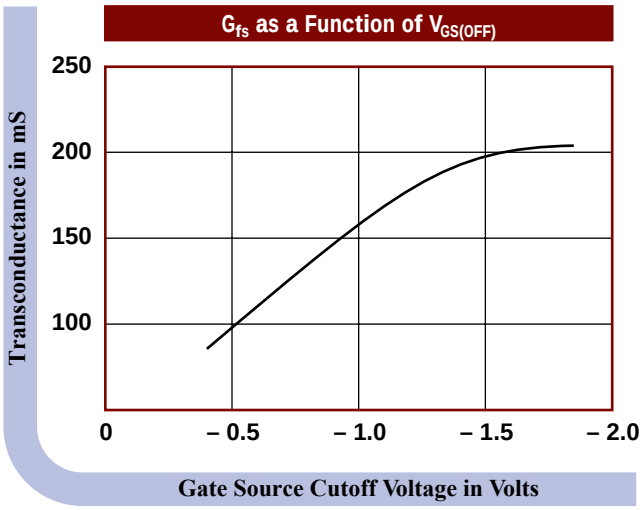
NJ903L Process

Silicon Junction Field-Effect Transistor

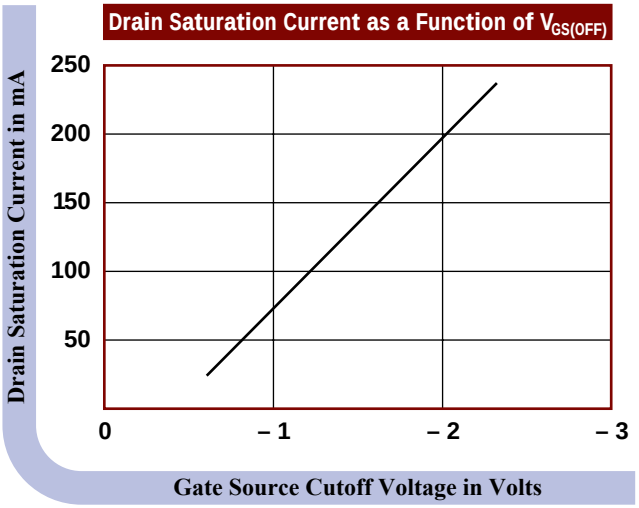
Drain Current as a Function of V_{DS}



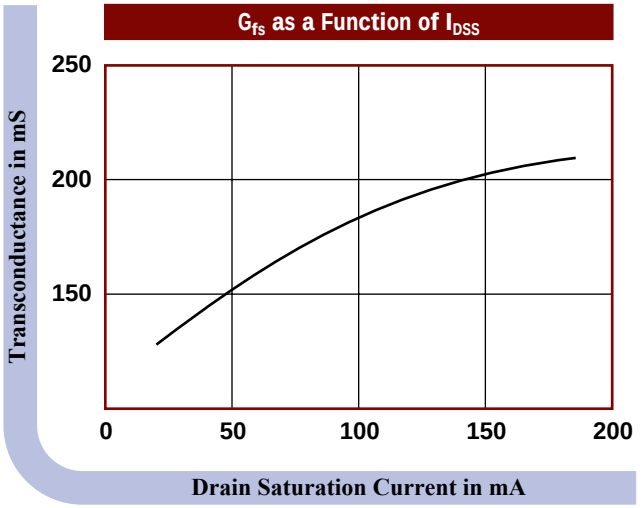
G_{fs} as a Function of $V_{GS(OFF)}$



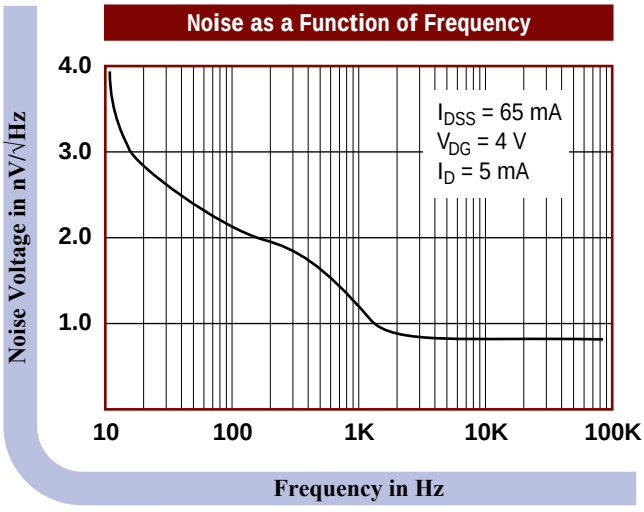
Drain Saturation Current as a Function of $V_{GS(OFF)}$



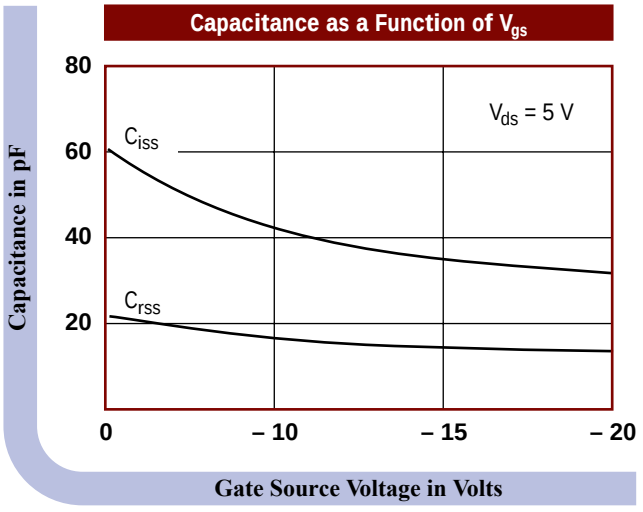
G_{fs} as a Function of I_{DSS}



Noise as a Function of Frequency



Capacitance as a Function of V_{gs}



NJ1800D Process

Silicon Junction Field-Effect Transistor

- **Ultra Low-Noise Pre-Amplifier**

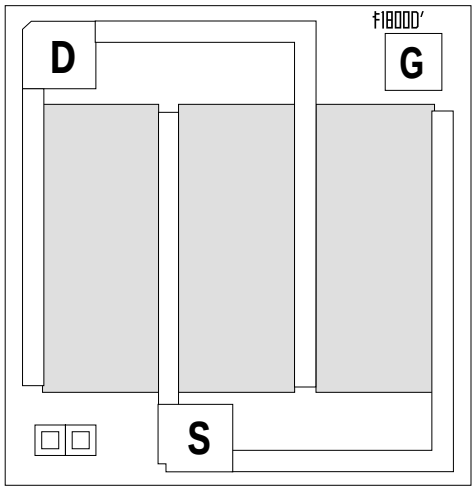
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Devices in this Databook based on the NJ1800D Process.

Datasheet

U290, U291



Die Size = 0.052" X 0.052"
All Bond Pads ≥ 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		NJ1800D Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 20	– 30		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 30	– 100	pA	V_{GS} = – 10V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	50		1000	mA	V_{DS} = 10V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.1		– 7	V	V_{DS} = 10V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance (Pulsed)	g_{fs}		350		mS	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Drain Source ON Resistance	$r_{ds(on)}$	2		7	Ω	I_D = 1 mA, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		100		pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{rss}		50		pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 MHz

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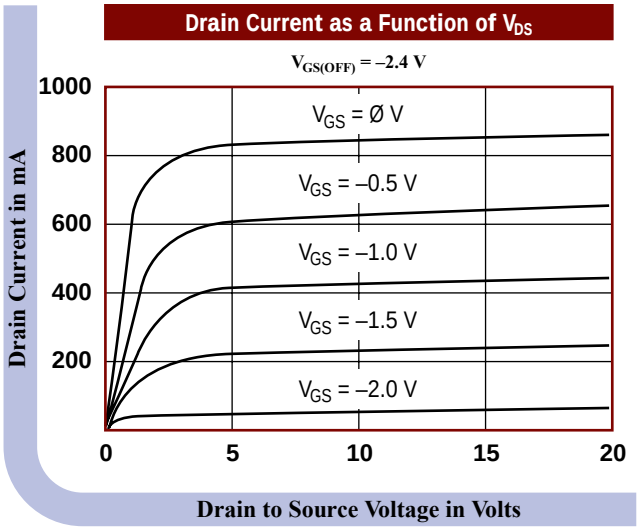
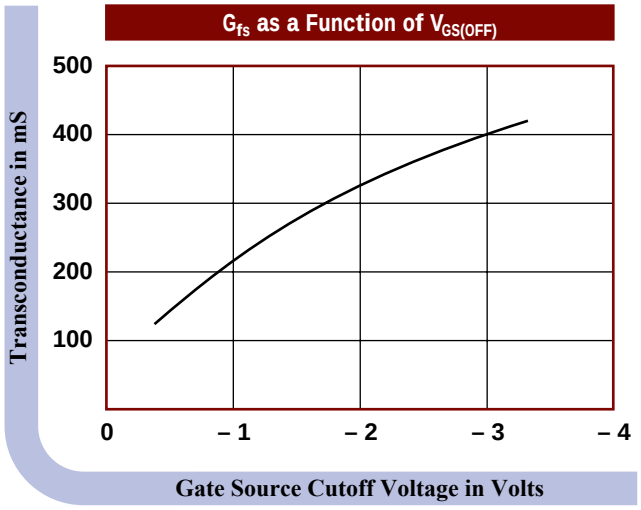
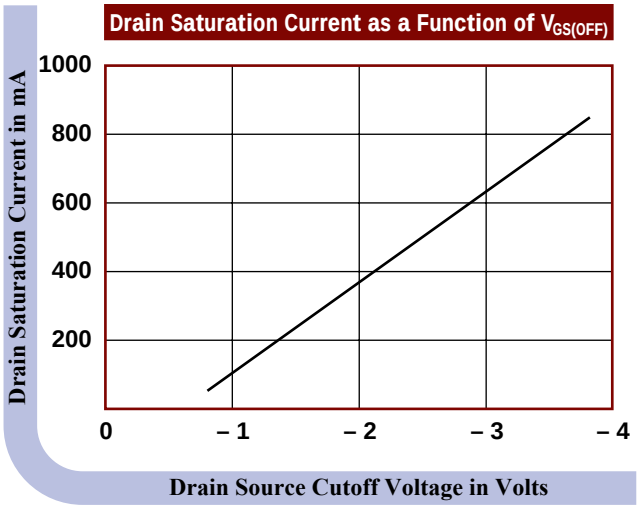
Drain Current as a Function of V_{DS}



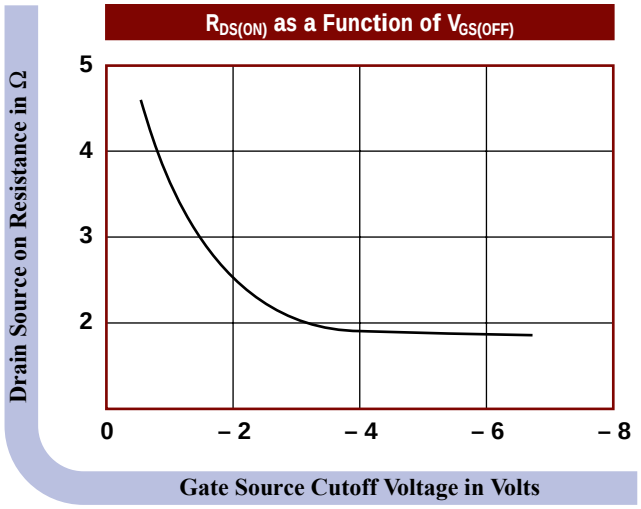
G_{fs} as a Function of $V_{GS(OFF)}$



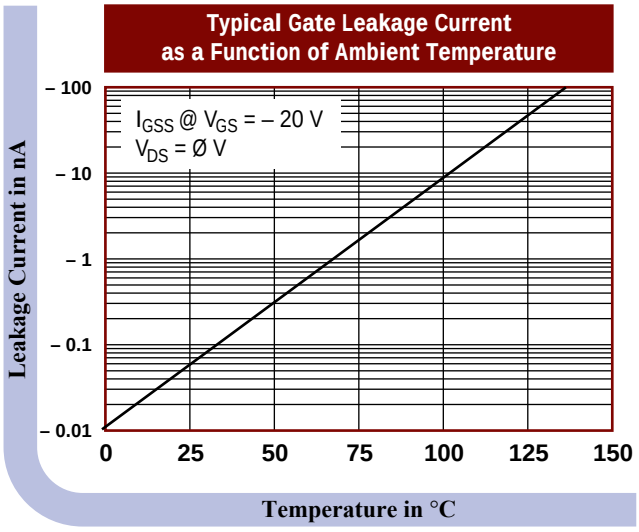
Drain Saturation Current as a Function of $V_{GS(OFF)}$



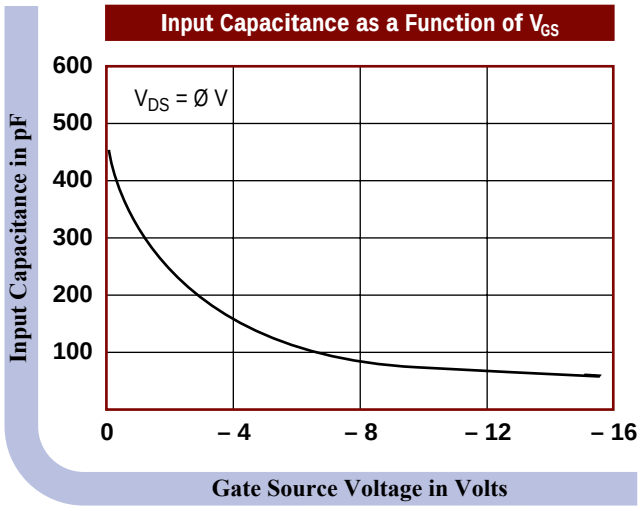
$R_{DS(ON)}$ as a Function of $V_{GS(OFF)}$



Typical Gate Leakage Current as a Function of Ambient Temperature



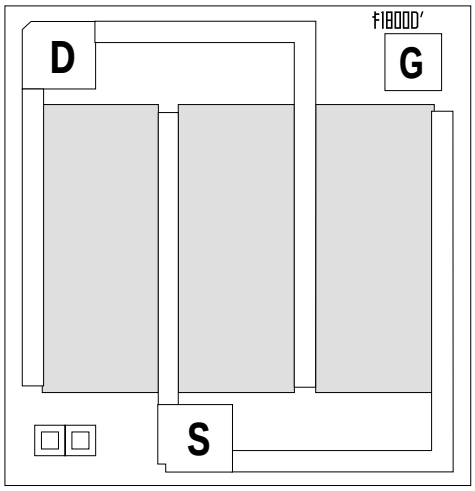
Input Capacitance as a Function of V_{GS}



NJ1800DL Process

Silicon Junction Field-Effect Transistor

- Low-Current
- Low Gate Leakage Current
- High Input Impedance
- Low-Noise



Die Size = 0.052" X 0.052"
All Bond Pads ≥ 0.004" Sq.
Substrate is also Gate.

Absolute maximum ratings at 25°C free-air temperature.

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Device in this Databook based on the NJ1800DL Process.

Datasheet

IF1801

At 25°C free air temperature:		NJ1800DL Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 15	– 25		V	I_G = – 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		– 30	– 100	pA	V_{GS} = – 10V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	50		800	mA	V_{DS} = 10V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.1		– 4	V	V_{DS} = 10V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Forward Transconductance (Pulsed)	g_{fs}		350		mS	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		160		pF	I_D = 1 mA, V_{GS} = ØV	f = 1 MHz
Feedback Capacitance	C_{rss}		50		pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 MHz
Equivalent Noise Voltage	$\bar{e}_N$		0.7		nV/√HZ	V_{DG} = 4V, I_D = 5 mA	f = 1 kHz

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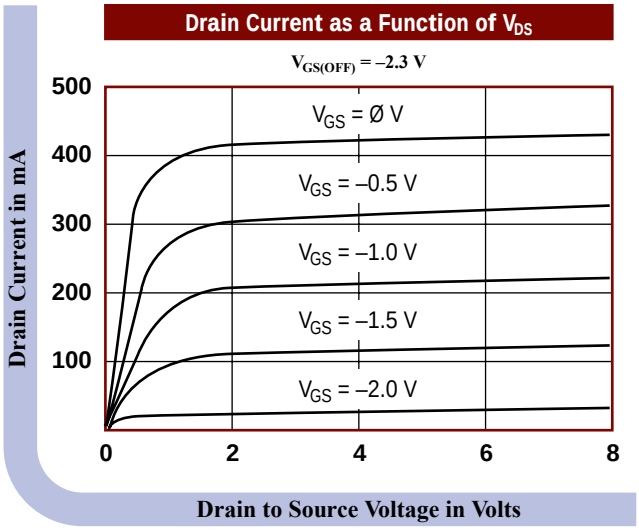
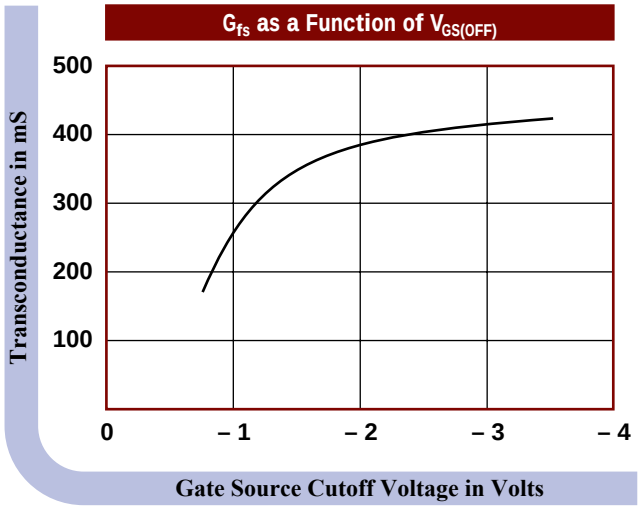
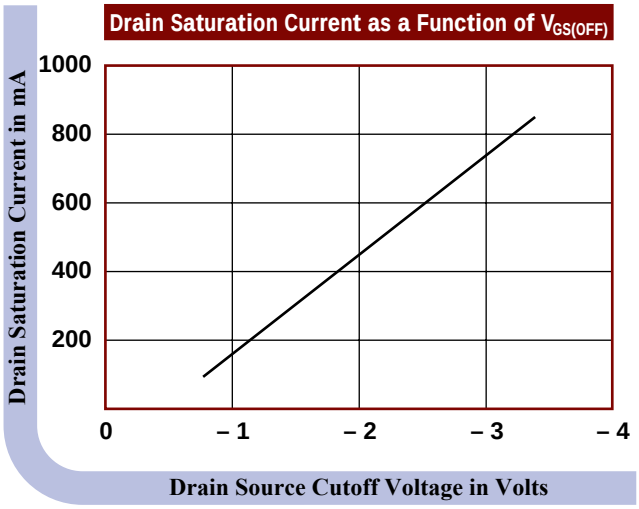
Drain Current as a Function of V_{DS}



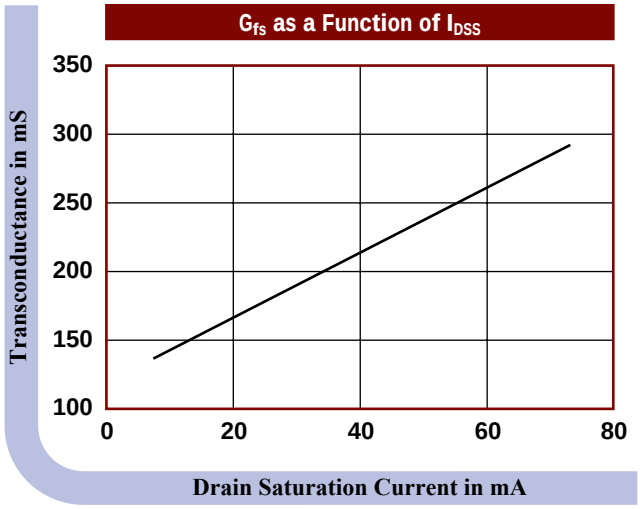
G_{fs} as a Function of $V_{GS(OFF)}$



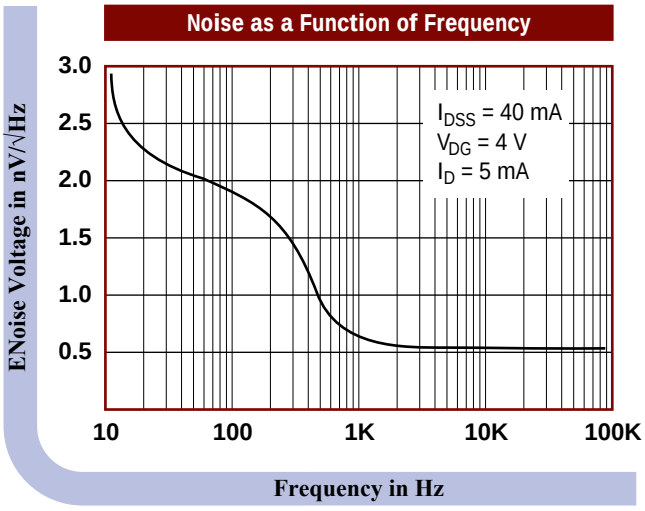
Drain Saturation Current as a Function of $V_{GS(OFF)}$



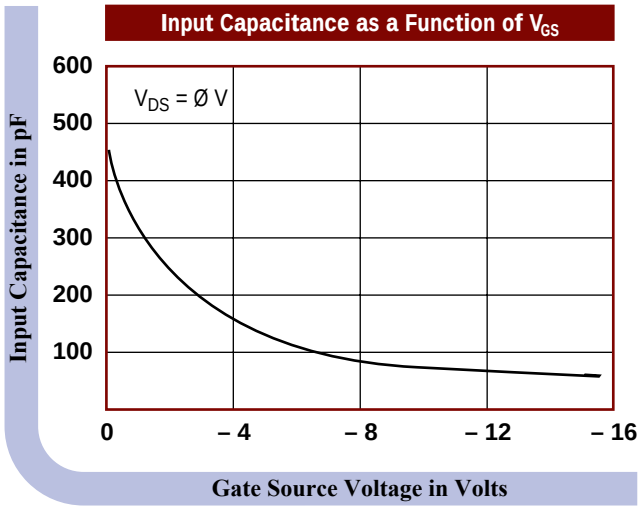
G_{fs} as a Function of I_{DSS}



Noise as a Function of Frequency



Input Capacitance as a Function of V_{GS}



NJ3600L Process

Silicon Junction Field-Effect Transistor

- Large Capacitance Detector Pre-Amplifier

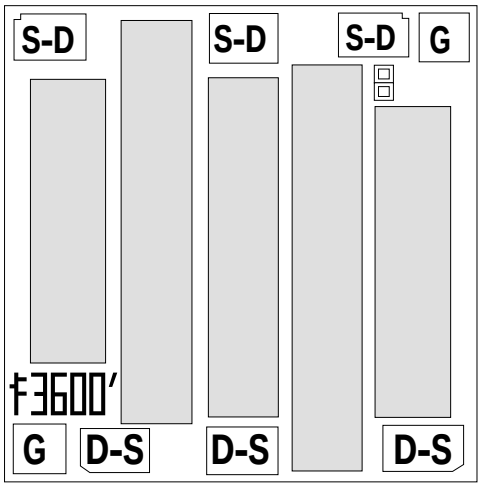
Absolute maximum ratings at TA = 25°C

Gate Current, Ig	10 mA
Operating Junction Temperature, Tj	+150°C
Storage Temperature, Ts	– 65°C to +175°C

Device in this Databook based on the NJ3600L Process.

Datasheet

IF3601
IF3602



Die Size = 0.074" X 0.074"
All Bond Pads ≥ 0.004" Sq.
Substrate is also Gate.

At 25°C free air temperature:		NJ3600L Process					
Static Electrical Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 15	– 22		V	I_G = 1 µA, V_{DS} = ØV	
Reverse Gate Leakage Current	I_{GSS}		100	1000	pA	V_{GS} = 10V, V_{DS} = ØV	
Drain Saturation Current (Pulsed)	I_{DSS}	50		1000	mA	V_{DS} = 10V, V_{GS} = ØV	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 0.5		– 3	V	V_{DS} = 10V, I_D = 1 nA	
Dynamic Electrical Characteristics							
Drain Source ON Resistance	$r_{ds(on)}$	1		4	Ω	I_D = 1 mA, V_{GS} = ØV	f = 1 kHz
Forward Transconductance (Pulsed)	g_{fs}		750		mS	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Input Capacitance	C_{iss}		650		pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Feedback Capacitance	C_{rss}		80		pF	V_{DS} = 10V, V_{GS} = ØV	f = 1 kHz
Equivalent Noise Voltage	$\bar{e}_N$		0.35		nV/√HZ	V_{DG} = 3V, I_D = 5 mA	f = 30 Hz

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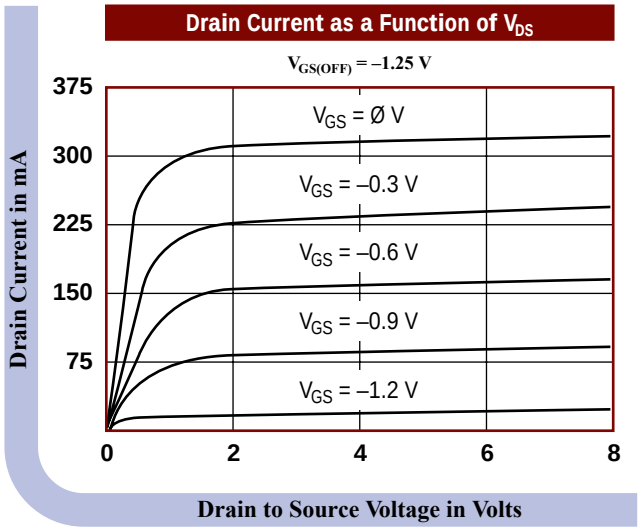
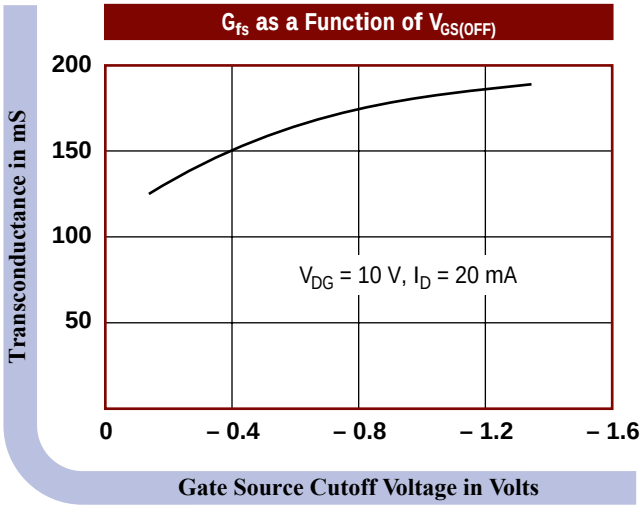
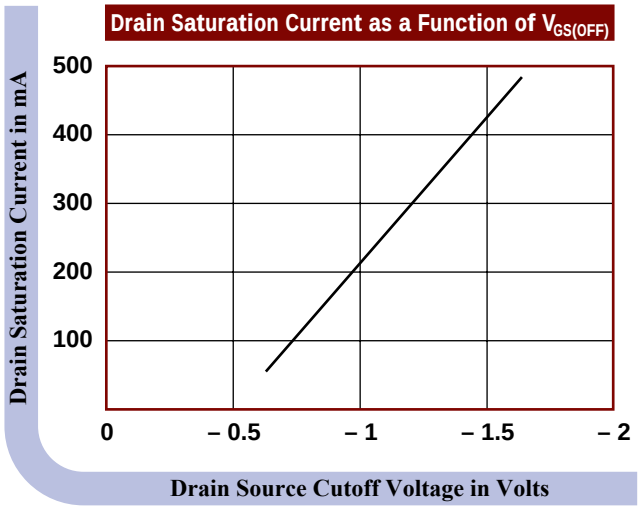
Drain Current as a Function of V_{DS}



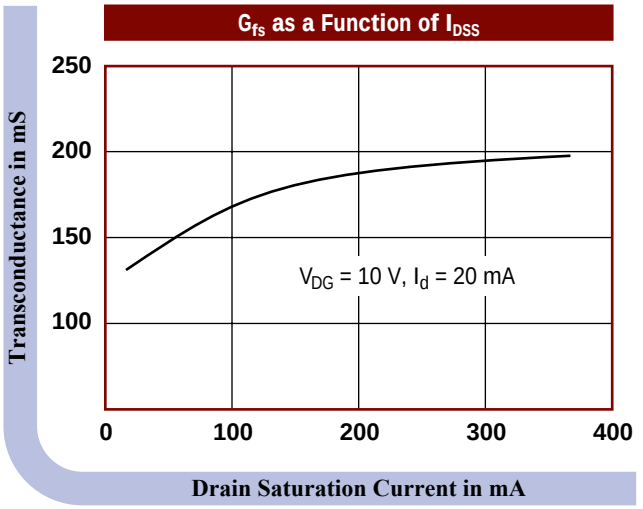
G_{fs} as a Function of $V_{GS(OFF)}$



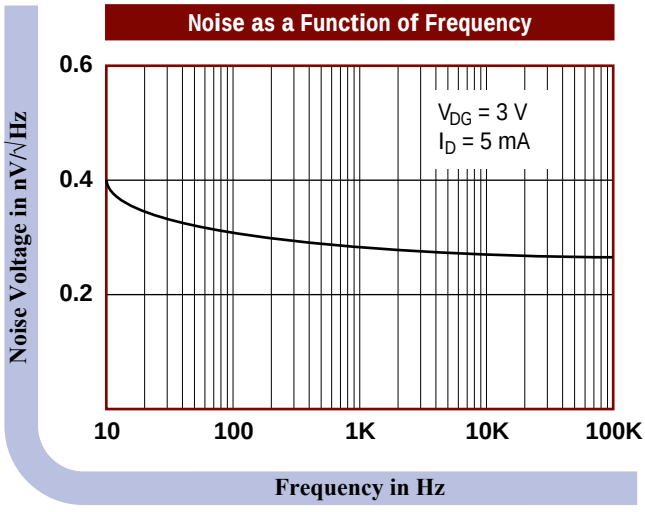
Drain Saturation Current as a Function of $V_{GS(OFF)}$



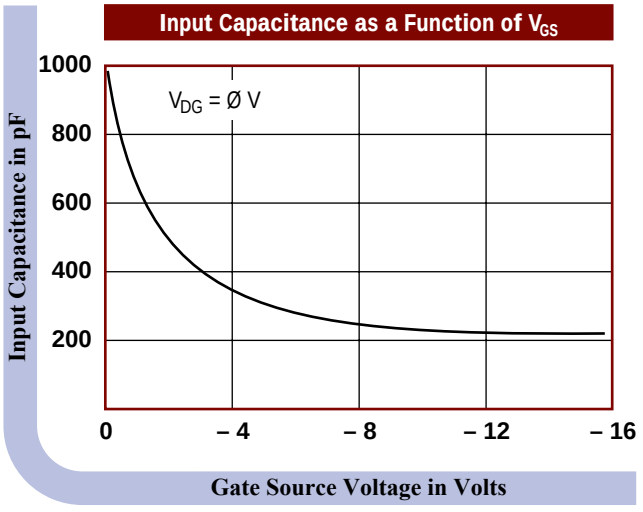
G_{fs} as a Function of I_{DSS}



Noise as a Function of Frequency



Input Capacitance as a Function of V_{GS}



Semiconductor Databook

Section G

Package Information

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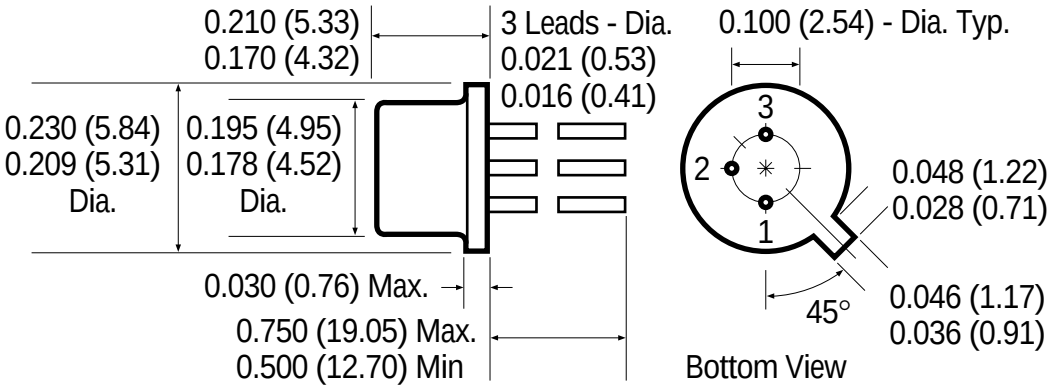
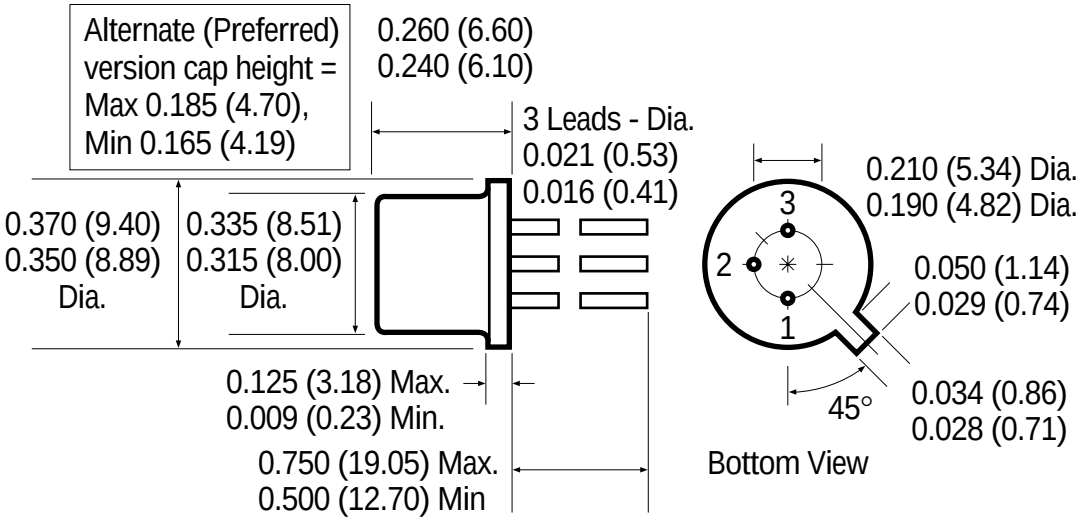
TO-18 Package

Dimensions in Inches (mm)



TO-39 Package

Dimensions in Inches (mm)



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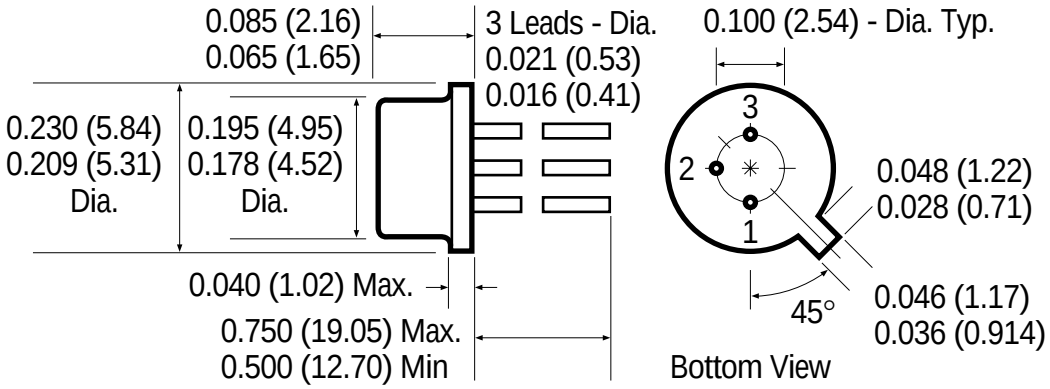
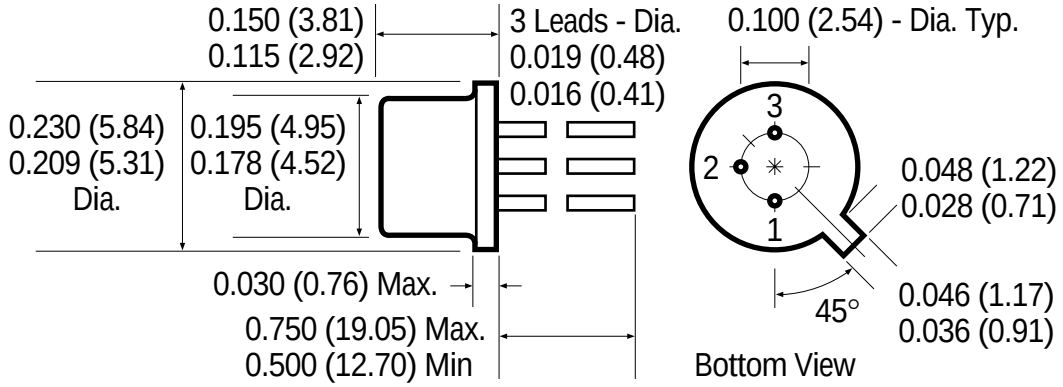
TO-46 Package

Dimensions in Inches (mm)



TO-52 Package

Dimensions in Inches (mm)



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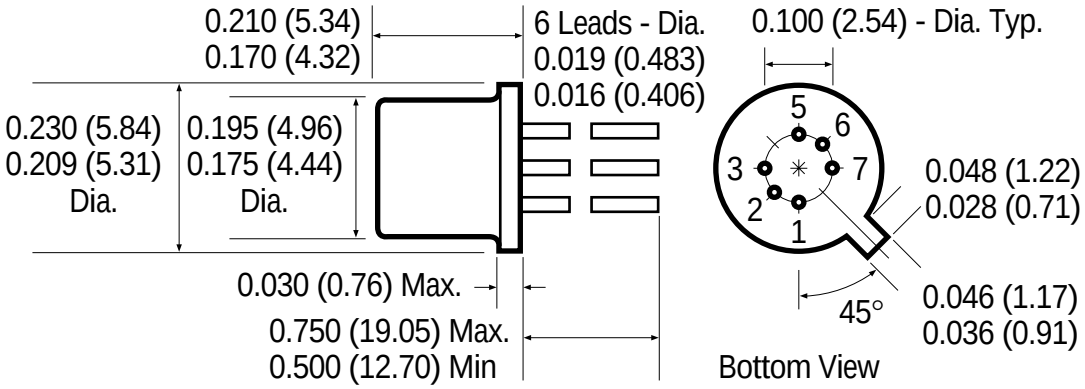
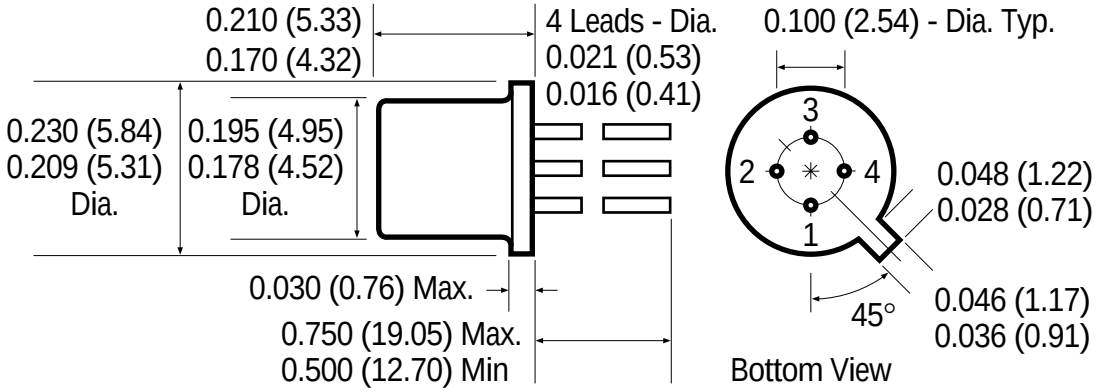
TO-71 Package

Dimensions in Inches (mm)



TO-72 Package

Dimensions in Inches (mm)



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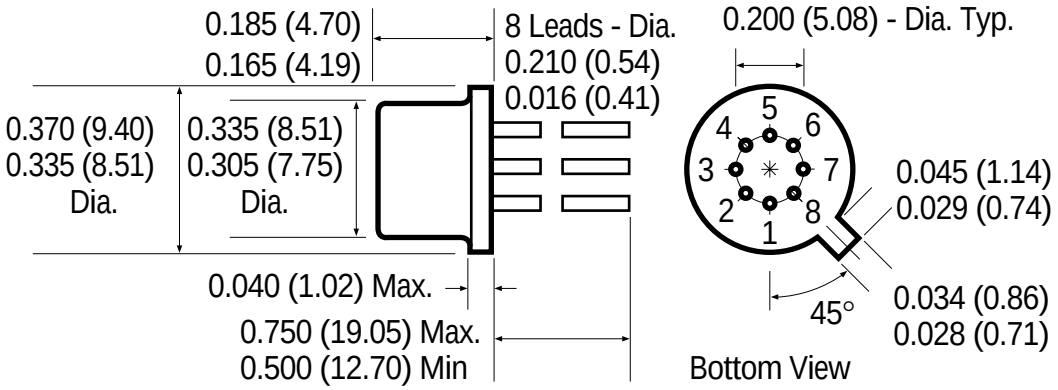
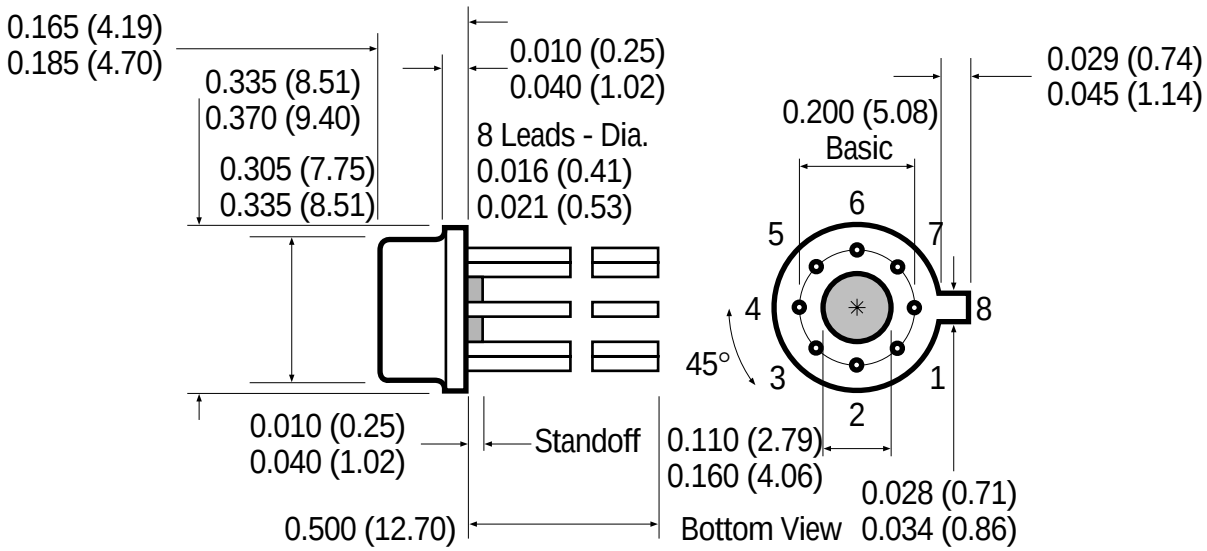
TO-78 Package

Dimensions in Inches (mm)



TO-99 Package

Dimensions in Inches (mm)



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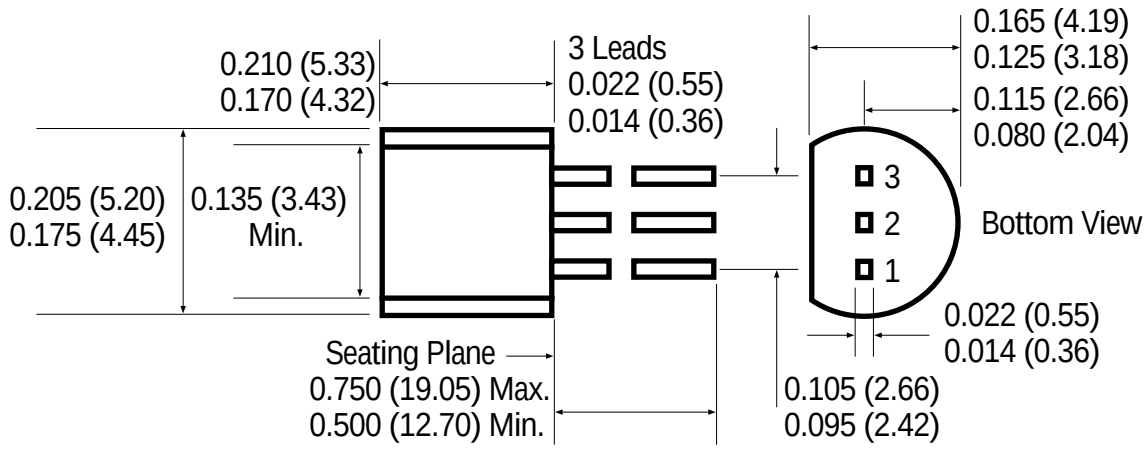
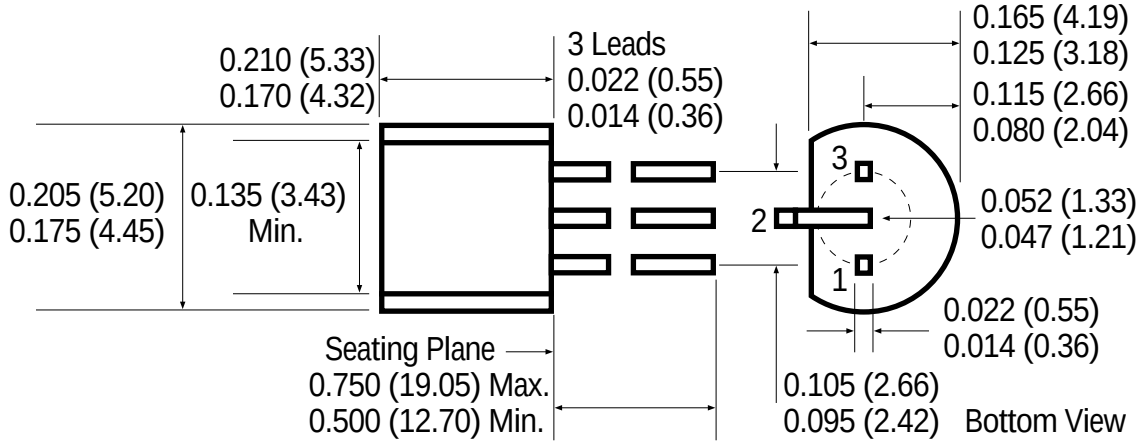
TO-226AA Package (TO-92)

Dimensions in Inches (mm)



TO-226AB Package (TO-92/18)

Dimensions in Inches (mm)



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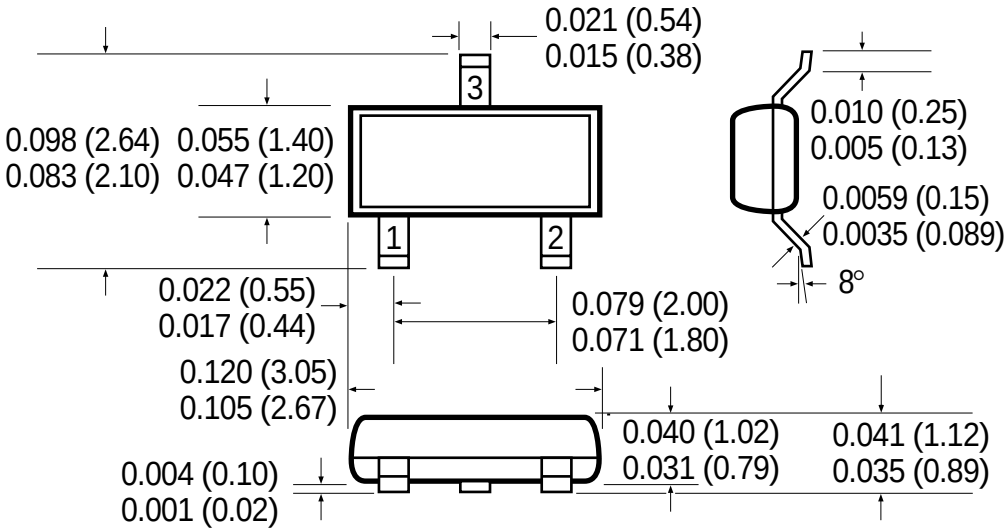
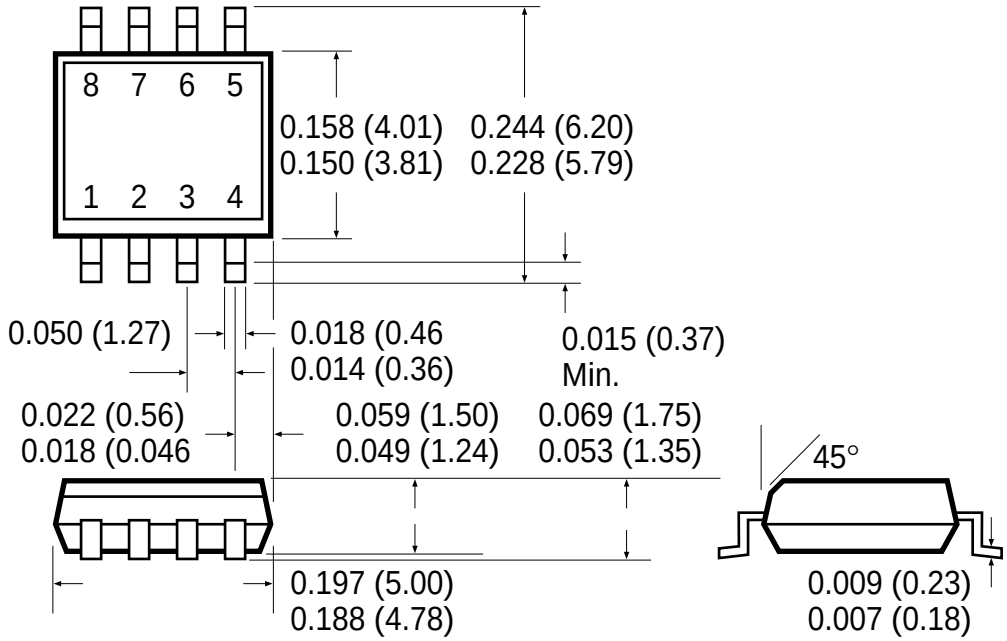
TO-236AB Package (SOT-23)

Dimensions in Inches (mm)



SOIC-8 Package

Dimensions in Inches (mm)



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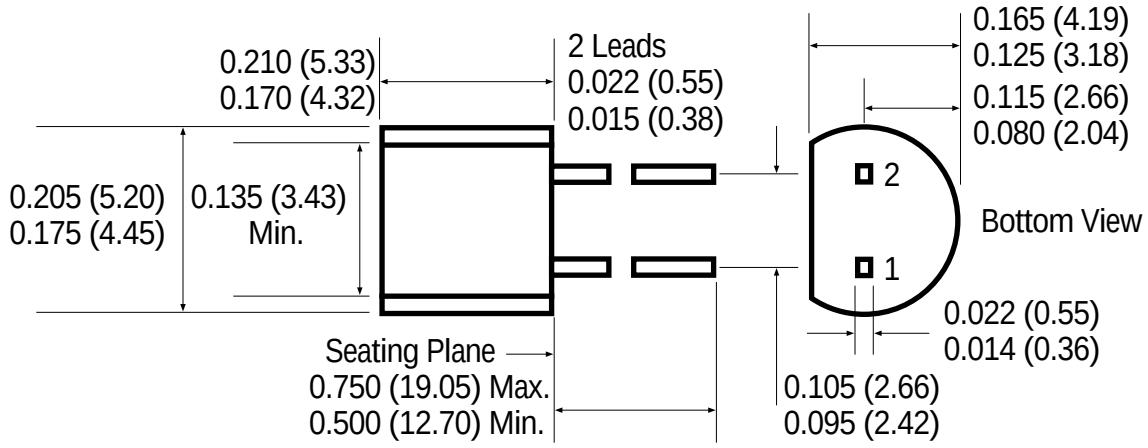
TO-92 Two-Lead Package

Dimensions in Inches (mm)



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Section H

Application Notes

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Junction Field Effect Transistors

InterFET Application Notes

Introduction

The field effect transistor was actually conceived before the more familiar bipolar transistor. Due to limited technology and later the rapid rise of the bipolar device it was not pursued until the early 1960's as a viable semiconductor alternative. At this time further investigation of the field effect transistor and advances in semiconductor process technology lead to the types in use today.

Field effect transistors include the Junction FET (JFET) and the MOSFET. The MOSFET is a metal-oxide semiconductor technology and is sometimes referred to as the IGFET or Insulated Gate FET. All field effect transistors are majority carrier devices. This means that current is conducted by the majority carrier species present in the channel of the FET. This majority carrier consists of hole for p-channel devices and electrons for n-channel devices. The JFET operates with current flow through a controlled channel in the semiconductor material. The MOSFET creates a channel under the insulated gate region which is produced by an electric field induced in the semiconductor by applying a voltage to the gate. The JFET is a depletion mode device whereas the MOSFET can operate as a depletion mode or an enhancement mode device. Depletion mode devices are controlled by depleting the current channel of charge carriers. Enhancement mode devices are controlled by enhancing the channel with additional charge carriers.

The JFET

The junction field effect transistor in its simplest form is essentially a voltage controlled resistor. The resistive element is usually a bar of silicon. For an N-channel JFET this bar is an N-type material sandwiched between two layers of P-type material. The two layers of P-type material are electrically connected together and are called the gate. One end of the N-type bar is called the source and the other is called the drain. Current is injected into the channel from the source terminal, and collected at the drain terminal. The interface region of the P- and the N-type materials forms a P-N junction as shown in Figure 1.

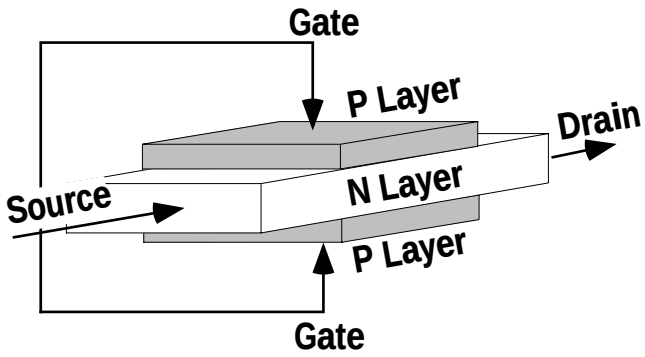

Figure 1

As in any material, the resistance of the conducting channel is defined by:

(1) $R = \rho l / A$

where R = total channel resistance

ρ = resistivity of the silicon

l = length of the conducting path

A = cross sectional area of the conducting path

Figure 2 illustrates a JFET with the two gate areas electrically connected together, as are the source and the drain. Application of a reverse bias voltage on the drain/gate terminals results in the formation of depletion regions at the PN junction. Increasing the voltage causes the depletion regions to reach further into the channel and effectively reduces its cross-sectional area. It can be seen from Equation 1 that this increases the channel resistance. Continuing to increase the voltage will result in the depletion regions touching in the middle of the channel. The channel is then said to be pinched off and the voltage required to cause this is called the pinch-off voltage.

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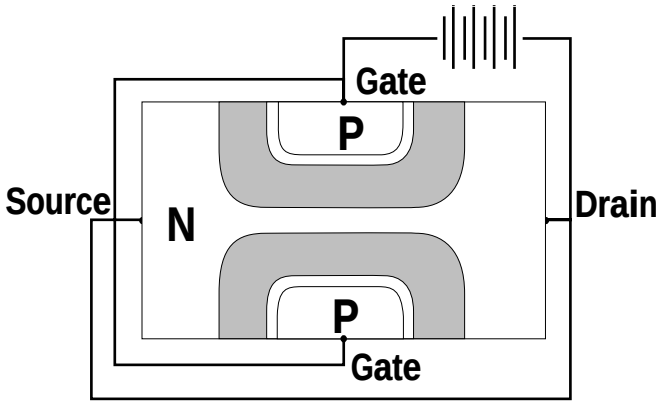

Figure 2

Connecting the gate to the source and applying a voltage between the drain and source also produces the formation of a depletion region at the PN junction. The depletion region is then concentrated at the drain end of the channel, as shown in Figure 3. Once again, increasing the voltage causes the depletion region to spread farther into the channel. This results in a corresponding increase in channel resistance due to the reduction in the cross sectional area of the channel. The voltage at which the two depletion regions just touch in the middle of the channel is called the drain saturation voltage. Operation of the JFET at voltages below and above the drain saturation voltage are referred to the linear (or resistive) and saturation regions, respectively. When operated in the saturated region, changes in voltage cause little change in channel net current. The amount of current which will flow in the channel of a JFET operating in this manner is called the drain saturation current. The JFET is normally operated in the saturated region when used as an amplifier.

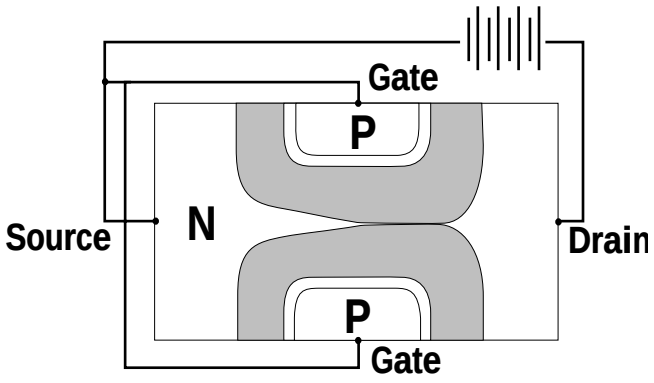

Figure 3

The application of an additional voltage between the gate and the source in reverse bias condition causes the depletion region to become more evenly distributed throughout the channel. This further increases the channel resistance and reduces the amount of channel current with a given drain voltage. Continuing to increase the gate voltage to the pinchoff point will reduce the drain current to a very low value, effectively zero. This illustrates the operation of the JFET by showing that a voltage modulation of the gate results in a corresponding drain current modulation.

A typical set of JFET characteristic curves is shown in Figure 4. The three primary regions shown on the graph are the linear region, the saturated region, and the breakdown region. The linear region is that region where the drain to source voltage is less than the drain saturation voltage. It can be seen that the voltage current relationship is a linear function. At the point where the drain to source voltage reaches the drain saturation voltage, the saturated region begins. The curves illustrate that increasing the gate reverse voltage reduces the drain current as well as the drain saturation voltage. This also shows the manner in which the drain current is modulated when modulating the gate voltage. The final region of interest is the breakdown region. This is the point at which

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the gate to drain reverse biased depletion region breaks down due to the voltage applied and the current is no longer blocked. When operated in this manner the current flow is essentially uncontrolled and the device could be damaged and destroyed.

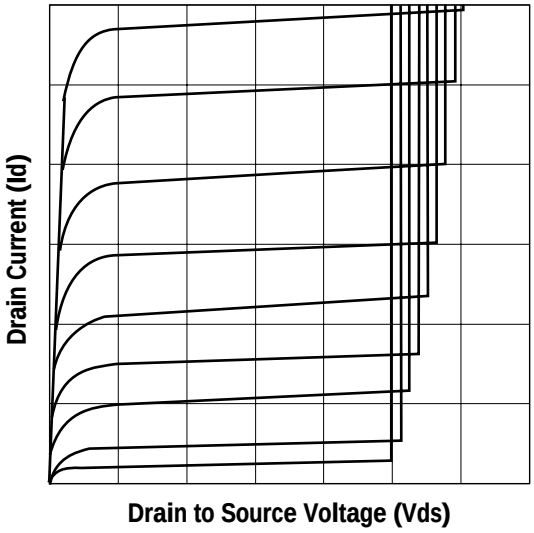

Figure 4

A typical set of JFET characteristic curves.

Conclusions

The previous discussion of the JFET illustrates that:

1. The JFET is basically a voltage controlled resistor,
2. The JFET operates as a depletion mode device, and,
3. The JFET performs as a voltage controlled current amplifier.

The JFET is preferred in many circuit applications due to its high input impedance because it is a reverse biased PN junction. Its operation is that of the flow of majority carriers only and therefore acts as a resistive switch. It also is inherently less noisy than bipolar devices and can be used in low signal level applications.

References:

1. Millman, J. and Halkias, C.: *Integrated Electronics Analog and Digital Circuits and Systems*, McGraw-Hill Book Company, New York, 1972
2. Sevin, L.J.: *Field Effect Transistors*, McGraw Hill Book Co., New York, 1965
3. Grove, A.S.: *Physics and Technology of Semiconductor Devices*, John Wiley And Son, New York, 1967
4. Grebene, A.B.: *Analog Integrated Circuit Design*, Van Nostrand Reinhold, New York, 1972
5. Pierce, J.F. and Paulus, T.: *Applied Electronics*, Charles E. Merrill, Columbus, Ohio, 1972

Introduction

The Junction Field Effect Transistor (JFET) exhibits characteristics which often make it more suited to a particular application than the bipolar transistor. Some of these applications are:

High Input Impedance Amplifier
Low-Noise Amplifier
Differential Amplifier
Constant Current Source
Analog Switch or Gate
Voltage Controlled Resistor

In this application note, these applications, along with a few others, will be discussed. Only the basics will be shown without going into too much technical detail.

Basic JFET Amplifier Configurations

There are three basic JFET circuits: the common source, the common gate, and the common drain as shown in Figure 1. Each circuit configuration describes a two port network having an input and an output. The transfer function of each is also determined by the input and output voltages or currents of the circuit.

Common Source

Common Gate

Common Drain

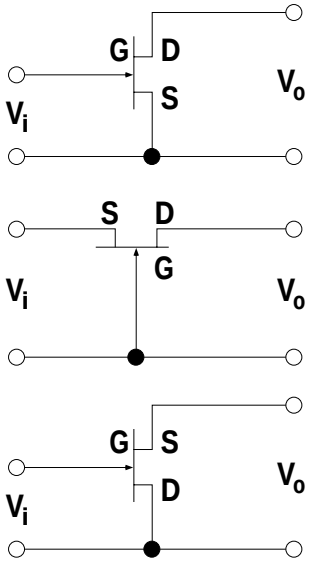

Figure 1

Basic JFET Amplifier Circuit Configurations

The most common configuration for the JFET as an amplifier is the common source circuit. For an N-channel device the circuit would be biased as shown in Figure 2

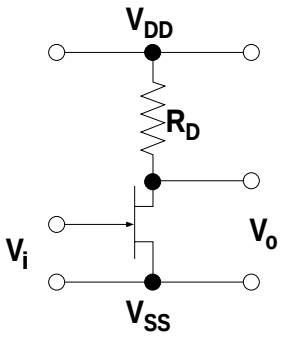

Figure 2

Basic Common Source Amplifier Circuit Biasing Configuration

Since the N-Channel JFET is a depletion mode device and is normally on, a gate voltage which has a negative polarity with respect to the source is required to modulate or control the drain current. This negative voltage can be provided by a single positive power supply using the self biasing method shown in Figure 3. This is accomplished by the voltage which is dropped across the source resistor, Rs, according to the current flowing through it. The gate-to-source voltage is then defined as:

(1) $V_{GS} = I_D \times R_S$

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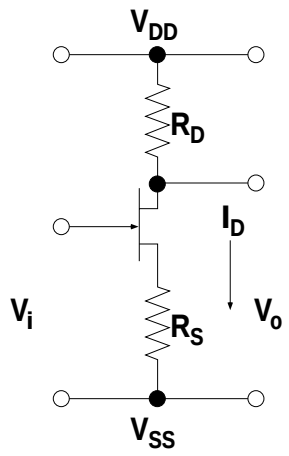

Figure 3

Common Source Amplifier
Using VGS Self-Biasing Method

The circuit of Figure 3 also defines a basic single stage JFET amplifier. The source resistor value is determined by selecting the bias point for the circuit from the characteristic curves of the JFET being used. The value of the drain resistor is then chosen from the required gain of the amplifier and the value of the drain current which was previously selected in determining the gate voltage. The value of this resistor must also allow the circuit to have sufficient dynamic range, or voltage swing, required by the following stage. The following stage could be anything from another identical circuit to a loud speaker for an audio system. The voltage gain of this circuit is then defined as:

(2) $A_V = (g_m \times Z_l) / (1 + g_m \times R_S)$

where A_V = the voltage gain

g_m = the forward transconductance or gain of the JFET

Z_l = the equivalent load impedance

R_S = the value of the source resistor

The effect of the source resistor on the gain of the circuit can be removed at higher frequencies by connecting a capacitor across the source resistor. This then results in an amplifier which has a gain of:

(3) $A_V = g_m \times Z_l$

but only at frequencies above that defined by the resistor-capacitor network in the source circuit. This frequency is defined as:

(4) $f_{lo} = 1 / (2\pi \times R_S \times C_S)$

where f_{lo} = the low frequency corner

π = the constant 3.1418

R_S = the value of the source resistor in ohms

C_S = the value of the source capacitor in farads

This circuit also has a high input impedance, generally equal to the value of the input impedance of the JFET.

A Low-Noise Amplifier

A minor change to the circuit of Figure 3 describes a basic single stage low-noise JFET amplifier. Figure 4 shows that this change only incorporates a resistor from the gate to Vss. This resistor supplies a path for the gate leakage current in an AC coupled circuit. Its value is chosen by the required input impedance of the amplifier and its desired low-noise characteristics. The noise components of this amplifier are the thermal noise of the drain and gate resistors plus the noise components of the JFET. The noise contribution of the JFET is from the shot noise of the gate leakage current, the thermal noise of the channel resistance, and the frequency noise of the channel. These noise characteristics are generally lower than those found in bipolar transistors if the JFET is properly selected for the application. The voltage gain of the circuit is again defined by Equation (3).

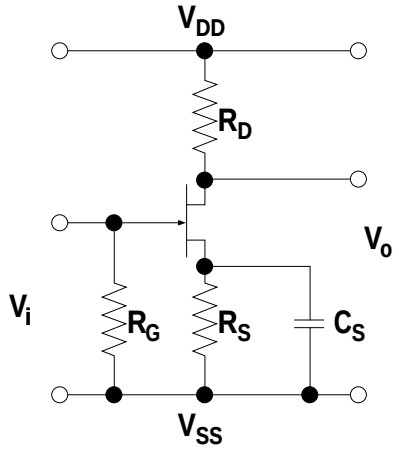

Figure 4

Low-Noise JFET Single Stage Amplifier with Source By-Pass Capacitor, CS

The JFET Differential Amplifier

Another application of the JFET is the differential amplifier. This configuration is shown in Figure 5. The differential amplifier requires that the two transistors be closely matched electrically and physically located near each other for thermal stability. Either input and either output can be used or both inputs and only one output and conversely only one input and both outputs can be used. For the configuration shown the source resistor is chosen to determine the gate to source bias voltage, remembering that the current will be twice that of each of the JFET drain currents. The value of the drain resistors is chosen to provide a suitable dynamic range at the output. The gain of this circuit is defined by:

(5) $A_V = 2x\ (g_m \times R_l) / (1 + g_m \times R_S)$

where all the terms in the equation have previously been defined.

This circuit configuration is very useful as a high input impedance stage to be connected to the input of a low cost operational amplifier, such as the popular 741 Op-Amp

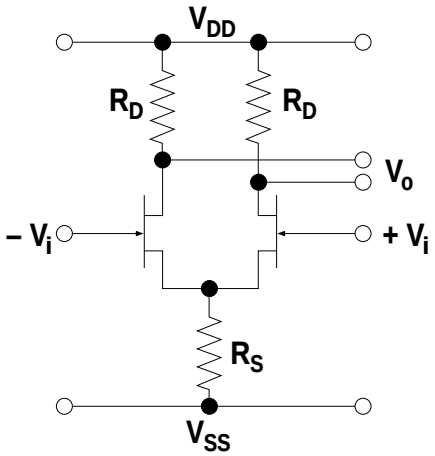

Figure 5

The Matched Pair JFET Differential Amplifier

The JFET Constant Current Source

A constant current source using a JFET is shown in Figure 6. This circuit configuration has many useful applications ranging from charging circuits for integrators or timers to replacing the source resistor in the differential amplifier shown in Figure 5. The current provided by the constant current source of Figure 6 is defined as

(6) $I_D = I_{DSS}\ [1 - (V_{GS} / V_p)]^2$

where I_D = the drain current or magnitude of current sourced

I_{DSS} = the drain saturation current of the JFET

V_{GS} = $I_D \times R_S$

V_p = the JFET pinch-off voltage

2 = the squared value of the term in brackets.

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It can be readily seen that the use of this circuit in the source circuit of the differential amplifier of Figure 5 would improve the circuit voltage gain as well as reduce the amplifier noise and enhance the CMRR of the amplifier.

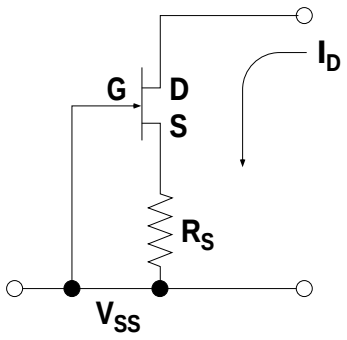

Figure 6

JFET Constant Current Source

The JFET Analog Switch

Figures 7, 8, and 9 show three different applications for the JFET to be used as an analog switch or gate. Figures 7 and 8 both demonstrate methods for realizing programmable gain amplifiers, while Figure 9 shows an analog multiplexer circuit using JFETs and a common op-amp integrated circuit.

It can be seen from Figure 7 that the gain of the stage can be changed by switching in any combination of feedback resistors R1 through Rn. The JFET in series with the input resistor should be of the same type as those in the feedback paths and is used for thermal stability of the circuit gain. The transfer function of the circuit of Figure 7 is approximated by:

(7) $V_o / V_i = 1 / [(1 / R_1) + (1 / R_2) + ... + (1 / R_n)] / R_i$

where R_1 through R_n = the feedback resistors

R_i = the input resistors

V_o = the output voltage

V_i = the input voltage

Note that only those feedback resistors which are switched into the circuit are to be included in the the transfer function equation.

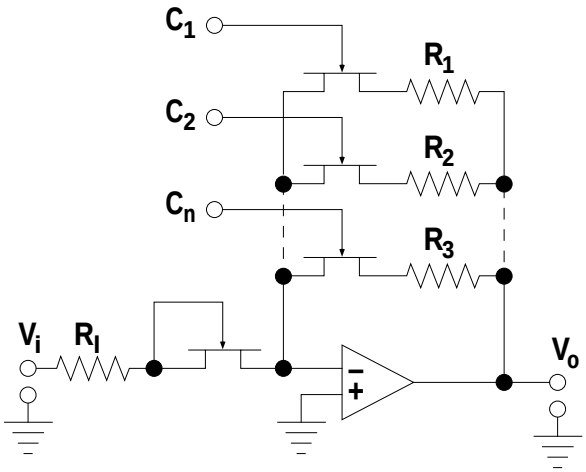

Figure 7

Programmable Gain Amplifier

The circuit of Figure 8 shows another method to realize a programmable gain amplifier using a common op-amp, four resistors, and only two JFETs. The gain of this circuit can also be changed by switching in the desired resistors by turning off the appropriate JFET thus switching in the parallel resistor. The transfer function of this circuit is approximated by:

(8) $V_o / V_i = (R_3 + R_4) / (R_1 + R_2)$

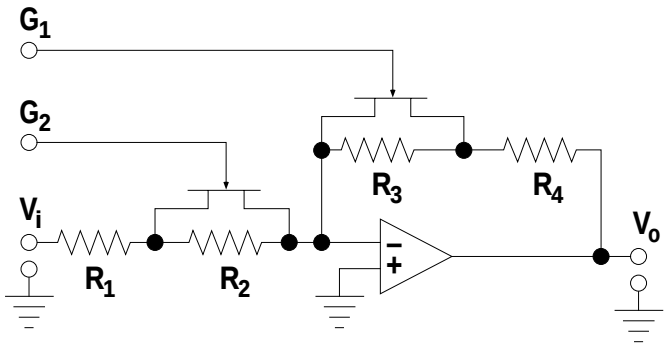

Figure 8

Programmable Gain Amplifier with 4 Resistors and 2 JFETs

It should be noted that only those resistors which are switched into the circuit are to be included in the transfer function equation.

Figure 9 shows a circuit in which the JFETs are acting as analog switches to multiplex several input signal sources to a single output source. The transfer function of this circuit is then approximated by:

(9) $V_o / V_i = R_f / R_n$

where R_f = the feedback resistor

R_n = any one of the input resistors

Further examination of this circuit shows that it can also be used as a programmable summing amplifier by switching in any combination of input signals. The transfer function is then approximated by:

(10) $V_o / V_i = (R_f / R_1) + (R_f / R_2) + ... + (R_f / R_n)$

Again in this application only those resistors which are switched into the circuit are to be included in the transfer function equation.

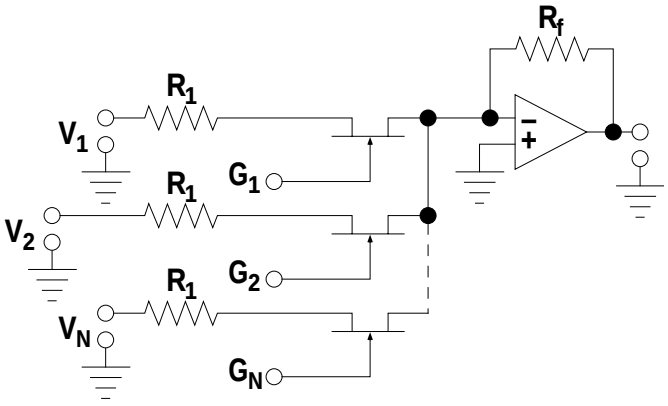

Figure 9

Analog Multiplexer Circuit which can also be used as a Programmable Summing Amplifier

The JFET Voltage Controlled Resistor

Another common application for the JFET is as a voltage controlled resistor. The JFET action in normal operation simply changes the cross sectional dimensions of the channel. When the JFET is biased in the resistive or linear region as shown in Figure 10, a change in gate voltage and the corresponding change in channel dimensions simply changes the drain to source resistance of the device.

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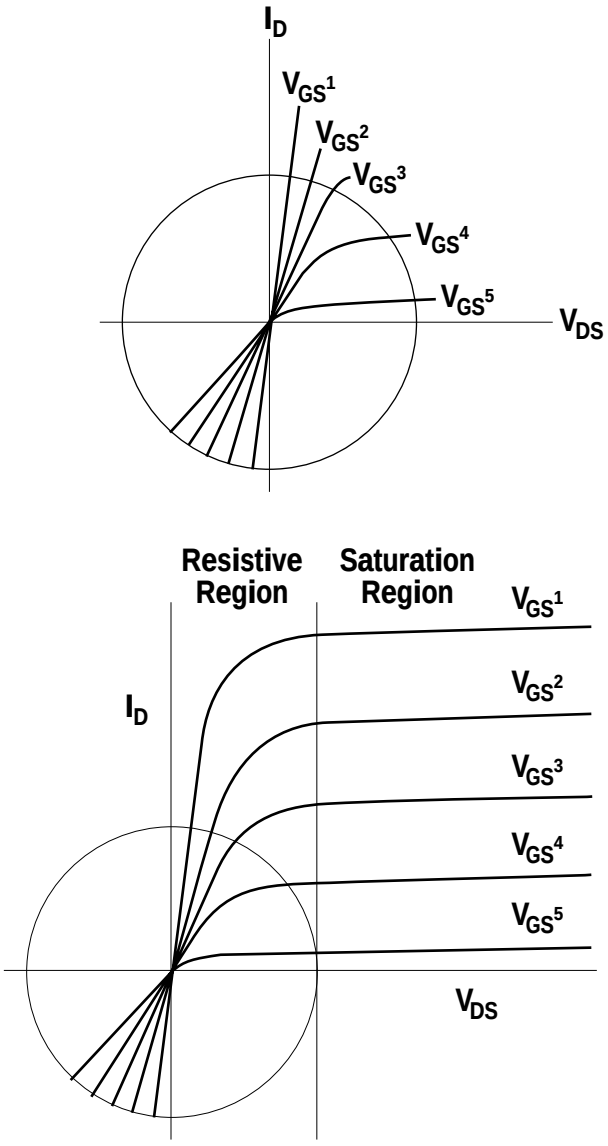

Figure 10

JFET Family of Characteristic Curves of I_D vs. V_{DS} and V_{GS}

Figure 11 depicts a JFET being used as a voltage controlled resistor (VCR). The resistance is determined from the bias point conditions selected from the curves of Figure 10. The resistance is then defined as

(11) $R_{DS} = V_{DS} / I_{DS}$

where R_{DS} = the drain to source resistance

$V_{DS} = V_o$ or the output voltage

I_{DS} = the drain current

It can readily be seen from the curves of Figure 10 that any change in the input voltage (Vi) or the gate to source voltage will cause a corresponding change in the drain current. Equation (11) indicates that there is a corresponding change in the drain to source resistance (RDS). Therefore, the resistance is controlled by the voltage applied to the gate, resulting in a voltage controlled resistor.

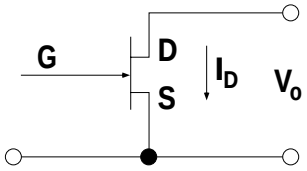

Figure 11

JFET used as a Voltage Controlled Resistor, where $R_{DS} = V_o / I_D$

Conclusions

This application note describes several useful junction field effect transistor circuit configurations. The high input impedance and low-noise circuits are often used as input stages to voltage measurement instruments such as oscilloscopes and digital volt meters.

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The differential amplifier is a very widely used circuit in applications where the difference between two voltages is to be measured, such as the input stage of an operational amplifier. The use of JFETs in this application provides high input impedance and low input leakage current. Constant current sources have many uses such as setting bias conditions for many other circuits in a system and as charging circuits for integrators and timing circuits. The analog switch is most often used in an analog multiplexer and in sample and hold circuits. Voltage controlled resistors are normally found in automatic gain control circuits and voltage controlled tuning circuits.

Therefore it is clearly seen that many applications for Junction Field Effect Transistors exist. Those discussed in this application note have many variations, refinements, and other uses. It should be noted that these applications were described in the simplest detail and additional study of the particular application should be considered before using any of the circuits presented.

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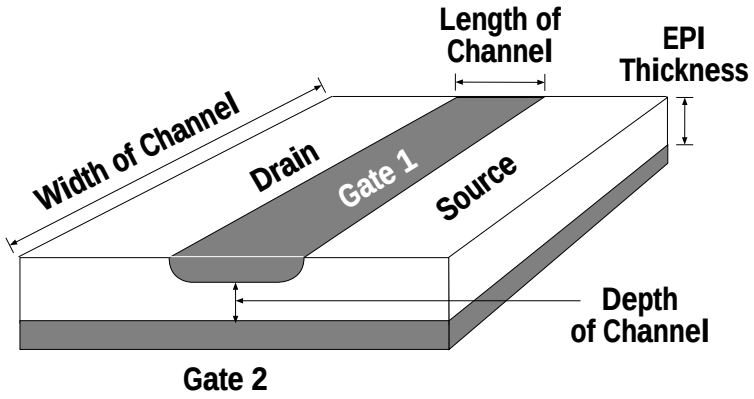
JFET Parameter - Geometry Relationships

InterFET Application Notes



Increasing Dimension will (Inc)rease, (Dec)rease, or have Ø Effect		Channel Length	Channel Width	Channel Depth	EPI Thickness	EPI Resistivity
Breakdown Voltage	BV_{GSS}	Dec	Ø	Ø	Inc	Inc
Transconductance	G_m	Dec	Inc	Inc	Dec	Dec
Max Drain Current	I_{dss}	Dec	Inc	Inc	Dec	Dec
Pinch Off Voltage	V_p	Ø	Ø	Inc	Ø	Ø
ON Resistance	r_{ds}	Inc	Dec	Dec	Inc	Inc
Input Capacitance	C_{iss}	Inc	Inc	Ø	Inc	Dec
Gate Leakage	I_{gss}	Inc	Inc	Ø	Ø	Ø
Short Circuit Input Noises	eN	Inc	Dec	Dec	Inc	Inc
Input Current Noise	I_n	Inc	Inc	Ø	Ø	Inc

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