High Performance, 145 MHz *FastFET* Op Amps

AD8065/AD8066

FEATURES

FET input amplifier
1 pA input bias current
Low cost
High speed: 145 MHz, −3 dB bandwidth (G = +1)
180 V/µs slew rate (G = +2)
Low noise
  7 nV/√Hz (f = 10 kHz)
  0.6 fA/√Hz (f = 10 kHz)
Wide supply voltage range: 5 V to 24 V
Single-supply and rail-to-rail output
Low offset voltage 1.5 mV maximum
High common-mode rejection ratio: −100 dB
Excellent distortion specifications
SFDR −88 dBc @ 1 MHz
Low power: 6.4 mA/amplifier typical supply current
No phase reversal
Small packaging: SOIC-8, SOT-23-5, and MSOP-8

APPLICATIONS

Instrumentation
Photodiode preamps
Filters
A/D drivers
Level shifting
Buffering

CONNECTION DIAGRAMS

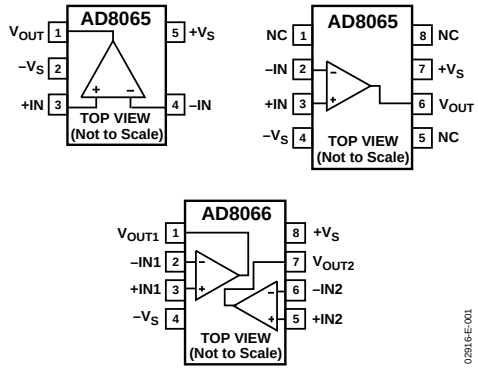

Figure 1.

GENERAL DESCRIPTION

The AD8065/AD8066[1] *FastFET*™ amplifiers are voltage feedback amplifiers with FET inputs offering high performance and ease of use. The AD8065 is a single amplifier, and the AD8066 is a dual amplifier. These amplifiers are developed in the Analog Devices, Inc. proprietary XFCB process and allow exceptionally low noise operation (7.0 nV/√Hz and 0.6 fA/√Hz) as well as very high input impedance.

With a wide supply voltage range from 5 V to 24 V, the ability to operate on single supplies, and a bandwidth of 145 MHz, the AD8065/AD8066 are designed to work in a variety of applications. For added versatility, the amplifiers also contain rail-to-rail outputs.

Despite the low cost, the amplifiers provide excellent overall performance. The differential gain and phase errors of 0.02% and 0.02°, respectively, along with 0.1 dB flatness out to 7 MHz, make these amplifiers ideal for video applications. Additionally, they offer a high slew rate of 180 V/µs, excellent distortion (SFDR of −88 dBc @ 1 MHz), extremely high common-mode rejection of −100 dB, and a low input offset voltage of 1.5 mV maximum under warmed up conditions. The AD8065/AD8066 operate using only a 6.4 mA/amplifier typical supply current and are capable of delivering up to 30 mA of load current.

[1] Protected by U. S. Patent No. 6,262,633.

The AD8065/AD8066 are high performance, high speed, FET input amplifiers available in small packages: SOIC-8, MSOP-8, and SOT-23-5. They are rated to work over the industrial temperature range of −40°C to +85°C.

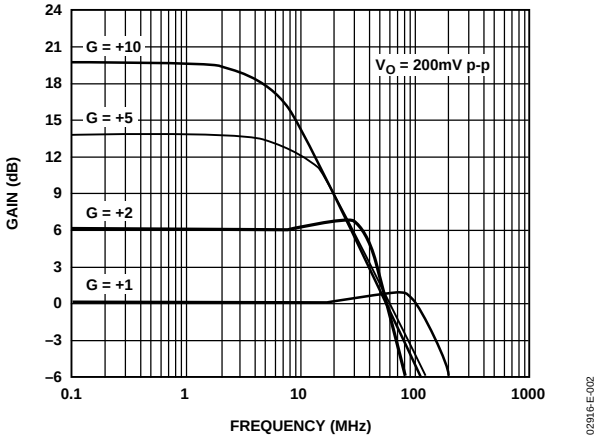

Figure 2. Small Signal Frequency Response

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SPECIFICATIONS

@ T_A = 25°C, V_S = ±5 V, R_L = 1 kΩ, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p (AD8065)	100	145		MHz
	G = +1, V_O = 0.2 V p-p (AD8066)	100	120		MHz
	G = +2, V_O = 0.2 V p-p		50		MHz
	G = +2, V_O = 2 V p-p		42		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p		7		MHz
Input Overdrive Recovery Time	G = +1, −5.5 V to +5.5 V		175		ns
Output Recovery Time	G = −1, −5.5 V to +5.5 V		170		ns
Slew Rate	G = +2, V_O = 4 V step	130	180		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V step		55		ns
	G = +2, V_O = 8 V step		205		ns
NOISE/HARMONIC PERFORMANCE					
SFDR	f_C = 1 MHz, G = +2, V_O = 2 V p-p		−88		dBc
	f_C = 5 MHz, G = +2, V_O = 2 V p-p		−67		dBc
	f_C = 1 MHz, G = +2, V_O = 8 V p-p		−73		dBc
Third-Order Intercept	f_C = 10 MHz, R_L = 100 Ω		24		dBm
Input Voltage Noise	f = 10 kHz		7		nV/√Hz
Input Current Noise	f = 10 kHz		0.6		fA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.02		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.02		Degrees
DC PERFORMANCE					
Input Offset Voltage	V_{CM} = 0 V, SOIC package		0.4	1.5	mV
Input Offset Voltage Drift			1	17	µV/°C
Input Bias Current	SOIC package		2	6	pA
	T_{MIN} to T_{MAX}		25		pA
Input Offset Current			1	10	pA
	T_{MIN} to T_{MAX}		1		pA
Open-Loop Gain	V_O = ±3 V, R_L = 1 kΩ	100	113		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1000 || 2.1		GΩ || pF
Differential Input Impedance			1000 || 4.5		GΩ || pF
Input Common-Mode Voltage Range					
FET Input Range		−5 to +1.7	−5.0 to +2.4		V
Common-Mode Rejection Ratio	V_{CM} = −1 V to +1 V	−85	−100		dB
	V_{CM} = −1 V to +1 V (SOT-23)	−82	−91		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ	−4.88 to +4.90	−4.94 to +4.95		V
	R_L = 150 Ω		−4.8 to +4.7		V
Output Current	V_O = 9 V p-p, SFDR ≥ −60 dBc, f = 500 kHz		35		mA
Short-Circuit Current			90		mA
Capacitive Load Drive	30% overshoot G = +1		20		pF
POWER SUPPLY					
Operating Range		5		24	V
Quiescent Current per Amplifier			6.4	7.2	mA
Power Supply Rejection Ratio	±PSRR	−85	−100		dB

@ T_A = 25°C, V_S = ±12 V, R_L = 1 kΩ, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p (AD8065)	100	145		MHz
	G = +1, V_O = 0.2 V p-p (AD8066)	100	115		MHz
	G = +2, V_O = 0.2 V p-p		50		MHz
	G = +2, V_O = 2 V p-p		40		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p		7		MHz
Input Overdrive Recovery	G = +1, −12.5 V to +12.5 V		175		ns
Output Overdrive Recovery	G = −1, −12.5 V to +12.5 V		170		ns
Slew Rate	G = +2, V_O = 4 V step	130	180		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V step		55		ns
	G = +2, V_O = 10 V step		250		ns
NOISE/HARMONIC PERFORMANCE					
SFDR	f_C = 1 MHz, G = +2, V_O = 2 V p-p		−100		dBc
	f_C = 5 MHz, G = +2, V_O = 2 V p-p		−67		dBc
	f_C = 1 MHz, G = +2, V_O = 10 V p-p		−85		dBc
Third-Order Intercept	f_C = 10 MHz, R_L = 100 Ω		24		dBm
Input Voltage Noise	f = 10 kHz		7		nV/√Hz
Input Current Noise	f = 10 kHz		1		fA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.04		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.03		Degrees
DC PERFORMANCE					
Input Offset Voltage	V_{CM} = 0 V, SOIC package		0.4	1.5	mV
Input Offset Voltage Drift			1	17	µV/°C
Input Bias Current	SOIC package		3	7	pA
	T_{MIN} to T_{MAX}		25		pA
Input Offset Current			2	10	pA
	T_{MIN} to T_{MAX}		2		pA
Open-Loop Gain	V_O = ±10 V, R_L = 1 kΩ	103	114		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1000 || 2.1		GΩ || pF
Differential Input Impedance			1000 || 4.5		GΩ || pF
Input Common-Mode Voltage Range					
FET Input Range		−12 to +8.5	−12.0 to +9.5		V
Common-Mode Rejection Ratio	V_{CM} = −1 V to +1 V	−85	−100		dB
	V_{CM} = −1 V to +1 V (SOT-23)	−82	−91		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ	−11.8 to +11.8	−11.9 to +11.9		V
	R_L = 350 Ω		−11.25 to +11.5		V
Output Current	V_O = 22 V p-p, SFDR ≥ −60 dBc, f = 500 kHz		30		mA
Short-Circuit Current			120		mA
Capacitive Load Drive	30% overshoot G = +1		25		pF
POWER SUPPLY					
Operating Range		5		24	V
Quiescent Current per Amplifier			6.6	7.4	mA
Power Supply Rejection Ratio	±PSRR	−84	−93		dB

@ T_A = 25°C, V_S = 5 V, R_L = 1 kΩ, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p (AD8065)	125	155		MHz
	G = +1, V_O = 0.2 V p-p (AD8066)	110	130		MHz
	G = +2, V_O = 0.2 V p-p		50		MHz
	G = +2, V_O = 2 V p-p		43		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p		6		MHz
Input Overdrive Recovery Time	G = +1, −0.5 V to +5.5 V		175		ns
Output Recovery Time	G = −1, −0.5 V to +5.5 V		170		ns
Slew Rate	G = +2, V_O = 2 V step	105	160		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V step		60		ns
NOISE/HARMONIC PERFORMANCE					
SFDR	f_C = 1 MHz, G = +2, V_O = 2 V p-p		−65		dBc
	f_C = 5 MHz, G = +2, V_O = 2 V p-p		−50		dBc
Third-Order Intercept	f_C = 10 MHz, R_L = 100 Ω		22		dBm
Input Voltage Noise	f = 10 kHz		7		nV/√Hz
Input Current Noise	f = 10 kHz		0.6		fA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.13		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.16		Degrees
DC PERFORMANCE					
Input Offset Voltage	V_{CM} = 1.0 V, SOIC package		0.4	1.5	mV
Input Offset Voltage Drift			1	17	µV/°C
Input Bias Current	SOIC package		1	5	pA
	T_{MIN} to T_{MAX}		25		pA
Input Offset Current			1	5	pA
	T_{MIN} to T_{MAX}		1		pA
Open-Loop Gain	V_O = 1 V to 4 V (AD8065)	100	113		dB
	V_O = 1 V to 4 V (AD8066)	90	103		dB
INPUT CHARACTERISTICS					
Common-Mode Input Impedance			1000 || 2.1		GΩ || pF
Differential Input Impedance			1000 || 4.5		GΩ || pF
Input Common-Mode Voltage Range					
FET Input Range		0 to 1.7	0 to 2.4		V
Common-Mode Rejection Ratio	V_{CM} = 0.5 V to 1.5 V	−74	−100		dB
	V_{CM} = 1 V to 2 V (SOT-23)	−78	−91		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ	0.1 to 4.85	0.03 to 4.95		V
	R_L = 150 Ω		0.07 to 4.83		V
Output Current	V_O = 4 V p-p, SFDR ≥ −60 dBc, f = 500 kHz		35		mA
Short-Circuit Current			75		mA
Capacitive Load Drive	30% overshoot G = +1		5		pF
POWER SUPPLY					
Operating Range		5		24	V
Quiescent Current per Amplifier		5.8	6.4	7.0	mA
Power Supply Rejection Ratio	±PSRR	−78	−100		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	26.4 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	V_{EE} − 0.5 V to V_{CC} + 0.5 V
Differential Input Voltage	1.8 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8065/AD8066 packages is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8065/AD8066. Exceeding a junction temperature of 175°C for an extended time can result in changes in the silicon devices, potentially causing failure.

The still air thermal properties of the package and PCB (θ_{JA}), ambient temperature (T_A), and total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature can be calculated by

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, then the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = Quiescent\ Power + \left(Total\ Drive\ Power - Load\ Power\right)$$

$$P_D = \left(V_S \times I_S\right) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to V_S-, as in single-supply operation, then the total drive power is $V_S \times I_{OUT}$.

If the rms signal levels are indeterminate, then consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = \left(V_S \times I_S\right) + \frac{\left(V_S/4\right)^2}{R_L}$$

In single-supply operation with R_L referenced to V_S-, worst case is $V_{OUT} = V_S/2$.

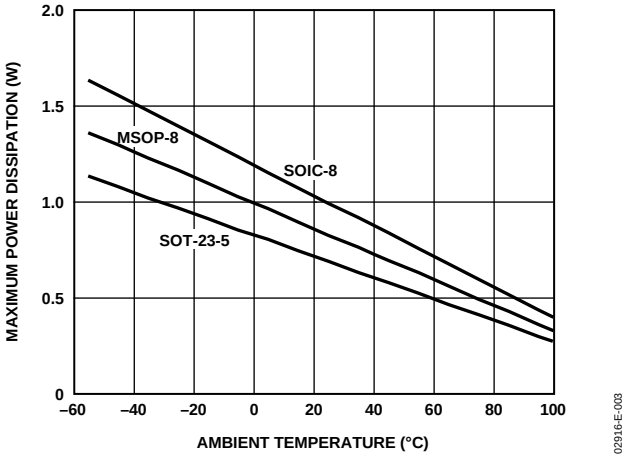


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduce the θ_{JA}. Care must be taken to minimize parasitic capacitances at the input leads of high speed op amps as discussed in the Layout, Grounding, and Bypassing Considerations section.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the SOIC (125°C/W), SOT-23 (180°C/W), and MSOP (150°C/W) packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

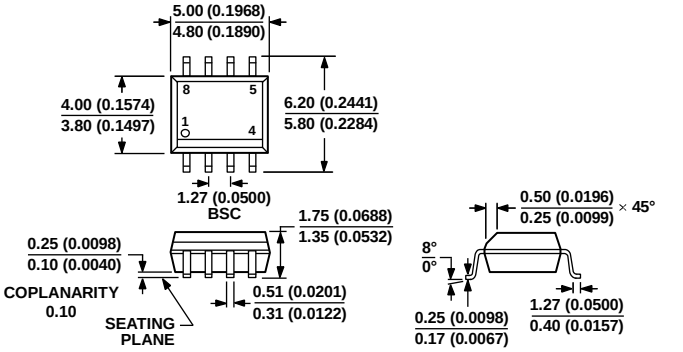
OUTPUT SHORT CIRCUIT

Shorting the output to ground or drawing excessive current for the AD8065/AD8066 will likely cause catastrophic failure.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS

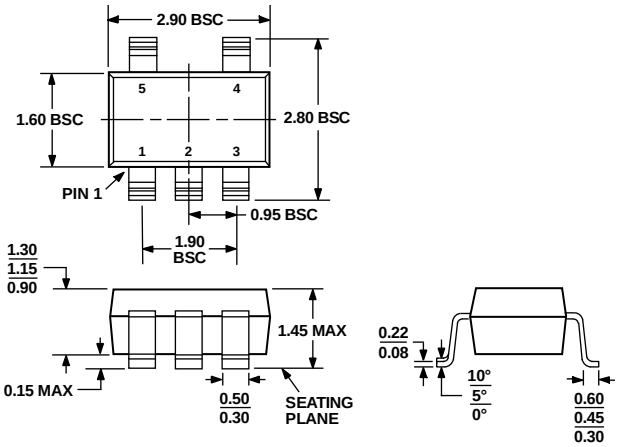


COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

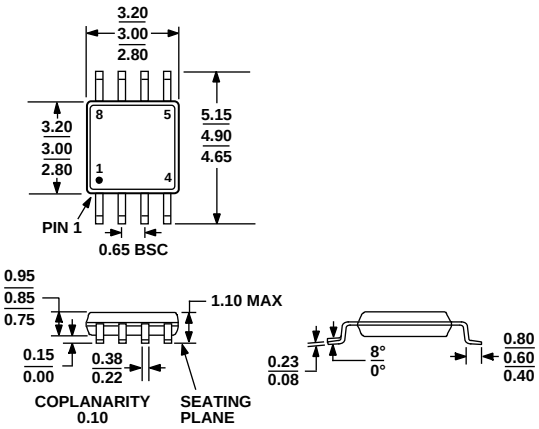
012407-A

Figure 62. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 63. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 64. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8065AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8065AR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8065AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8065ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8065ARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8065ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8065ART-R2	−40°C to +85°C	5-Lead SOT-23	RJ-5	HRA
AD8065ART-REEL	−40°C to +85°C	5-Lead SOT-23	RJ-5	HRA
AD8065ART-REEL7	−40°C to +85°C	5-Lead SOT-23	RJ-5	HRA
AD8065ARTZ-R2[1]	−40°C to +85°C	5-Lead SOT-23	RJ-5	HRA #
AD8065ARTZ-REEL[1]	−40°C to +85°C	5-Lead SOT-23	RJ-5	HRA #
AD8065ARTZ-REEL7[1]	−40°C to +85°C	5-Lead SOT-23	RJ-5	HRA #
AD8066AR	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8066AR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8066AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8066ARZ[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8066ARZ-RL[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8066ARZ-R7[1]	−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8066ARM	−40°C to +85°C	8-Lead MSOP	RM-8	H1B
AD8066ARM-REEL	−40°C to +85°C	8-Lead MSOP	RM-8	H1B
AD8066ARM-REEL7	−40°C to +85°C	8-Lead MSOP	RM-8	H1B
AD8066ARMZ[1]	−40°C to +85°C	8-Lead MSOP	RM-8	H7C
AD8066ARMZ-REEL7[1]	−40°C to +85°C	8-Lead MSOP	RM-8	H7C

[1] Z = RoHS Compliant Part, # denotes RoHS compliant product may be top or bottom marked.