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# AN-6604

## JFET Circuit Applications

### Introduction

JFETs continue to be a popular choice for many analog applications due to their low price, low noise, and input current and broad range of operation from DC to UHF.

In Figure 1, the 2N4393 JFET was selected because of its low  $I_{GSS}$  (<100 pA), very low  $I_{D(OFF)}$  (<100 pA) and low pinch off voltage. Leakages of this level put the burden of circuit performance on clean, solder-resin free PCBs, and low leakage circuit layout.

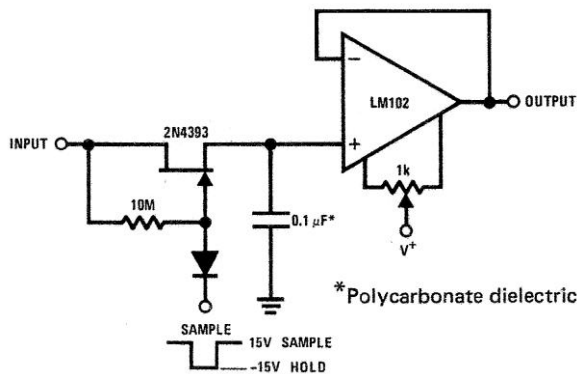


Figure 1. Sample and Hold with Offset Adjustment

Figure 2 is a simple reference circuit that provides a stable voltage reference almost totally free of supply voltage hash. Typical power supply rejection exceeds 100 dB.

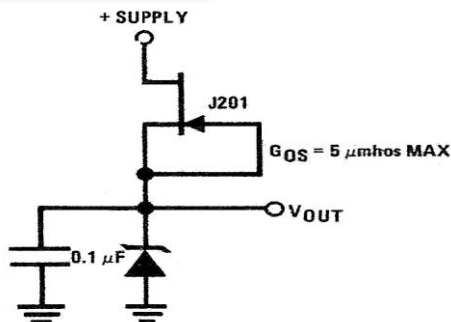


Figure 2. Low-Power Regulator Reference

Figure 3 utilizes the "u-amp" ("mu-amp") technique to achieve very high voltage gain. Using C1 in the circuit as a Miller integrator, or capacitance multiplier, allows this simple circuit to handle very long time constants.

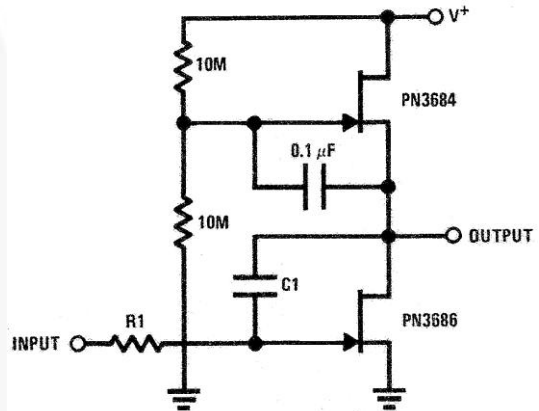


Figure 3. JFET AC Coupled Integrator

Figure 4 is configured to reduce input capacitance. The 2N5485 is operated as a source follower with bootstrapped gate bias resistor and drain.

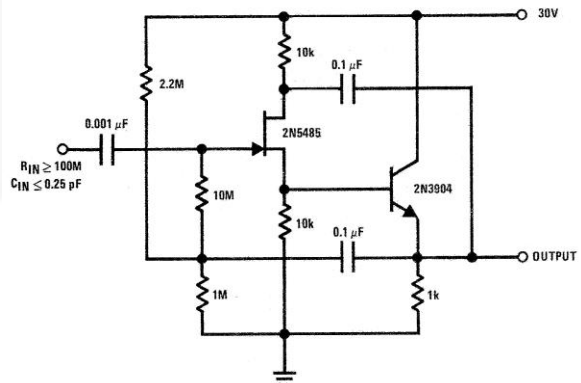


Figure 4. Ultra-High  $Z_{IN}$  Unity Gain Amplifier

Figure 5 is a JFET cascode video amplifier that has very low input loading and very low feedback. The 2N5485 is used because of its low capacitance and high  $Y_{fs}$ . Bandwidth of this amplifier is limited by  $R_L$  and load capacitance.

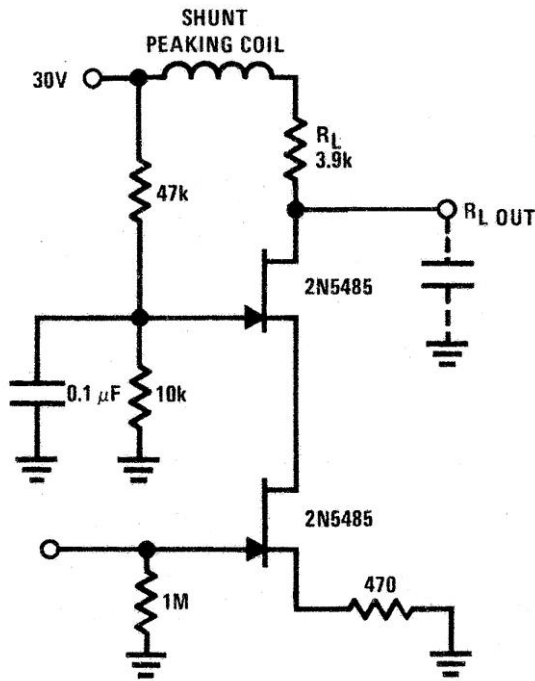


Figure 5. JFET Cascode Video Amplifier

Figure 6 uses a JFET to replace the vacuum tube in a typical VTVM while allowing battery operation. In addition, drift rates are far superior to vacuum tube circuits allowing a 0.5 V full-scale range which is impractical with most vacuum tubes. The low leakage, low noise NPD8303 is an ideal device for this application.

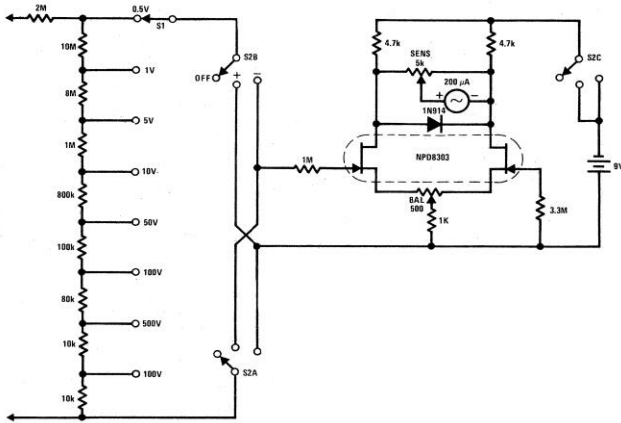


Figure 6. JFET Voltmeter

Figure 7 is a JFET Pierce crystal oscillator that can operate with a wide frequency range of crystals without circuit modification. Since the JFET gate does not load the crystal, good Q is maintained, thus insuring good frequency stability.

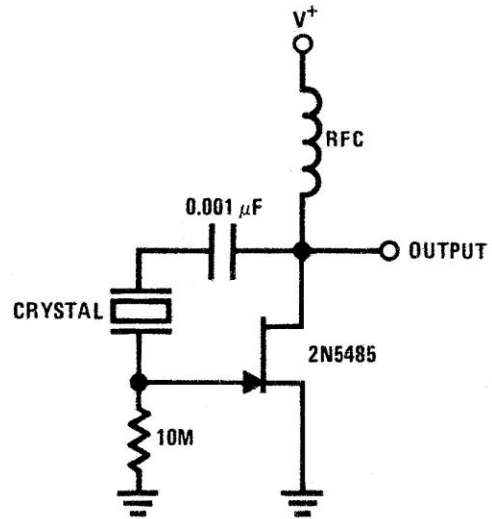


Figure 7. JFET Pierce Crystal Oscillator

In Figure 8, the 2N5458 JFET provides high input impedance and low noise characteristics to buffer an op amp-operated feedback type tone control circuit.

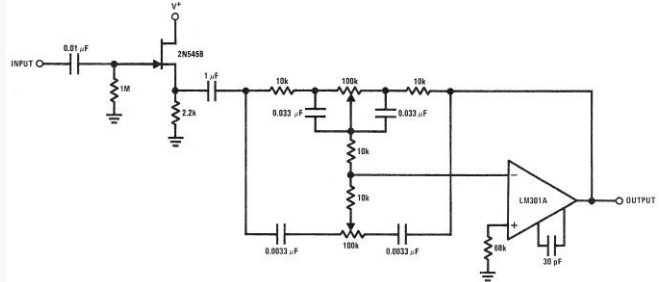


Figure 8. Hi-Fi Tone Control Circuit (Hi-Z Input)

In Figure 9, the 2N4416 JFET provides noise figures of less than 3 dB and power gain of greater than 20 dB. The JFET's outstanding low cross-modulation and low inter-modulation distortion provides an ideal characteristic for a Local Oscillator (L.O.) input stage. The output feeds into an LM171 used as a balanced mixer. This configuration greatly reduces L.O. radiation both into the antenna and into the IF strip and also reduces R F signal feed-through.

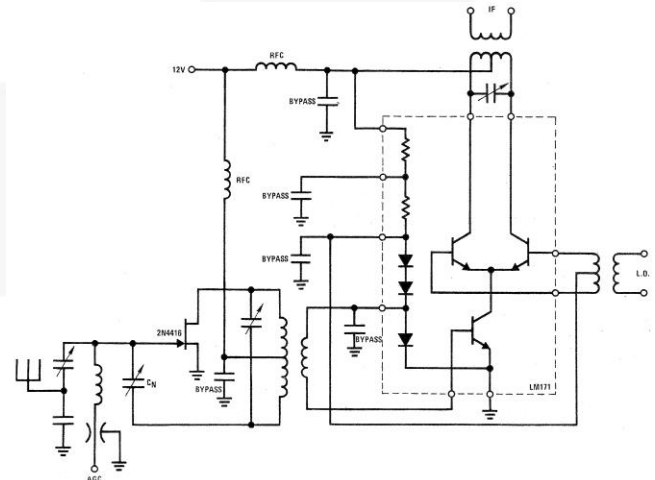


Figure 9. 100 MHz Converter

In Figure 10, the NPD5566 monolithic dual is used in a differential multiplexer application where  $R_{DS(ON)}$  should be closely matched. Since  $R_{DS(ON)}$  for the monolithic dual tracks at better than  $\pm 1\%$  over wide temperature ranges ( $-25^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ), this makes it an unusual but ideal choice for an accurate multiplexer. This close tracking greatly reduces errors due to common-mode signals.

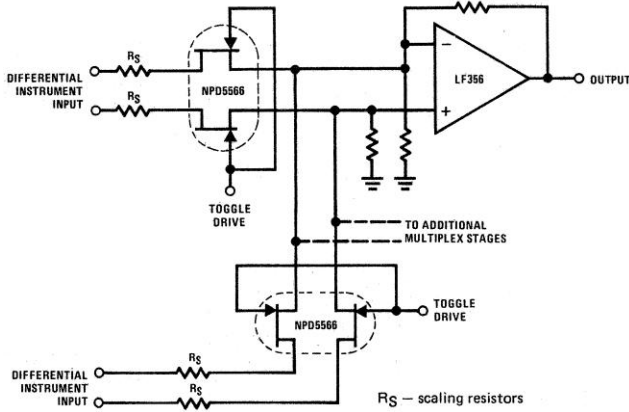


Figure 10. Differential Analog Switch

The preamplifier in Figure 11, provides proper loading to a reluctance phono cartridge. It provides approximately 35 dB of gain at 1 kHz (2.2 mV input for 100 mV output), it features S + N/N ratio of better than  $-70$  dB (referenced to 10 mV input at 1 kHz) and has a dynamic range of 84 dB (referenced to 1 kHz). The feedback provides for RIAA equalization.

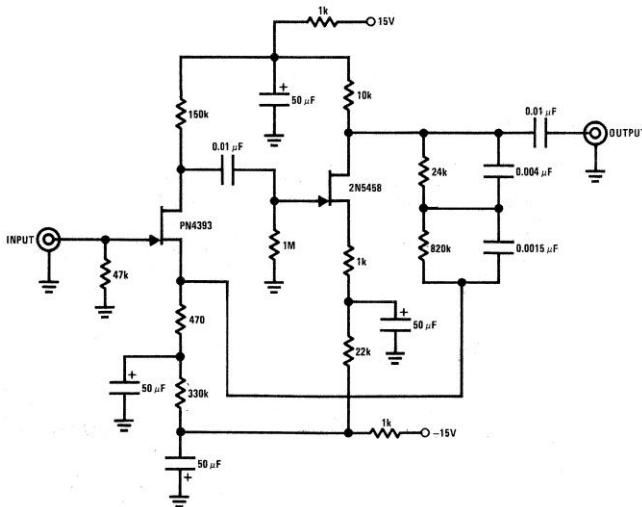


Figure 11. Magnetic Pickup Phono Preamplifier

In Figure 12, the 2N5457 acts as a voltage variable resistor with an  $R_{DS(ON)}$  of 800  $\Omega$  maximum. Since the differential voltage on the LM101 is in the low mV range, the 2N5457 JFET will have linear resistance over several decades of resistance providing an excellent electronic gain control.

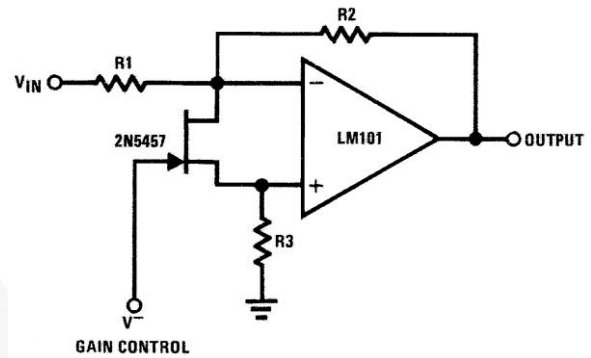


Figure 12. Voltage Controlled Variable Gain Amplifier

The PN4391, in Figure 13, provides a low  $R_{DS(ON)}$  (less than 30  $\Omega$ ). The tee attenuator provides for optimum dynamic linear range for attenuation and if complete turn-off is desired, attenuation of greater than 100 dB can be obtained at 10 MHz providing proper RF construction techniques are employed.

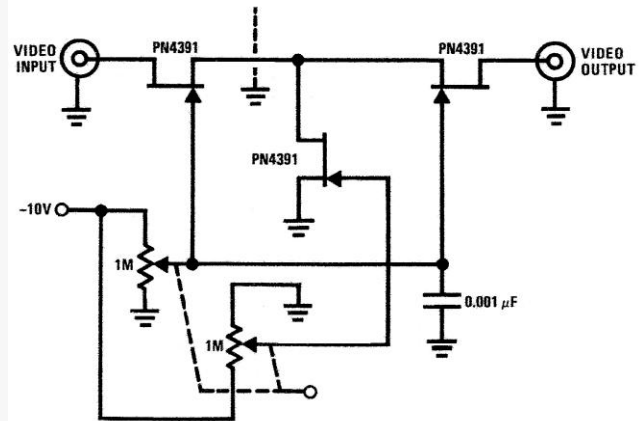


Figure 13. Variable Attenuator

In Figure 14, the 2N4391 provides a low ON resistance of 30  $\Omega$  and a high OFF impedance ( $< 0.2$  pF) when OFF. With proper layout and an "ideal" switch, the performance stated above can be readily achieved.

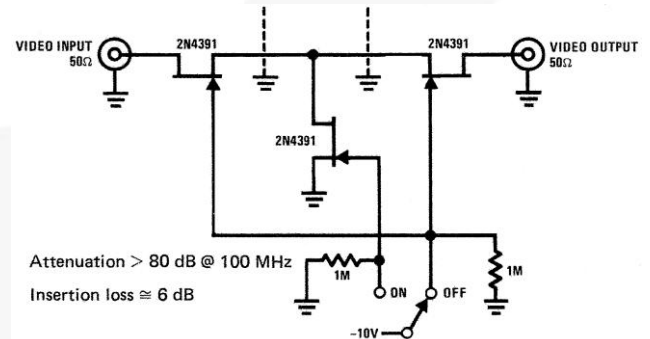
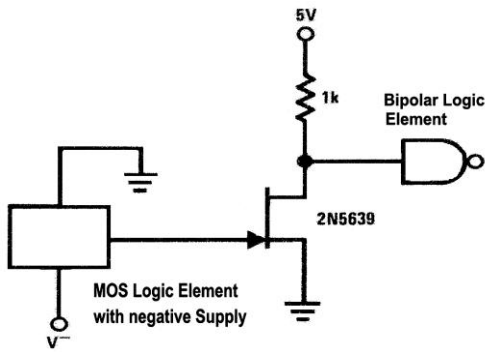


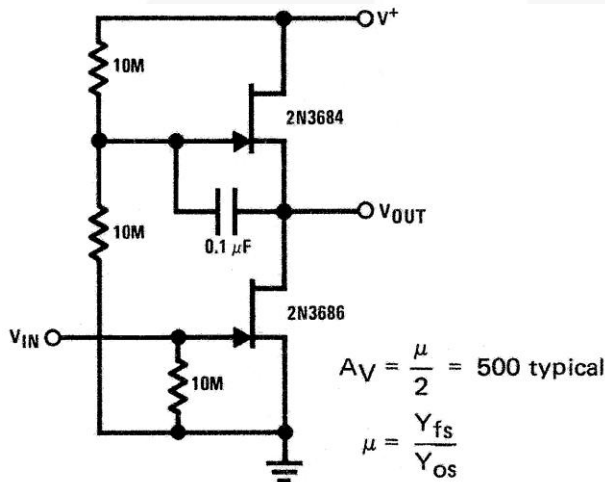
Figure 14. High Frequency Switch

Figure 15 is a simple circuit that provides for level shifting from any logic function (such as MOS) operating from minus to ground supply to any logic level (such as TTL) operating from a plus to ground supply. The 2N5639 provides a low  $R_{DS(ON)}$  and fast switching times.



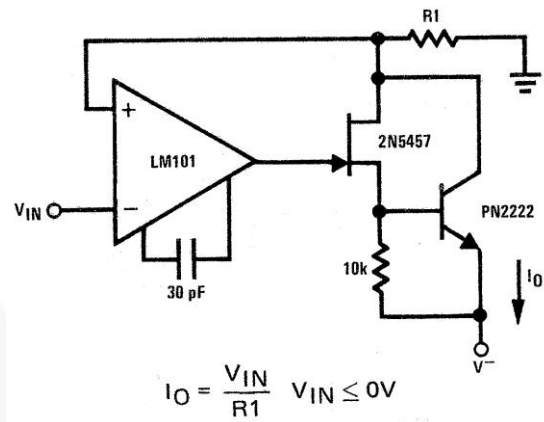
**Figure 15. Negative to Positive Supply Logic Level Shifter**

Figure 16, sometimes called the "JFET u-amp", this circuit provides a very low power, high gain amplifying function. Since  $\mu$  of a JFET increases as drain current decreases, the more gain you get. You do sacrifice input dynamic range with increasing gain, however.



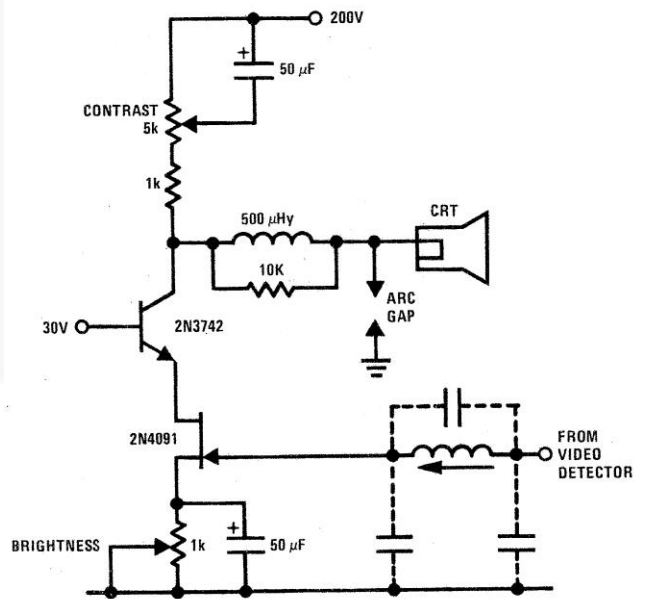
**Figure 16. Ultra-High Gain Amplifier**

In Figure 17, the 2N5457 and PN2222 bipolar serve as voltage isolation devices between the output and the current sensing resistor, R1. The LM101 provides a large amount of loop gain to assure that the circuit acts as a current source. For small values of current (<1 mA), the PN2222 and 10 k resistor may be eliminated with the output appearing at the source of the 2N5457.



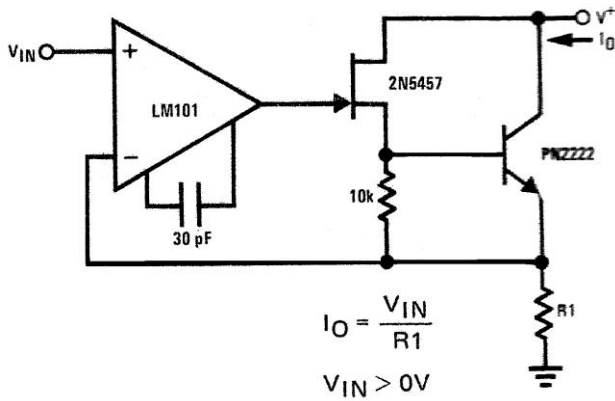
**Figure 17. Precision Current Source**

In Figure 18, the JFET-bipolar cascode circuit provides full video output for the CRT cathode drive. Gain is about 90. The cascode configuration eliminates Miller capacitance problems with the 2N4091 JFET, thus allowing direct drive from the video detector. An "m" derived filter using stray capacitance and a variable inductor prevents 4.5 MHz sound frequency from being amplified by the video amplifier.



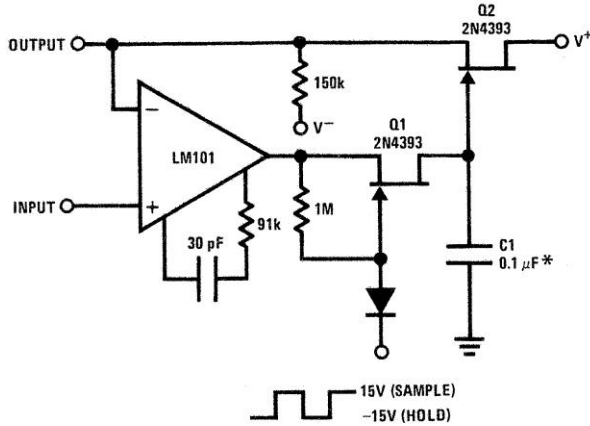
**Figure 18. JFET-Bipolar Cascode Circuit**

In Figure 19, the 2N5457 JFET and PN2222 bipolar have inherently high impedance. Using R1 as a current sensing resistor to provide feedback to the LM101 op amp provides a large amount of loop gain for negative feedback to enhance the true current sink nature of this circuit. For small current values, the 10 k resistor and PN2222 may be eliminated if the source of the JFET is connected to R1.



**Figure 19. Precision Current Sink**

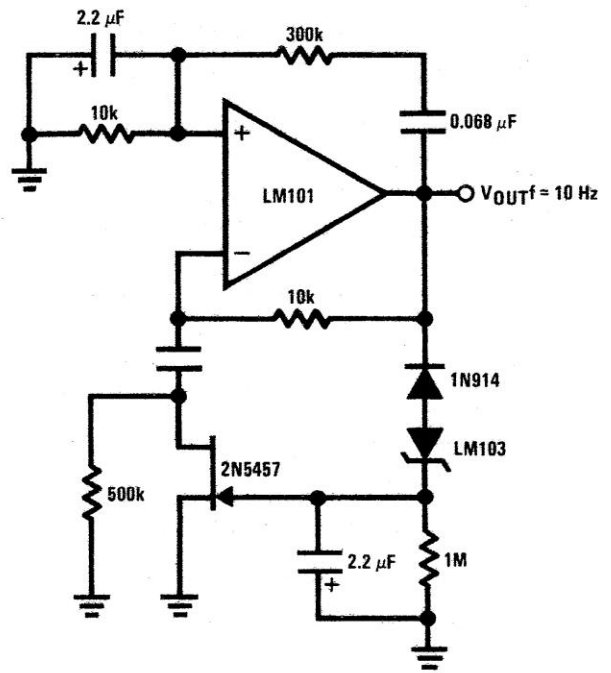
In Figure 20, the JFETs, Q1 and Q2, provide complete buffering to C1, the sample and hold capacitor. During sample, Q1 is turned ON and provides a path,  $R_{DS(ON)}$ , for charging C1. During hold, Q1 is turned OFF, thus leaving Q1  $I_{D(OFF)}$  (<100 pA) and Q2  $I_{GSS}$  (<100 pA) as the only discharge paths. Q2 serves a buffering function so feedback to the LM101 and output current are supplied from its source.



\*Polycarbonate dielectric capacitor

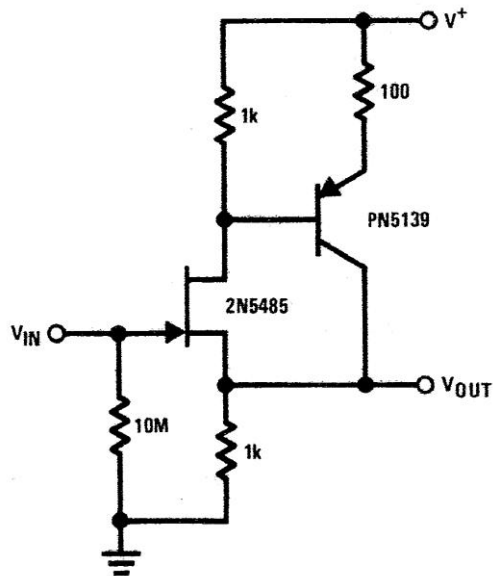
**Figure 20. Low Drift Sample and Hold**

Figure 21: The major problem in producing a low distortion, constant amplitude sine wave is getting the amplifier loop gain just right. By using the 2N5457 JFET as a voltage variable resistor in the amplifier feedback loop, this can be easily achieved. The LM103 Zener diode provides the voltage reference for the peak sine wave amplitude; this is rectified and fed to the gate of the 2N5457, thus varying its channel resistance and, hence, loop gain.



**Figure 21. Wein Bridge Sine-Wave Oscillator**

Figure 22: The 2N5485 features low input capacitance which makes this compound series-feedback buffer a wide-band unity gain amplifier.



**Figure 22. High Impedance Wideband Buffer**

Figure 23: The logic voltage is applied simultaneously to the sample and hold JFETs. By matching input impedance and feed-back resistance and capacitance, errors due to  $R_{DS(ON)}$  of the JFETs is minimized.

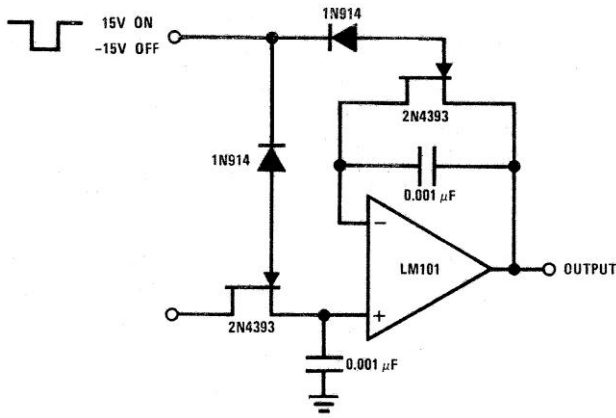


Figure 23. JFET Sample and Hold

Figure 24: This compound series-feedback circuit provides high input impedance and stable, wide-band gain for general purpose video amplifier applications.

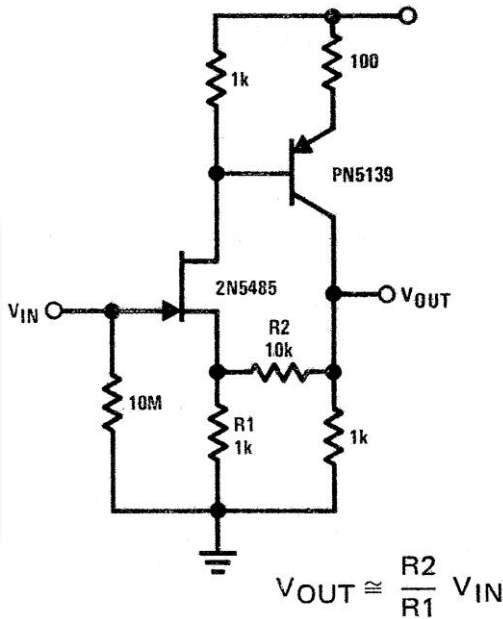


Figure 24. High Impedance Low Capacitance Amplifier

Figure 25: The Colpitts-Crystal oscillator is ideal for low frequency crystal operation. Excellent stability is assured because the 2N5484 JFET circuit loading does not vary with temperature.

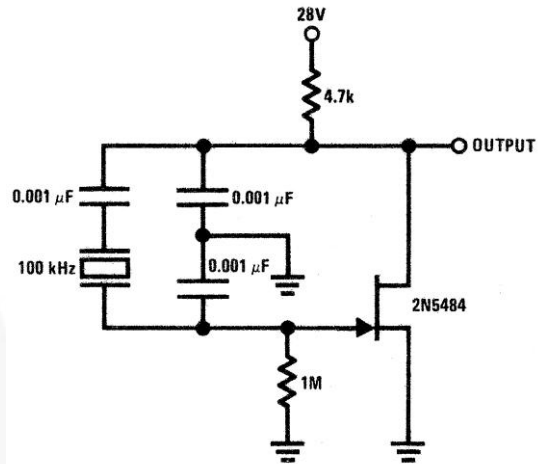


Figure 25. Stable Low Frequency Crystal Oscillator

Figure 26: This analog switch uses the 2N4860 JFET for its 25 Ω R<sub>ON</sub> and low leakage. The LM102 serves as a voltage buffer. This circuit can be adapted to a dual trace oscilloscope chopper. The DS7800 monolithic IC provides adequate switch drive controlled by DTL/TTL logic levels.

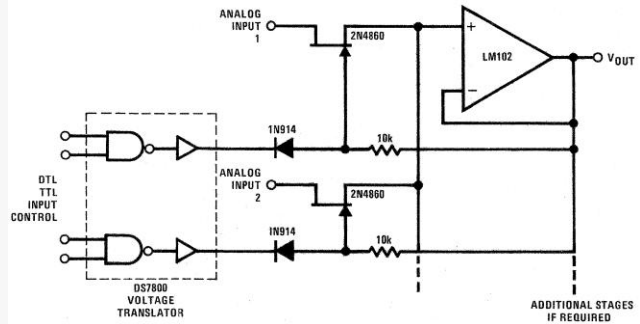


Figure 26. DTL-TTL Controlled Buffered Analog Switch

Figure 27: The 2N5485 JFET is capable of oscillating in a circuit where harmonic distortion is very low. The JFET local oscillator is excellent when low harmonic content is required for good mixer performance.

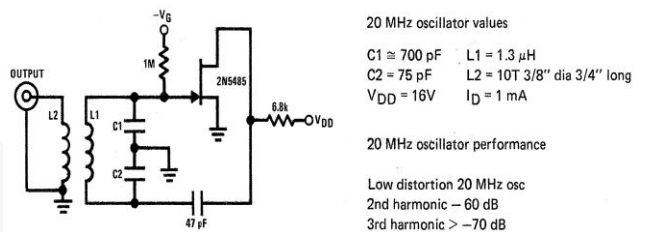


Figure 27. Low Distortion Oscillator

Figure 28: Each stage provides 0° to 180° phase shift. By ganging the 2 stages, 0° to 360° phase shift is achieved. The J202 JFETs are ideal since they do not load the phase shift networks.

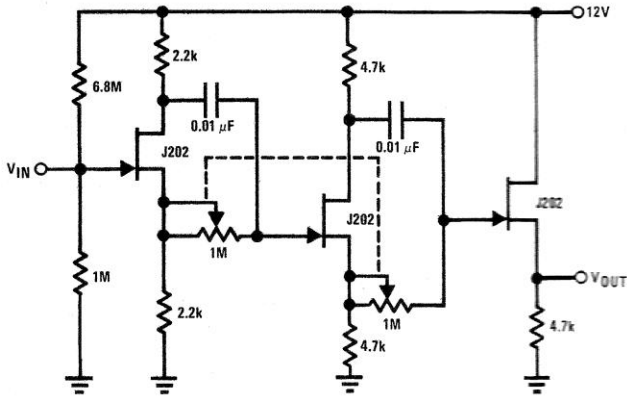


Figure 28. 0 to 360 degree Phase Shifter

In Figure 29, the 200 MHz JFET cascode circuit features low cross-modulation, large signal handling ability, no neutralization requirement, and AGC controlled by biasing the upper cascode JFET. The only special requirement of this circuit is that  $I_{DSS}$  of the upper unit must be greater than that of the lower unit.

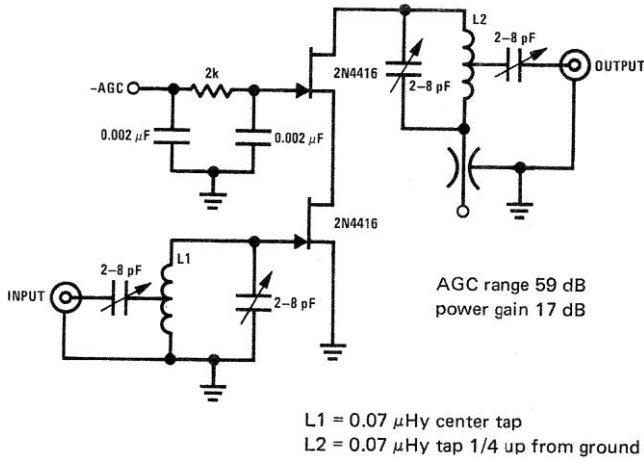


Figure 29. 200 MHz Cascode Amplifier

Figure 30: The NPD8301 monolithic-dual provides an ideal low offset, low drift buffer function for the LM101A op-amp. The excellent matching characteristics of the NPD8301 track well over its bias current range, thus improving common-mode rejection.

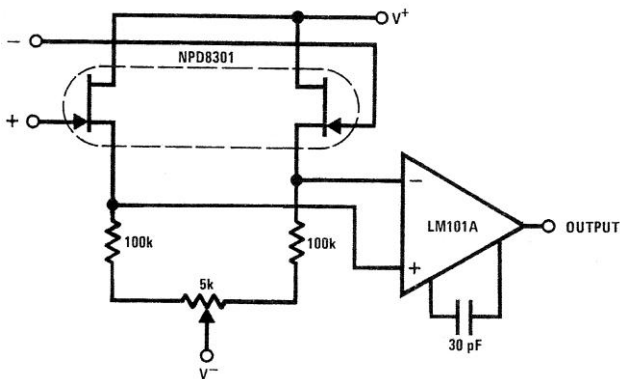


Figure 30. JFET Op-Amp

In Figure 31, the commutator circuit provides low impedance gate drive to the PN4091 analog switch for both ON and OFF drive conditions. This circuit also approaches the ideal gate drive conditions for high frequency signal handling by providing low AC impedance for OFF drive and high AC impedance for ON drive to the PN4091.

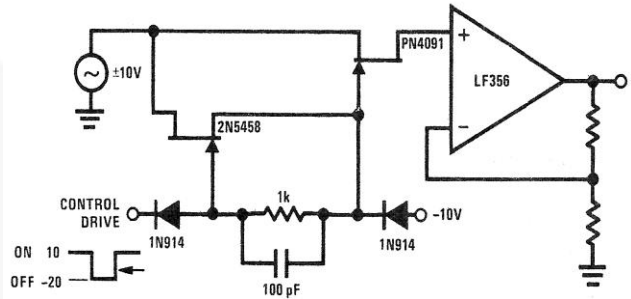


Figure 31. High Toggle Rate High Frequency Analog Switch

Figure 32: This 4-channel commutator uses the 2N4091 to achieve low channel ON resistance (<30 Ω) and low OFF current leakage. The DS7800 voltage translator is a monolithic device which provides from 10 V to -20 V gate drive to the JFETs while at the same time providing DTL/TTL logic compatibility.

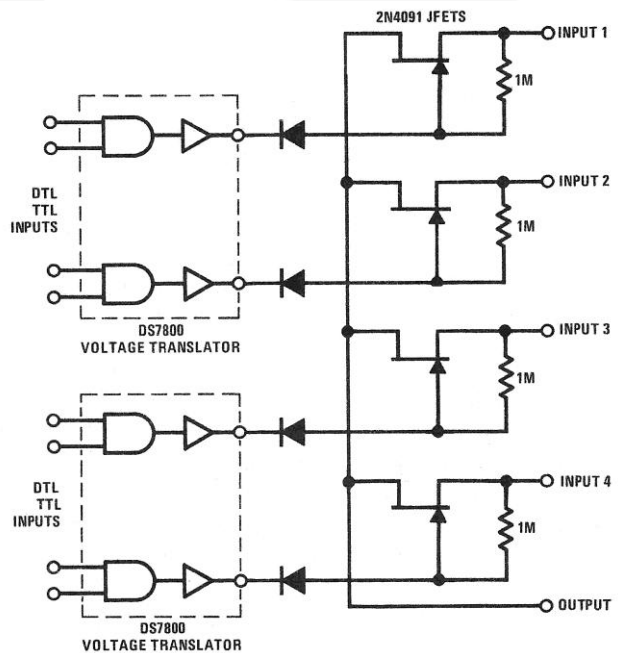
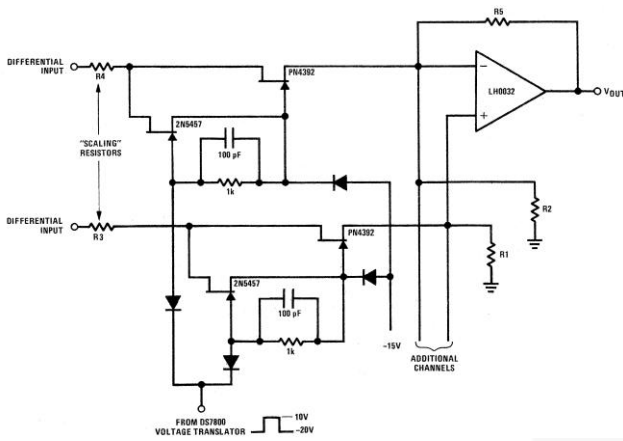


Figure 32. 4-Channel Commutator

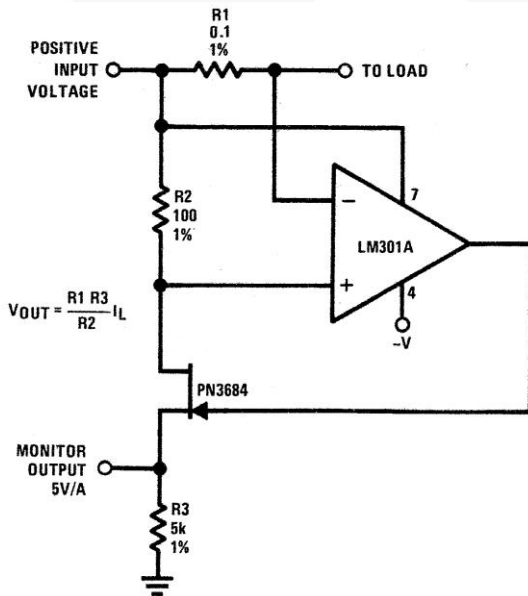
Figure 33: This design allows high frequency signal handling and high toggle rates simultaneously. Toggle rates up to 1 MHz and MHz signals are possible with this circuit.





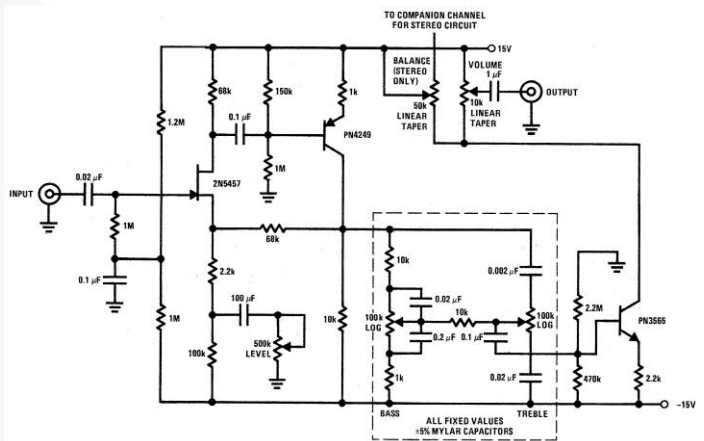
**Figure 33. Wide Band Differential Multiplexer**

Figure 34: R1 senses current flow of a power supply. The JFET is used as a buffer because  $I_d = I_s$ , therefore the output monitor voltage accurately reflects the power supply current flow.



**Figure 34. Current Monitor**

Figure 35: This preamp and tone control uses the JFET to its best advantage; as a low noise high input impedance device. All device parameters are non-critical, yet the circuit achieves harmonic distortion levels of less than 0.05% with an S/N ratio of over 85 dB. The tone controls allow 18 dB of cut and boost; the amplifier has a 1 V output for 100 mV input at maximum level.



**Figure 35. Low Cost High Level Preamp and Tone Control Circuit**

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