National Semiconductor

September 1995

LM6161/LM6261/LM6361
High Speed Operational Amplifier

General Description

The LM6161 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/μs and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

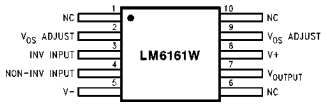
- High slew rate — 300 V/μs
- High unity gain freq — 50 MHz
- Low supply current — 5 mA
- Fast settling — 120 ns to 0.1%
- Low differential gain — <0.1%
- Low differential phase — 0.1°
- Wide supply range — 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply

Applications

- Video amplifier
- High-frequency filter
- Wide-bandwidth signal conditioning
- Radar
- Sonar

Connection Diagrams

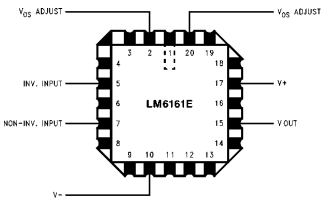
10-Lead Flatpak



TL/H/9057–13

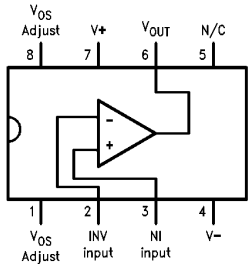
See NS Package Number W10A

20-Lead LCC



TL/H/9057–14

See NS Package Number E20A



TL/H/9057–5

See NS Package Number J08A, N08E or M08A

Temperature Range			Package	NSC Drawing
Military −55°C ≤ T_A ≤ +125°C	Industrial −25°C ≤ T_A ≤ +85°C	Commercial 0°C ≤ T_A ≤ +70°C		
	LM6261N	LM6361N	8-Pin Molded DIP	N08E
LM6161J/883 5962-8962101PA		LM6361J	8-Pin Ceramic DIP	J08A
	LM6261M	LM6361M	8-Pin Molded Surface Mt.	M08A
LM6161E/883 5962-89621012A			20-Lead LCC	E20A
LM6161W/883 5962-8962101HA			10-Pin Ceramic Flatpak	W10A

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Absolute Maximum Ratings (Note 12)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 8)	±8V
Common-Mode Voltage Range (Note 10)	$(V^+ - 0.7V)$ to $(V^- + 0.7V)$
Output Short Circuit to GND (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temp Range	−65°C to +150°C
Max Junction Temperature	150°C
ESD Tolerance (Notes 6 and 7)	±700V

Operating Ratings (Note 12)

Temperature Range (Note 2)	
LM6161	$-55°C \le T_J \le +125°C$
LM6261	$-25°C \le T_J \le +85°C$
LM6361	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, $V_{CM} = 0$, $R_L \ge 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_J = T_{MIN}$ to T_{MAX}; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6161	LM6261	LM6361	Units
				Limit (Notes 3, 11)	Limit (Note 3)	Limit (Note 3)	
V_{OS}	Input Offset Voltage		5	7 **10**	7 **9**	20 **22**	mV Max
V_{OS} Drift	Input Offset Voltage Average Drift		10				µV/°C
I_b	Input Bias Current		2	3 **6**	3 **5**	5 **6**	µA Max
I_{OS}	Input Offset Current		150	350 **800**	350 **600**	1500 **1900**	nA Max
I_{OS} Drift	Input Offset Current Average Drift		0.4				nA/°C
R_{IN}	Input Resistance	Differential	325				kΩ
C_{IN}	Input Capacitance	$A_V = +1$ @ 10 MHz	1.5				pF
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 2\ k\Omega$ (Note 9)	750	550 **300**	550 **400**	400 **350**	V/V Min
		$R_L = 10\ k\Omega$ (Note 9)	2900				V/V
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	+13.9 **+13.8**	+13.8 **+13.7**	Volts Min
			−13.2	−12.9 **−12.7**	−12.9 **−12.7**	−12.8 **−12.7**	Volts Min
		Supply = +5V (Note 4)	4.0	3.9 **3.8**	3.9 **3.8**	3.8 **3.7**	Volts Min
			1.8	2.0 **2.2**	2.0 **2.2**	2.1 **2.2**	Volts Max
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	94	80 **74**	80 **76**	72 **70**	dB Min
PSRR	Power Supply Rejection Ratio	$\pm 10V \le V^{\pm} \le \pm 16V$	90	80 **74**	80 **76**	72 **70**	dB Min
V_O	Output Voltage Swing	Supply = ±15V and $R_L = 2\ k\Omega$	+14.2	+13.5 **+13.3**	+13.5 **+13.3**	+13.4 **+13.3**	Volts Min
			−13.4	−13.0 **−12.7**	−13.0 **−12.8**	−12.9 **−12.8**	Volts Min

DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_J = T_{MIN}$ to T_{MAX}; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typ	LM6161 Limit (Notes 3, 11)	LM6261 Limit (Note 3)	LM6361 Limit (Note 3)	Units
V_O (Continued)	Output Voltage Swing (Continued)	Supply = +5V and R_L = 2 kΩ (Note 4)	4.2	3.5 **3.3**	3.5 **3.3**	3.4 **3.3**	Volts Min
			1.3	1.7 **2.0**	1.7 **1.9**	1.8 **1.9**	Volts Max
	Output Short Circuit Current	Source	65	30 **20**	30 **25**	30 **25**	mA Min
		Sink	65	30 **20**	30 **25**	30 **25**	mA Min
I_S	Supply Current		5.0	6.5 **6.8**	6.5 **6.7**	6.8 **6.9**	mA Max

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_J = T_{MIN}$ to T_{MAX}; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typ	LM6161 Limit (Notes 3, 11)	LM6261 Limit (Note 3)	LM6361 Limit (Note 3)	Units
GBW	Gain-Bandwidth Product	@ f = 20 MHz	50	40 **30**	40 **35**	35 **32**	MHz Min
		Supply = ±5V	35				MHz
SR	Slew Rate	A_V = +1 (Note 8)	300	200 **180**	200 **180**	200 **180**	V/μs Min
		Supply = ±5V (Note 8)	200				V/μs
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5				MHz
t_S	Settling Time	10V Step to 0.1% A_V = −1, R_L = 2 kΩ	120				ns
φm	Phase Margin		45				Deg
A_D	Differential Gain	NTSC, A_V = +4	<0.1				%
φD	Differential Phase	NTSC, A_V = +4	0.1				Deg
e_{np-p}	Input Noise Voltage	f = 10 kHz	15				nV/√Hz
i_{np-p}	Input Noise Current	f = 10 kHz	1.5				pA/√Hz

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/W, the molded plastic SO (M) package is 155°C/W, and the cerdip (J) package is 125°C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Limits are guaranteed by testing or correlation.

Note 4: For single supply operation, the following conditions apply: V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 & Pin 8 (Vos Adjust) are each connected to Pin 4 (V^-) to realize maximum output swing. This connection will degrade V_{OS}, V_{OS} Drift, and Input Voltage Noise.

Note 5: $C_L \leq 5$ pF.

Note 6: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially Vos, Ios, and Noise).

Note 7: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 8: V_{IN} = 8V step. For supply = ±5V, V_{IN} = 5V step.

Note 9: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

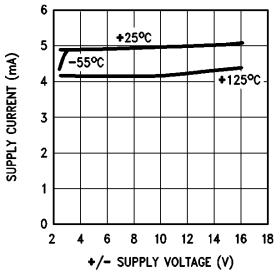
Note 10: The voltage between V^+ and either input pin must not exceed 36V.

Note 11: A military RETS electrical test specification is available on request. At the time of printing, the RETS6161X specs complied with all **Boldface** limits in this column.

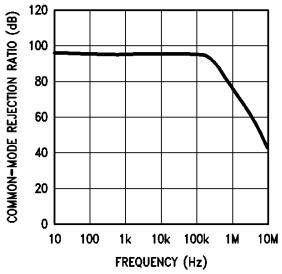
Note 12: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Typical Performance Characteristics (R_L = 10 kΩ, T_A = 25°C unless otherwise specified)

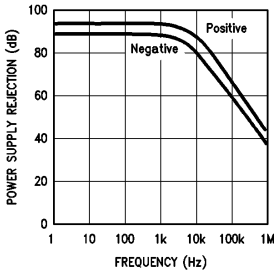
Supply Current vs Supply Voltage



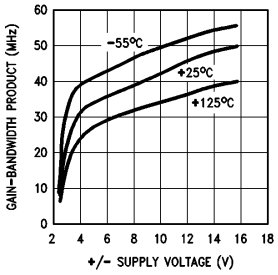
Common-Mode Rejection Ratio



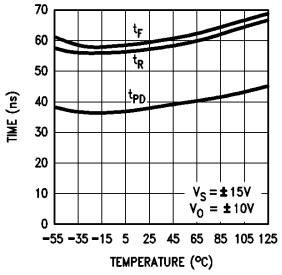
Power Supply Rejection Ratio



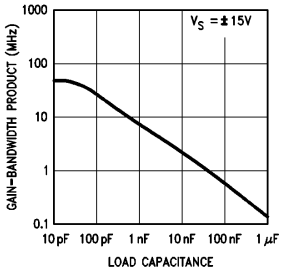
Gain-Bandwidth Product



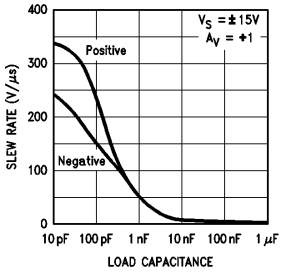
Propagation Delay Rise and Fall Times



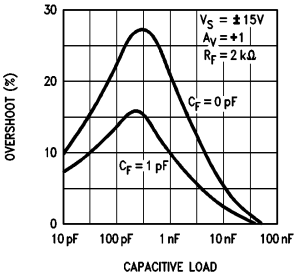
Gain-Bandwidth Product vs Load Capacitance



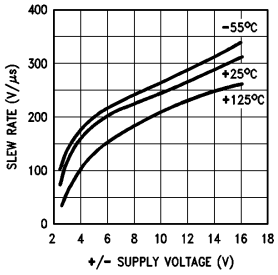
Slew Rate vs Load Capacitance



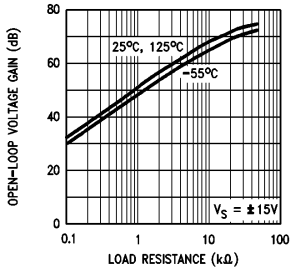
Overshoot vs Capacitive Load



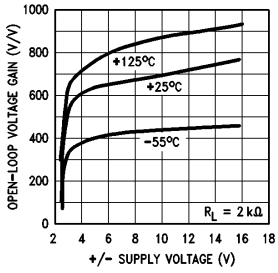
Slew Rate



Voltage Gain vs Load Resistance



Gain vs Supply Voltage



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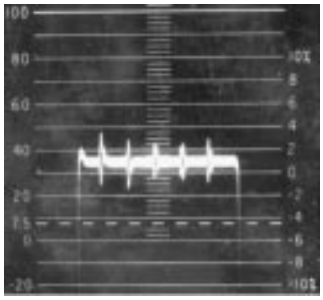
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

Differential Gain (Note)



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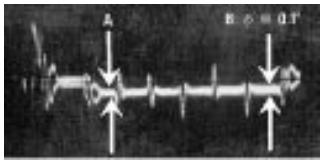
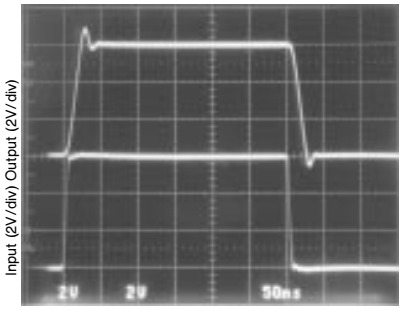
Differential Phase (Note)



TL/H/9057–8

Note: Differential gain and differential phase measured for four series LM6361 op amps configured as unity-gain followers, in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

Step Response; Av = +1



(50 ns/div)

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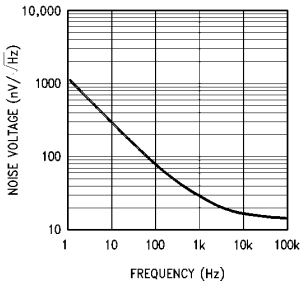
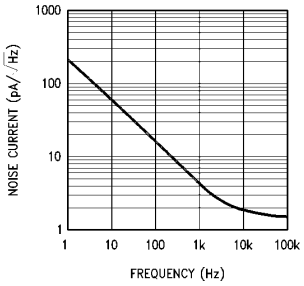
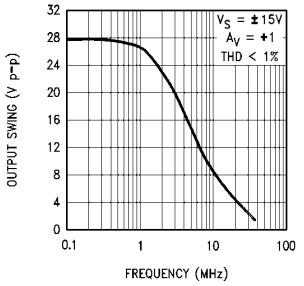
Input Noise Voltage



Input Noise Current



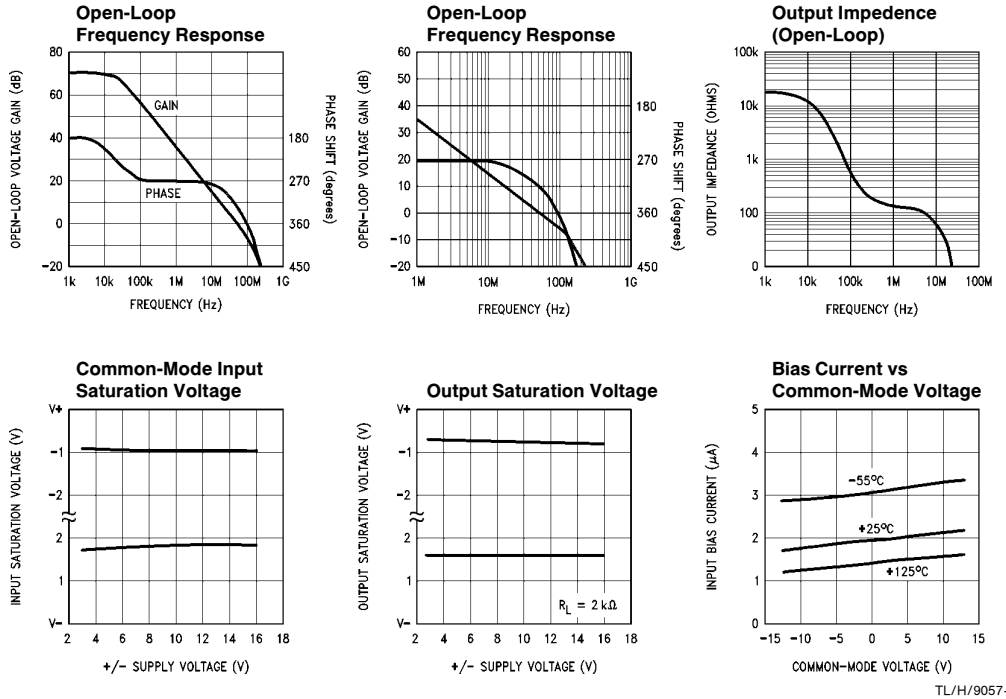
Power Bandwidth



TL/H/9057–9

Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)



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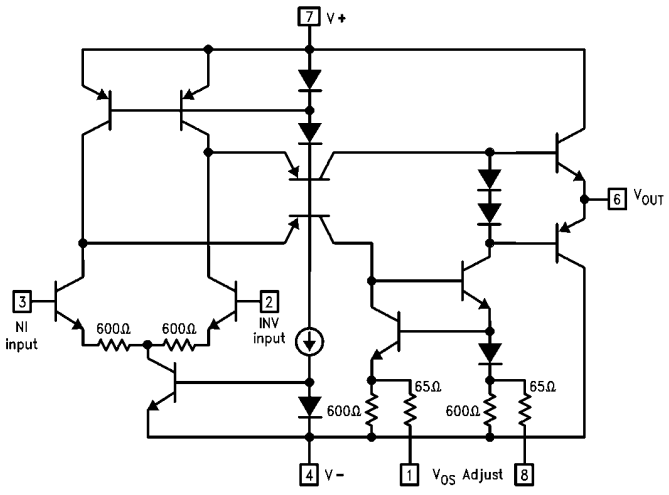
Simplified Schematic



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Applications Tips

The LM6361 has been compensated for unity-gain operation. Since this compensation involved adding emitter-degeneration resistors to the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains; thus, for gains between 5 and 25, the less-compensated LM6364 should be used, and the uncompensated LM6365 is appropriate for gains of 25 or more. The LM6361, LM6364, and LM6365 have the same high slew rate, regardless of their compensation.

The LM6361 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (especially in low-gain circuits). The LM6361's compensation is effectively increased with load capacitance, reducing its bandwidth and increasing its stability.

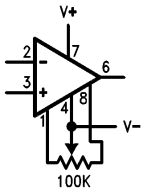
Power supply bypassing is not as critical for the LM6361 as it is for other op amps in its speed class. Bypassing will, however, improve the stability and transient response and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF of tantalum may provide extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling across adjacent nodes and can cause gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

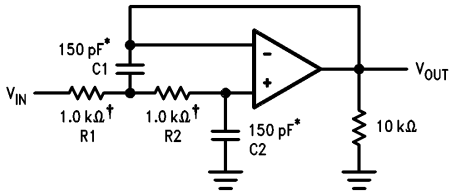
Typical Applications

Offset Voltage Adjustment



TL/H/9057–4

1 MHz Low-Pass Filter



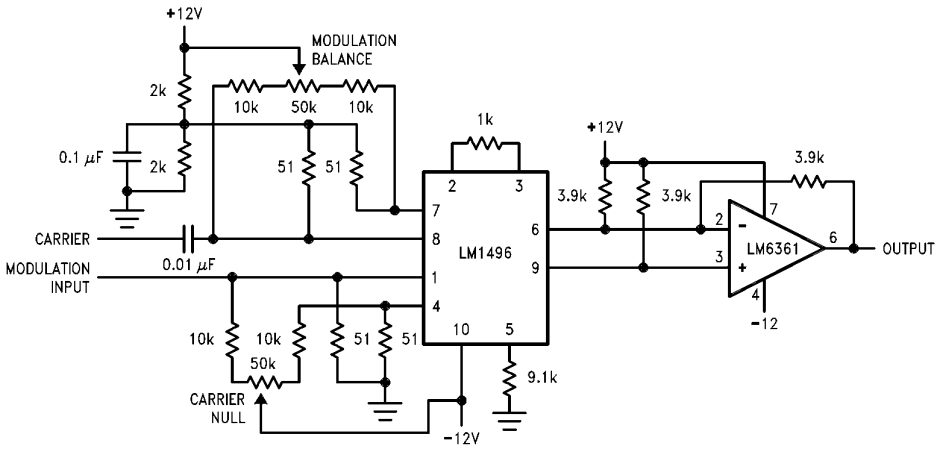
TL/H/9057–10

†1% tolerance

*Matching determines filter precision

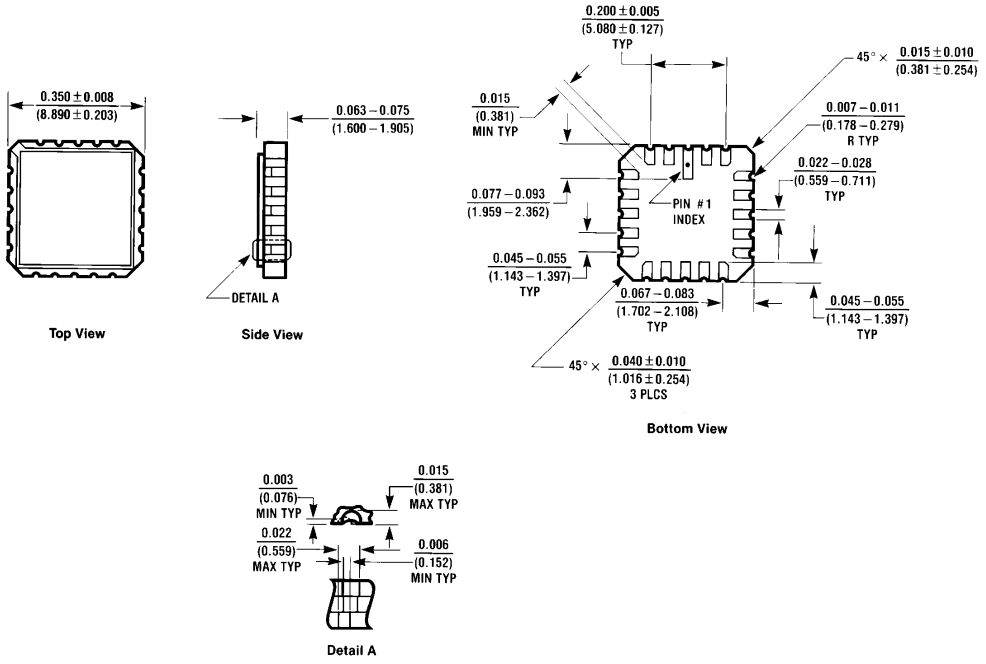
$f_c = (2\pi\sqrt{(R1\ R2\ C1\ C2)})^{-1}$

Modulator with Differential-to-Single-Ended Converter

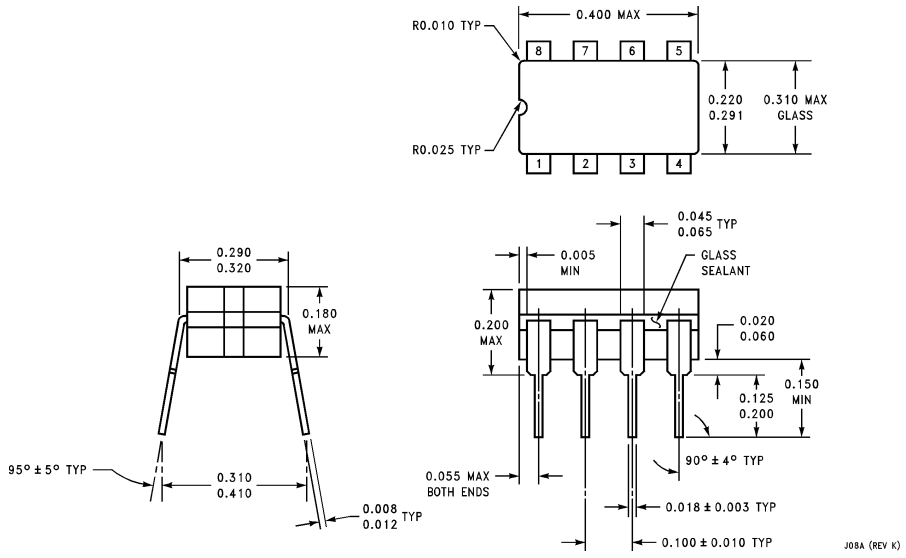


TL/H/9057–11

Physical Dimensions inches (millimeters)

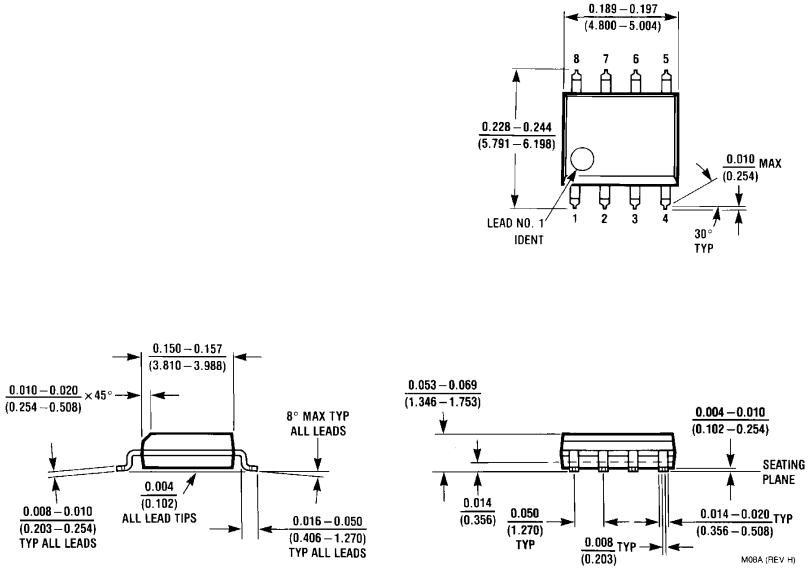


20-Lead Small Outline Package (E)
Order Number LM6161E/883
NS Package Number E20A

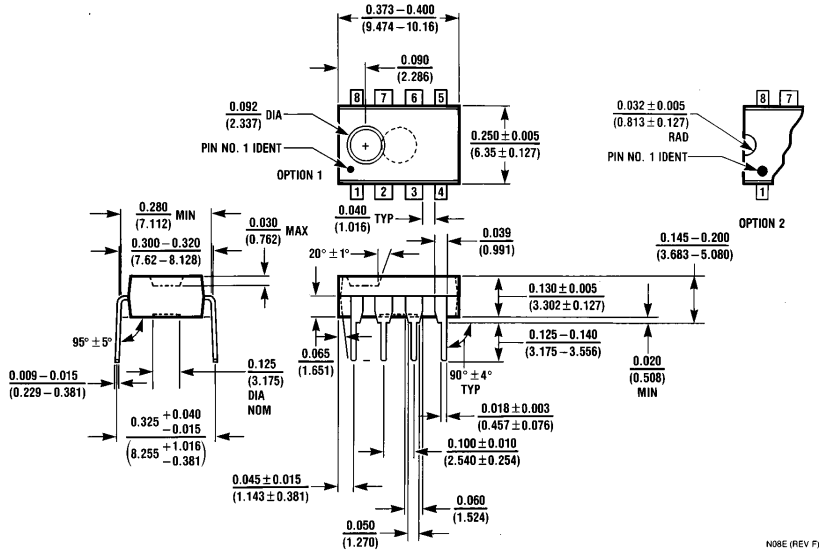


Ceramic Dual-In-Line Package (J)
Order Number LM6161J/883
NS Package Number J08A

Physical Dimensions inches (millimeters) (Continued)

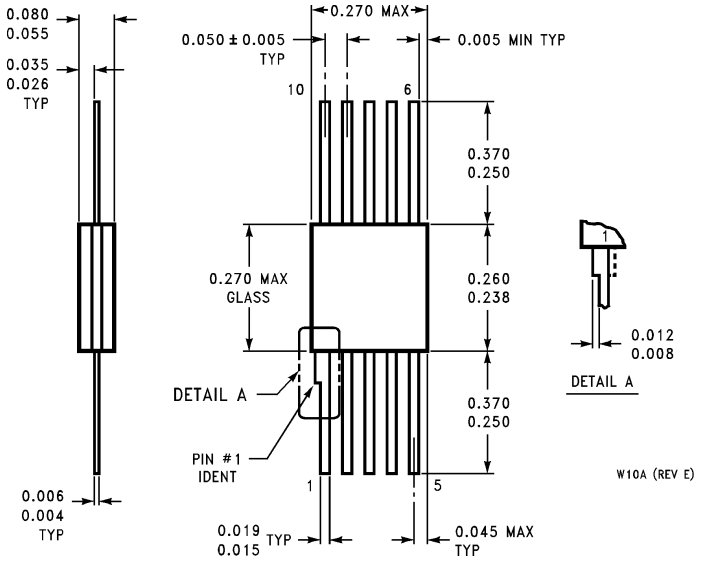


Molded Package SO (M)
Order Number LM6261M or LM6361M
NS Package Number M08A



Molded Dual-In-Line Package (N)
Order Number LM6261N or LM6361N
NS Package Number N08E

Physical Dimensions inches (millimeters) (Continued)



10-Pin Ceramic Flatpak
Order Number LM6161W/883
NS Package Number W10A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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