Application Report
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Application Design Guidelines for LM324/LM358 Devices

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Including LM124, LM224, LM2902, LM158, LM258, LM2904, LM321, TS321

ABSTRACT

The LM324 and LM358 family of op amps are popular and long-lived general purpose amplifiers due to their flexibility, availability, and cost-effectiveness. It is important to understand how these op amps are different than most other op amps before using them in your design. The information in this application guide will help promote first time design successes.

Contents

List of Figures

List of Tables

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1 Devices Covered in Application Note

1.1 Common Schematic

This application note covers all op amps that are based on the schematic in Figure 1, which contains a unique output stage that was revolutionary when released. Unlike other op amps of the time, it supports a near ground output voltage useful for single supply designs. The ~50-µA Current Regulator can pull the output close to ground because the other transistor emitters do not have a strong opposing current flow, unlike other op amps of this time period.

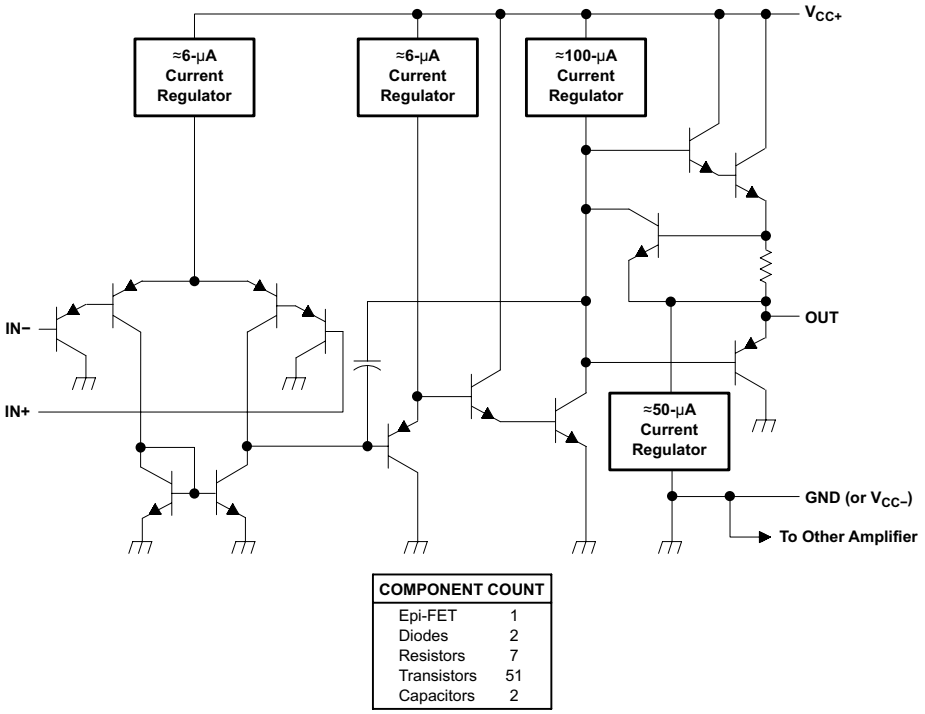

Figure 1. Device Schematic from Data Sheet

1.2 Base Part Numbers

The temperature range and channel count are used to create the base part number. The “-N” in a part name denotes devices acquired from National Semiconductor that matched an existing Texas Instruments (TI) base part number. There are no orderable part number duplicates because National Semiconductor and TI used different package suffixes.

Table 1. Base Part Number, Channel Count, and Temperature Range

Temperature Range	Single		Dual			Quad	
–55°C to 125°C	—	—	**LM158**		**LM158-N**	**LM124**	**LM124-N**
–40°C to 125°C	**TS321**	—	**LM2904**	**LM2904B**	LM158-N	**LM2902**	LM124-N
–40°C to 85°C	TS321	**LM321**	LM2904	**LM358B**	**LM2904-N**	LM2902	**LM2902-N**
–25°C to 85°C	TS321	LM321	**LM258**		**LM258-N**	**LM224**	**LM224-N**
0°C to 70°C	TS321	LM321	**LM358**		**LM358-N**	**LM324**	**LM324-N**
Automotive Q1	**TS321-Q1**		**LM2904-Q1**			**LM2902-Q1**	

Part numbers in bold have operating temperature regions that match the given temperature range exactly. Part numbers that are not in bold can operate within and beyond the given temperature range. Please note that, counterintuitively, LM2904 is a dual op amp, whereas LM2902 is a quad op amp.

1.3 Input Voltage Offset Grades

There are also grade options for V_{IO} (also known as V_{os}) tolerance. An “A” in the part number suffix will have better V_{IO} specifications compared to the same part number without an “A”.

Table 2. Maximum Input Offset Error at 25°C for Each Base Part Number with V_{IO} Grade Options

Single		Dual		Quad	
Part Number	V_{IO} Max 25°C	Part Number	V_{IO} Max 25°C	Part Number	V_{IO} Max 25°C
TS321	4 mV	LM158A	2 mV	LM124A	2 mV
TS321-Q1	4 mV	LM158A-N	2 mV	LM124A-N	2 mV
LM321	7 mV	LM2904AV	2 mV	LM2902KAV	2 mV
—	—	LM2904AV-Q1	2 mV	LM2902KAV-Q1	2 mV
		LM258A	3 mV	LM224A	3 mV
		LM358A	3 mV	LM324A	3 mV
		LM358A-N	3 mV	LM324A-N	3 mV
		LM358B	3 mV	LM124	5 mV
		LM2904B	3 mV	LM124-N	5 mV
		LM158	5 mV	LM224	5 mV
		LM158-N	5 mV	LM224-N	5 mV
		LM258	5 mV	LM2902K	7 mV
		LM258-N	5 mV	LM2902	7 mV
		LM2904	7 mV	LM2902-Q1	7 mV
		LM2904-N	7 mV	LM324	7 mV
		LM2904-Q1	7 mV	LM324-N	7 mV
		LM358	7 mV	—	—
		LM358-N	7 mV		

1.4 Maximum Supply Voltage

The default maximum supply voltage is 30 V; however LM290X devices have a 26-V maximum supply rating. The exceptions are LM2902 and LM2904 devices having a “V” in the suffix, which denotes maximum voltage up to 32 V. Two examples are LM2902KAVQDR and LM2904AVQDR. All devices with a “B” in the suffix have a maximum supply voltage rated at 36 V; examples are LM358BDR, LM2904BADR.

1.5 High Reliability Options

There are many high reliability options for dual and quad op amps.

Dual op amp product list: LM158QML-SP, LM158QML, LM158, LM158A, LM158-N, LM258A-EP, LM258-N, LM2904-EP

Quad op amp product list: LM124AQML-SP, LM124-N, LM124A, LM124AQML, LM124M, LM224-N, LM324-N-MIL, LM2902-EP

The qualifications and ratings of these devices are not covered in this application note.

1.6 HBM ESD Grade

For ESD purposes, the “K” and “B” suffixes in part names have the same meaning. A “K” or "B" in the suffix of a quad op amp denotes an HBM ESD rating of 2 kV. For example, LM324K, LM324KA, LM2902K, LM2902KA, LM2902KAV, LM2904B and LM358B all have a 2-kV HBM rating.

When greater ESD protection is desired, designers should incorporate system-level ESD solutions.

1.7 LM358B, LM358BA, LM2904B, LM2904BA

The “B” suffix is used to denote new device variant releases based on an advanced wafer process that provides many device improvements. Maximum supply voltage is increased to 36 V; EMI filters are added to inputs; input offset voltage is reduced (3 mV or 1.8 mV for parts with an ‘A’ in their suffix); tested low V_{OL} sink drive current is increased (from 12 µA to 50 µA) to support lower resistance feedback networks and more load current; 2-kV HBM ESD is standard. Most data sheet specifications use a setup of a load terminated to mid-supply to match modern data sheet test conditions.

2 Input Stage Considerations

2.1 Input Stage Schematic

The input stage in Figure 2 contains additional current source lines (shown boxed in red) not drawn in the simplified schematic found in the data sheets. All PNP emitters in the Darlington input stage have current source connections. These connections ensure a consistent input bias current that does not vary with the differential input voltage. This consistent current provides a high effective input to input resistance. Without the red box current sources, the input bias current would vary from zero to twice the normal bias current as the differential input voltage is varied. This is common on other bipolar transistor input op amps. TS321 is an exception to this rule because it does not have the additional current sources.

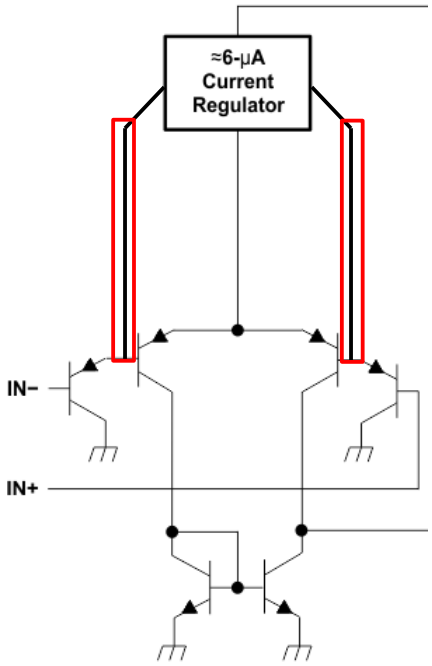

Figure 2. Input Stage Schematic with All Current Source Connections

2.2 Input Common Mode Range

The recommended common mode range is 0 V (relative to the negative supply) to V_{CC} – 2 V over the full temperature range. However, the actual upper common mode range varies by approximately 4 mV/°C, with cold temperatures reducing the upper limit of the common mode voltage range.

Note that when used as a comparator, only one input needs to be within the common mode range. The other input can be above the common mode range or above V_{CC} and the output will be the expected V_{OH} level (for $V_{in}+ > V_{in}–$) or V_{OL} level (for $V_{in} – > V_{in}+$). If both inputs exceed the upper common mode range, the output is undefined; it could be either the V_{OL} or V_{OH} level and the result may vary part-to-part, lot-to-lot, over process, over temperature, etc. If either input or both inputs are lower than –0.3 V with respect to the negative supply, excessive input current can flow and the output may display phase reversal, also called inversion.

Because the inputs have no internal diodes to V_{CC}, the input voltage can exceed the V_{CC} voltage. If this occurs, the input will block current flow due to a reverse biased diode forming in the input PNP transistor. Current flow is blocked even if V_{CC} equals 0 V. If either input or both inputs exceed maximum the V_{CC} rating, junction breakdown can occur. This may lead to permanent device damage per the table notes in the respective device's data sheet *Absolute Maximum Ratings* table.

2.3 Input Impedance

The input stage uses a Darlington PNP configuration with dedicated internal current sources on all of the transistor emitters. Therefore the input appears as a current source to the application. This current is the input PNP transistor's base current whose value is specified in the data sheet as I_{IB}. This effective input current source has a high impedance of approximately 1 GΩ and a wide voltage range compliance from 0 V to one diode drop below V_{CC}, including cases where a large differential input voltage is present (see Figure 4 region B). When the input voltage is greater than one diode voltage drop below V_{CC} or is greater than V_{CC}, the input becomes high impedance and no current flows other than a reverse diode leakage current (see Figure 4 region C). Matching the input resistance can reduce the input offset voltage from I_{IB}. This can be done by placing matching resistors on the inputs. Note that the consequential increase in resistor thermal noise may be unacceptable.

The input current profile for a unity gain buffer powered by a 5-V supply, shown in Figure 3, can be seen in Figure 4. Applying a negative input voltage will forward bias a diode formed from the input PNP transistor's base to the die's grounded substrate on the input pin. The result will be high current flow as indicated by the vertical slope near –0.5 V (region A). An input between 0 V and 3.5 V (region B) has a fixed current (I_{IB}) with an impedance of approximately 1 GΩ. Region C spans from 4.5 V to 7 V and beyond, continuing up to a maximum of V_{CC} where there is no input current flow.

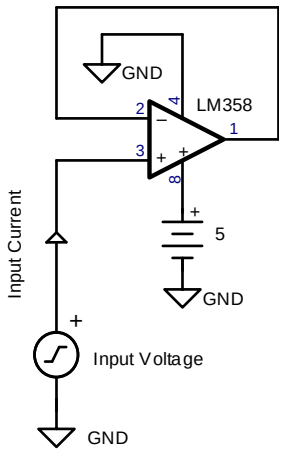

Figure 3. Unity Gain Buffer Test Configuration

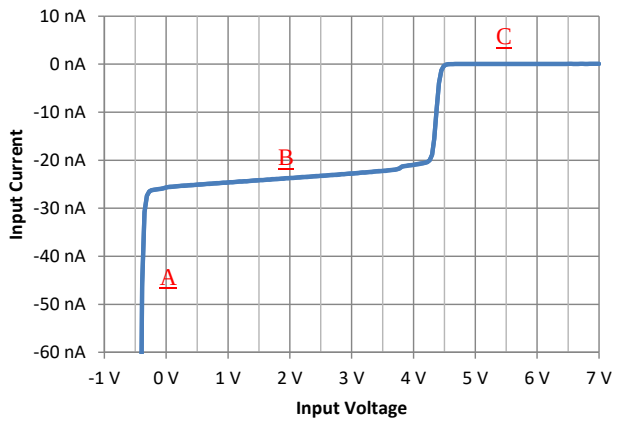

Figure 4. Input Current vs Input Voltage

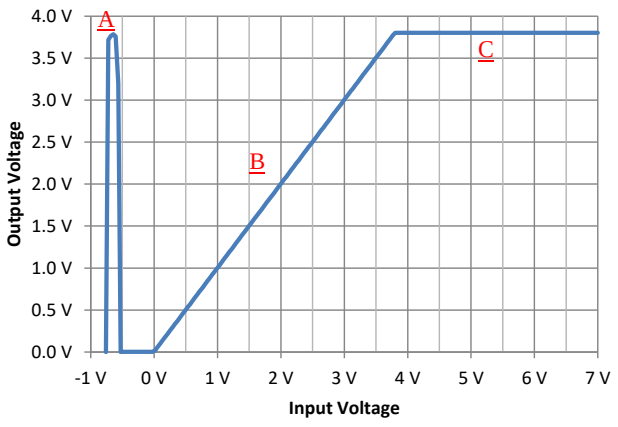

Figure 5. Output Voltage vs Input Voltage

2.4 Phase Reversal

Under certain conditions, the polarity of the output voltage can become inverted. This scenario, called "phase reversal," occurs when the input of the amplifier violates the common-mode voltage range. Figure 5 region ‘A’ shows output phase reversal from an invalid input voltage. A negative input voltage, relative to a grounded V– pin, may come from unexpected sources, such as switching noise or ground bounce in DC to DC converters. Negative input voltages can also arise when rapid fall times and large capacitors combine to temporarily set a negative voltage at the input. An input voltage of less than –0.3 V can cause parasitic diode conduction that results in the output assuming the minimum V_{OL} or maximum V_{OH} level. Operation in this region is not defined in the data sheet as it violates the absolute maximum specification for input voltage. The input current turns on internal parasitic NPN transistors that steal current from other internal nodes causing output phase reversal.

Do not try to determine phase reversal performance empirically as different units may have different performance. Negative inputs must be avoided, assuming a single supply configuration, unless the application can accept either the V_{OL} or V_{OH} level during the duration of the negative input. In cases where a negative input voltage cannot be avoided, use a resistor in series with the input to limit the current to –1 mA or less. This amount of input current is unlikely to cause any damage. If both inputs are above the upper common mode range, the output is undefined; it could be either V_{OL} or V_{OH}. This affects comparator applications, but normal, negative feedback applications are generally not affected because the upper limit of the input voltage range is the same as output high range (V_{OH}).

3 Output Stage Considerations

3.1 Output Stage Schematic, V_{OL} and I_{OL}

The op amp can provide a low output voltage near the negative rail, provided that the load and load termination voltage are aiding the 'Constant Current Sink' driver shown in Figure 6. Table 3 states that the output low voltage is less than 20 mV with a 10-kΩ or less load, assuming the negative supply is at GND. Therefore, if the load resistor is 10 kΩ or less and is terminated to the negative rail, then the load resistor helps the "Constant Current Sink" provide a very low output voltage.

Table 3. Data Sheet V_{OL} Parameter Setup Conditions

Parameter	Test Conditions	Typical	Maximum
V_{OL} Low-Level Output Voltage	$R_L \leq 10$ kΩ	5 mV	20 mV

If the op amp load, including the feedback network, is terminated to a positive voltage, then the op amp must sink current when driving the output low. The output stage seen in Figure 6 has a weak constant current sink consisting of a current regulator that provides a low output voltage for low levels of sink current. The PNP emitter follower can provide a much higher sink current at a higher output voltage.

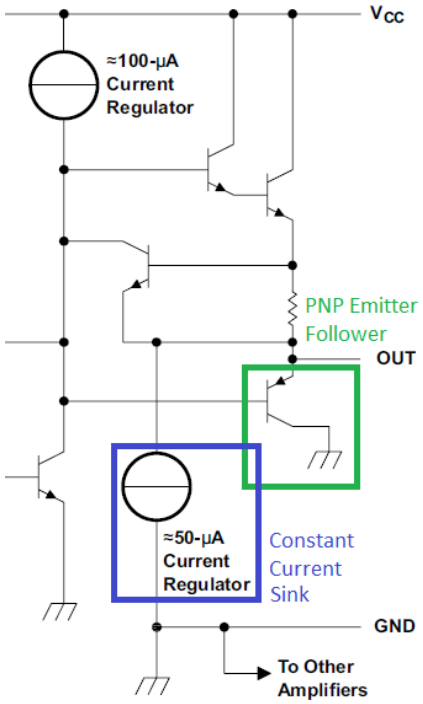

Figure 6. Schematic of Output Driver Stage With Highlighted Sink Drivers

The output pin can sink over 12 µA and still have a less than 200-mV output low level as seen in Table 4. From the electrical characteristics table in the data sheet, the typical output current is 30 µA or 40 µA. The "~50µA Current Regulator" in the device schematic is called a "constant current sink" driver in this application note because the current value is not necessarily 50 µA, as per the electrical characteristics table. Note that the data sheet specification has no maximum limit.

Table 4. Data Sheet Showing Output Current for 200 mV Output Voltage

Parameter	Test Conditions	Minimum	Typical
I_O Output Current	V_{ID} = 1 V < V_O = 200 mV	12 µA	40 µA

The output low voltage is less than 200 mV when sinking up to 12 µA. At higher current levels, the constant current sink is no longer sufficient. So, the PNP emitter follower supplies this current. However, no current is provided by the PNP emitter follower until the output voltage is approximately 600 mV, assuming room temperature. Note that when the PNP emitter follower is active, the V_{OL} level has a temperature coefficient of approximately –2 mV/°C. The PNP emitter follower provides a low output impedance and the base current flows to the output load for a higher efficiency.

Figure 7 plots the low output voltage level vs the sinking current. As can be seen, there is an obvious transition from the constant sink driver (region "A") to the PNP emitter follower (region "B"). Note that the constant sink driver, as its name suggests, is always on.

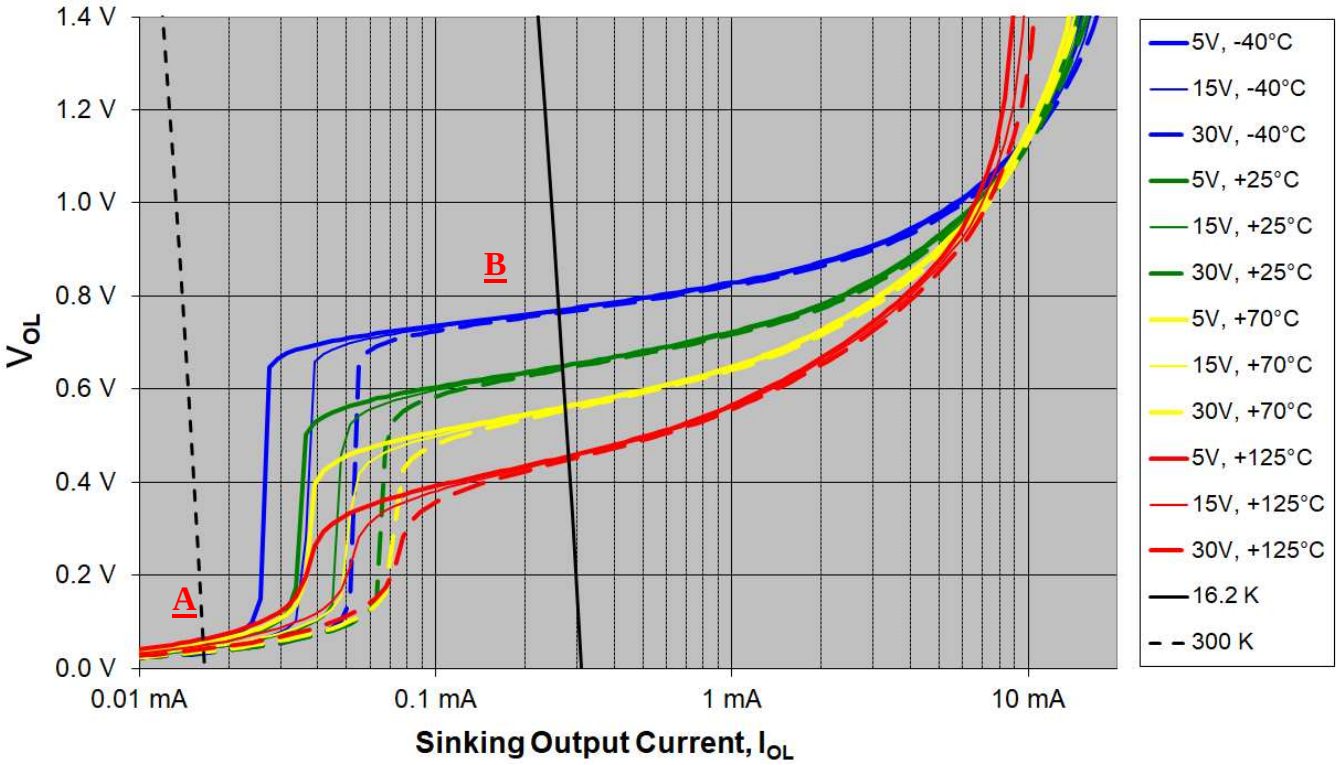

Figure 7. Typical Output Low Voltage vs Output Sinking Current

In Figure 7, two example load lines, a 16-kΩ (solid black line) resistor line and 300-kΩ (dotted black line) resistor line, are shown terminated to 5 V. The 300-kΩ load line intersects the device performance curves at a low V_{OL} level across supply voltage and temperature. Therefore, a low V_{OL} can be expected for this load. The 16-kΩ load line intersects the device performance curves at a higher V_{OL} that varies with temperature, but not with V_{CC}. With this load, a V_{OL} near the negative supply is not possible. If having a low V_{OL} is important, use high resistance loads or loads (including feedback) terminated to the negative supply.

3.2 I_{OL} and Common Mode Voltage

When the op amp is used to sink high current, consider making the input common mode greater than 0.8 V. Also, the maximum sink current of the PNP emitter follower can be reduced when the non-inverting input is 0 V and the junction temperature is high. Figure 8 shows the relation between the non-inverting input voltage and the sinking current with a 2-V output and a junction temperature of 125°C.

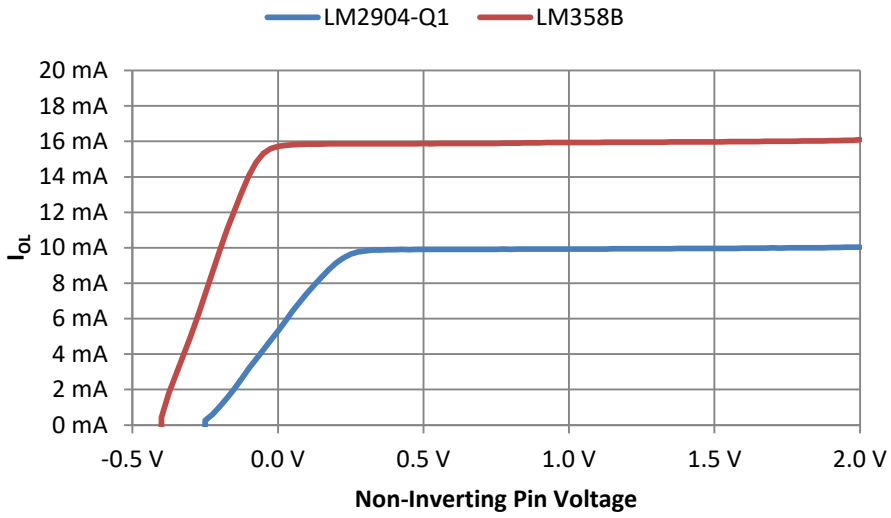

Figure 8. I_{OL} vs Non-Inverting Pin Voltage, V_{CC} = 5 V, V_{OUT} = 2 V, T_J = 125°C

If a high sink current during faults is undesirable, such as an accidental output short to power, setting the common mode voltage to 0 V can offer some reduction in sinking current as the die temperature increases. Shorts to positive voltage may damage the device as stated in the absolute maximum rating table in the data sheets. Damage is more likely if the short voltage is greater than 10 V relative to the GND, or V–, pin.

3.3 Output Stage Schematic, V_{OH} and I_{OH}

Unlike most new op amps that have a rail-to-rail output, this family of op amps has a high level output voltage that is significantly lower than the V_{CC} power rail, regardless of the load sourcing current. Figure 9 shows the Darlington NPN transistors that provide sourcing current. An active current limiter helps protect the op amp and load from overcurrent conditions.

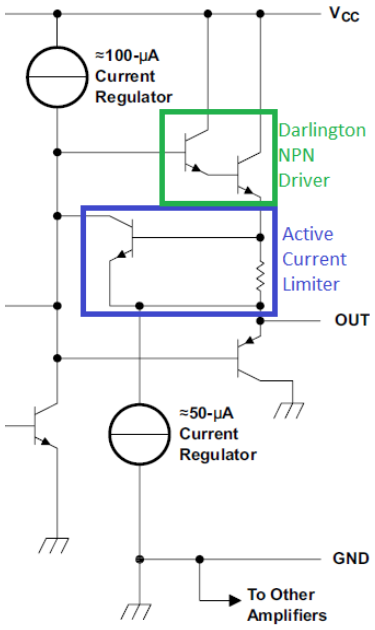

Figure 9. Schematic of Output Driver Stage with Highlighted Source Driver and Current Limiter

The Darlington NPN provides a low output impedance and the base current flows to the output load for higher efficiency. This setup has a high headroom requirement that significantly reduces the V_{OH} level. The two base emitter junctions in the Darlington NPN have a combined temperature coefficient of approximately –4 mV/°C. Therefore V_{OH} has an equal and opposite temperature coefficient of 4 mV/°C. Per the data sheet *Electrical Characteristics* tables, the V_{OH} level is V_{CC} – 1.5 V or better with a 2-kΩ load to ground when V_{CC} is 5 V at 25°C. The typical V_{OH} level varies with load current and also varies with temperature as seen in Figure 10. V_{OH} performance relative to V_{CC} is independent of V_{CC}, which means the set of curves in Figure 10 apply to the entire operating range of V_{CC}.

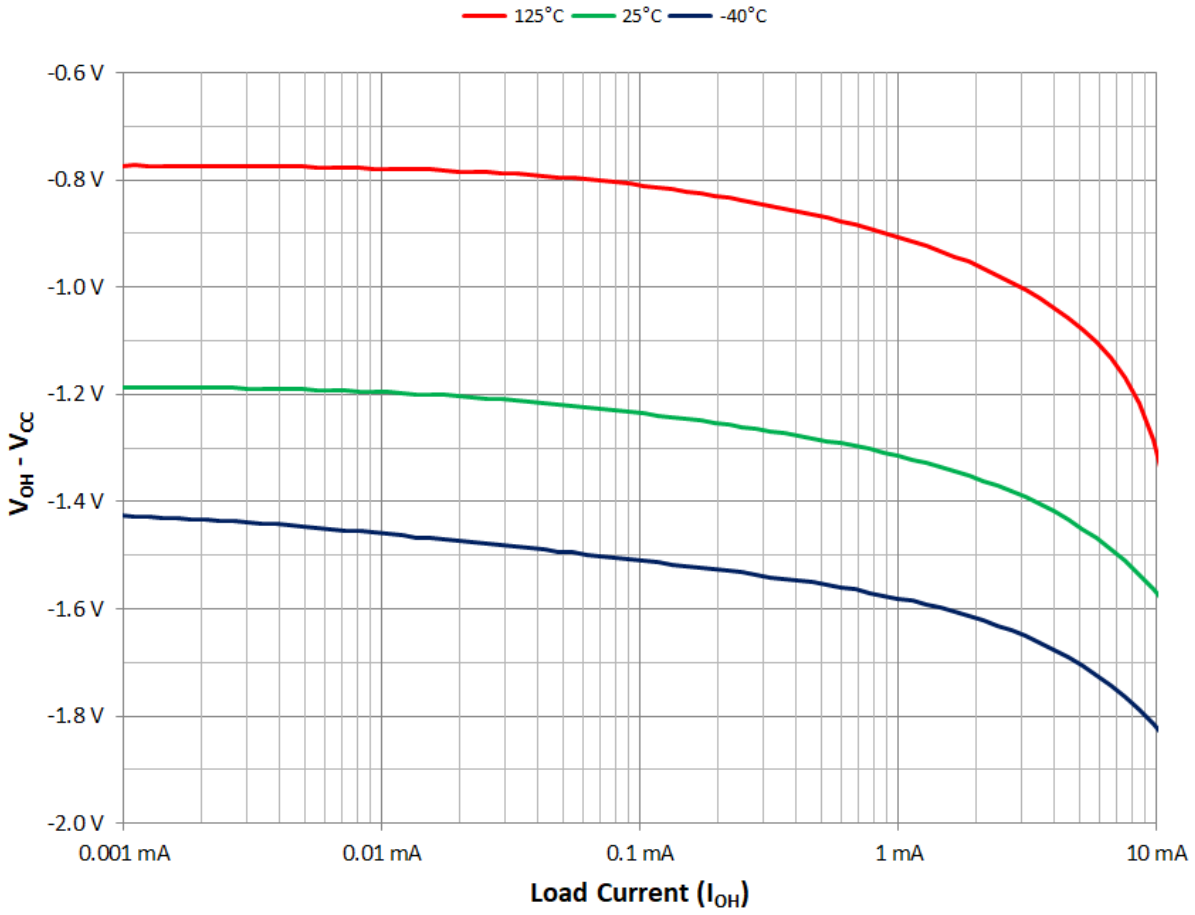

Figure 10. Plot Showing V_{OH} Relative to V_{CC} (V_{OH} - V_{CC}) vs Load Current (I_{OH})

3.4 Short Circuit Sourcing Current

The Darlington NPN driver has a current limiting circuit to protect against shorts to ground. The current limiting feature protects the device from immediate damage. However, device overheating can occur during prolonged shorts especially when the $V_{CC} – V_{OUT}$ voltage is high. Note that power dissipation in the op amp is $((V_{CC} – V_{OUT}) \times I_{OUT})$. The op amp sets I_{OUT} and the application determines both the V_{CC} value and the short voltage, V_{OUT} , affecting the power dissipated. The op amp has no over-temperature shutdown circuitry. Therefore, excessive power dispassion can lead to very high die temperature. The data sheet absolute maximum ratings table only allows shorts to ground for $V_{CC} \leq 15$ V. The current limit magnitude, in Figure 11, decreases as die temperature increases.

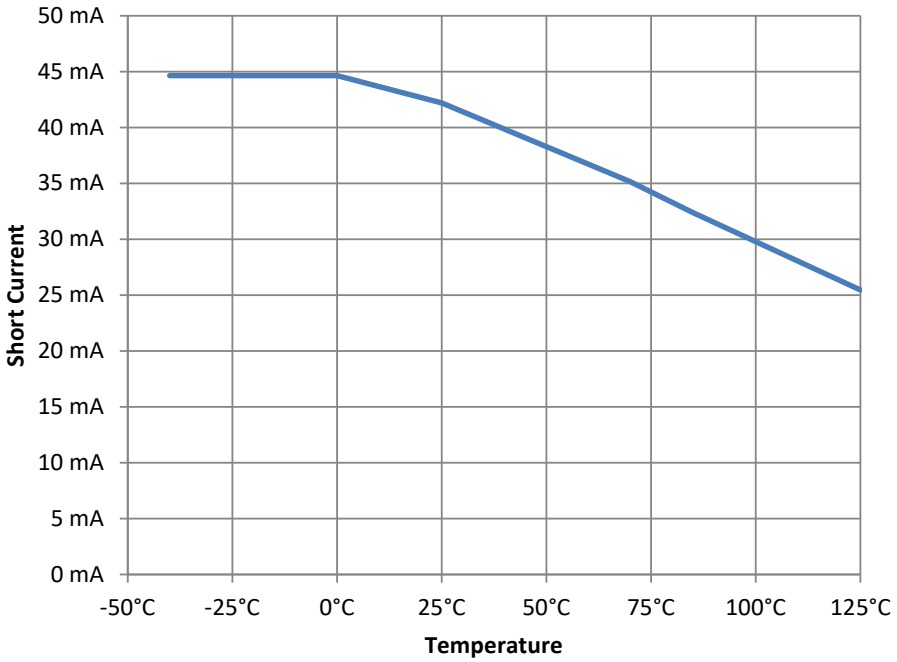

Figure 11. Plot Showing Short Circuit Current vs Junction Temperature

4 AC Performance

4.1 Slew Rate and Bandwidth

All slew rate and bandwidth specifications are typical and not tested in production. The typical values vary marginally among channel count variants.

Table 5. Typical Slew Rate and Gain Bandwidth

Typical	Single	Dual	Quad
Slew Rate	0.4 V/µs	0.3 V/µs	0.5 V/µs
Bandwidth	0.8 MHz	0.7 MHz	1.2 MHz

4.2 Slew Rate Variability

It is best to allow for some margin between the application's slew rate requirement and the typical slew rate of the device used. Normal process variance affects internal bias currents and capacitor oxide thickness, which are two factors that determine slew rate. These components are highlighted in blue in Figure 12. There may also be a slight difference between the positive and negative slew rates. The reason for this difference is simple: the transistor in the red box in Figure 12 has no turn off drive. The NPN transistor driving the red box transistor can only source current to turn on, but can't sink current to turn off. The base to collector capacitance of the transistor in the red box in this device family varies among the dies in production. The NPN transistor's beta is also a factor in determining slew rate. If the natural turn off slew rate of the red boxed transistor

$$SR_{Natural} = \frac{100\ \mu A}{\beta_{NPN} \times Cap_{CB}}$$

is slower than the slew rate set by the bias and compensation capacitor

$$SR_{Comp} = \frac{6\ \mu A}{Cap_{Comp}}$$

then the positive slew rate will be reduced while the negative slew rate is not affected. Hence, the positive slew rate can be slower than the negative slew rate. LM358B and LM2904B have a discharge path for the base of the red boxed transistor. Therefore, the slew rate will not be affected by this highlighted transistor.

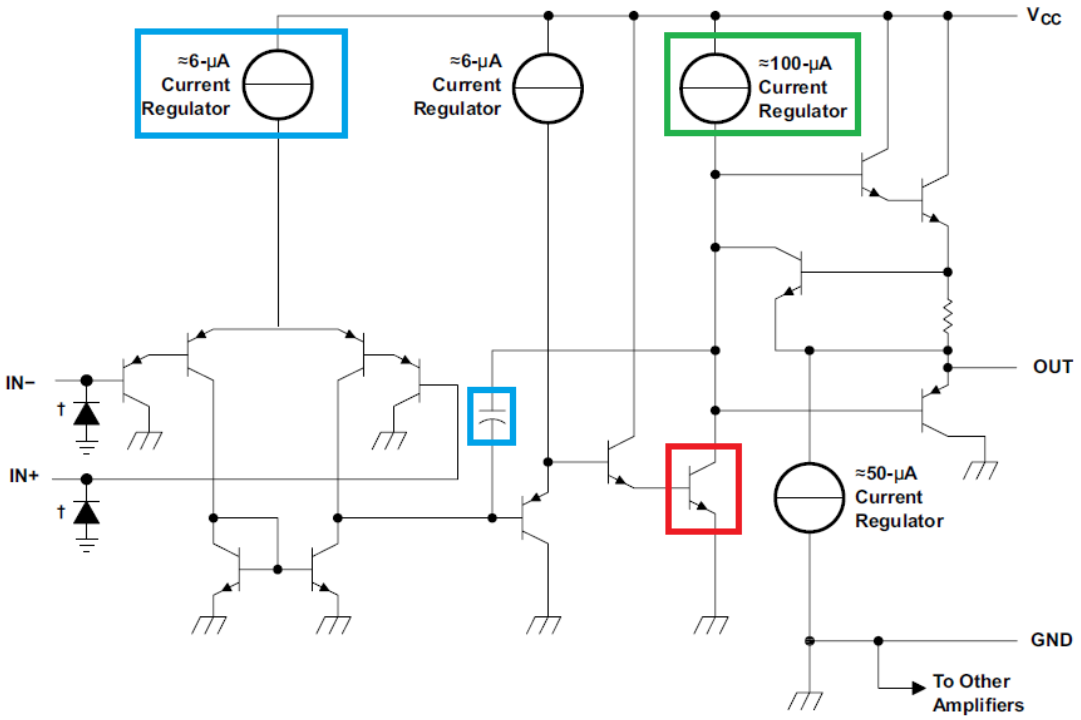

Figure 12. Schematic With the Following Slew Rate Components Highlighted: Tail Current (Blue), Compensation Capacitor (Blue), Collector Current (Green), Collector to Base Capacitance (Red)

Only the commercial grade quad op amp with the widest input offset specification has a die with enough base-collector capacitance to typically demonstrate variation in high temperature slew rates. Slew rate differing in all other device variants will be a rare occurrence. The key point is not to depend on matching slew rate. Fortunately, few circuits actually require matching slew rate. For reference, the slew rate curves of two common devices are shown below with the commercial grade in Figure 13 and the automotive grade in Figure 14. Note that the other die designs typically have matching positive and negative slew rates. A small percentage of samples may exhibit some differences at high temperature.

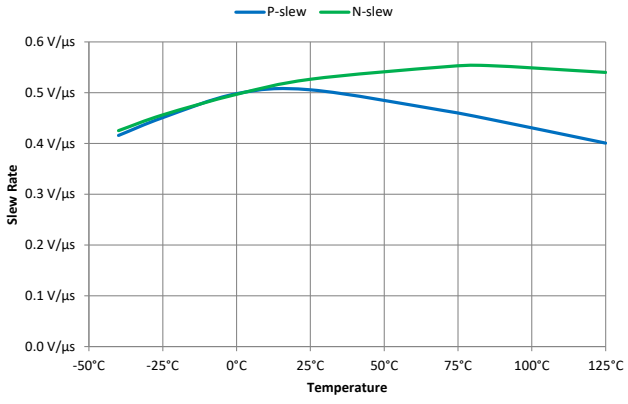

Figure 13. Plot Showing Slew Rate vs Temperature for LM2902DR

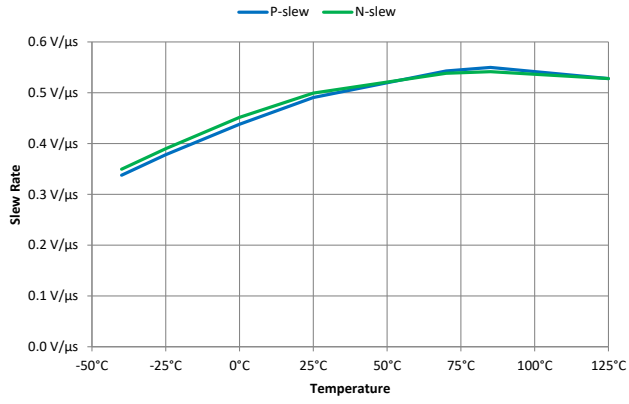

Figure 14. Slew Rate vs Temperature for LM2902QDRQ1

4.3 Output Crossover Time Delay

This op amp family does not provide any static bias for any of the output transistors (Class B type) highlighted in the blue boxes in Figure 15. Most other op amp designs provide a small static bias to the output transistors (Class AB type) to make output current transitions seamless. The advantage of having no static bias is allowing the 'Constant Current Sink' driver to pull the output close to the negative supply voltage. The disadvantage of having no static bias is a time delay when switching between the output source and sink drivers.

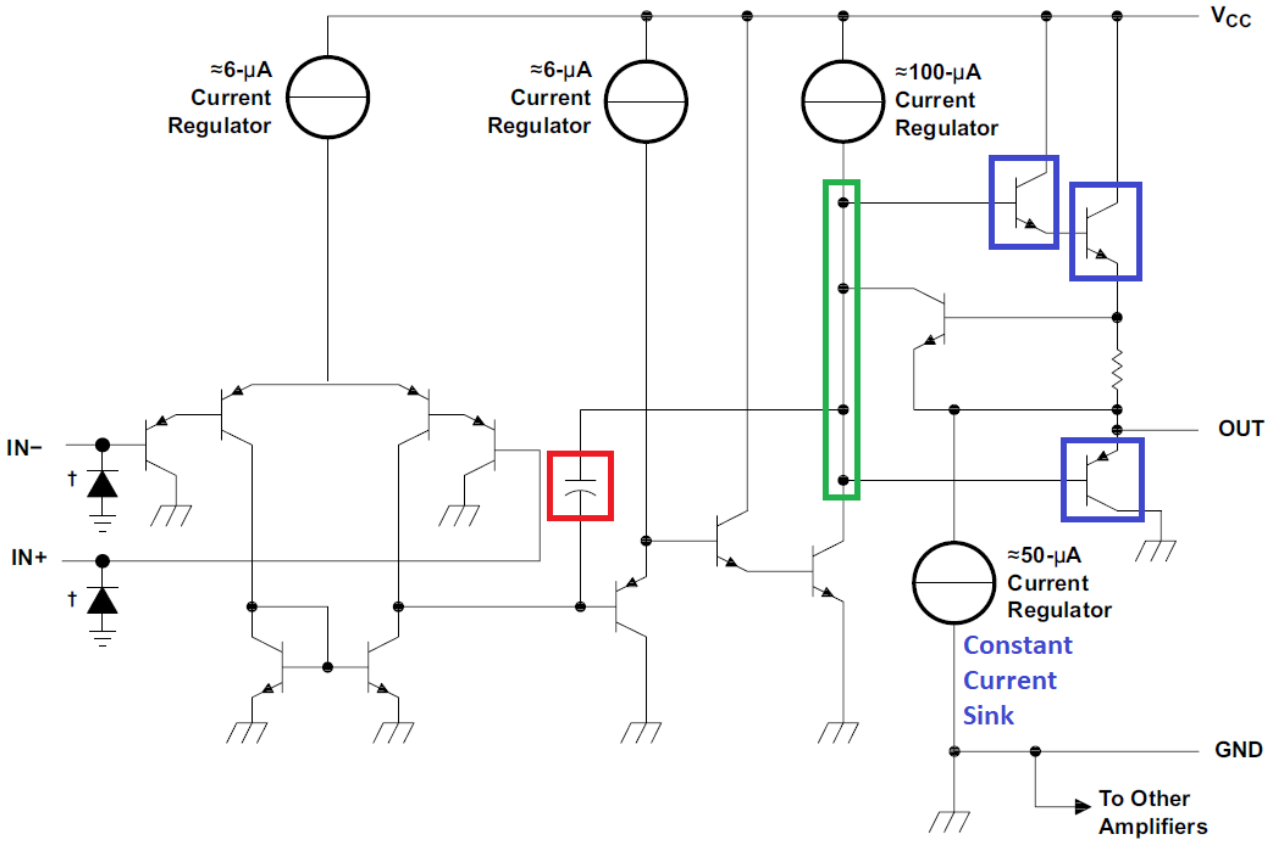

Figure 15. Schematic with the Following Time Delay Components Highlighted: Shared Input Node (Green), Compensation Capacitor (Red), and Output Transistors (Blue)

The op amp's Darlington NPN driver and PNP emitter follower output transistors share an input signal highlighted in the green box. The compensation capacitor is also connected to this common node. Therefore, the slew rate of the green node is the same as the output's slew rate, which can be found on the data sheet as a typical value. When the op amp needs to change between the Darlington NPN and PNP emitter follower drivers, there is a time delay of approximately

$$T_{Delay} = \frac{3 \times V_{BE}}{Slew\ Rate}$$

Depending on the application, this delay may or may not be significant. The maximum application frequency and load current range are relevant factors in determining whether or not the time delay will be significant.

Two test circuits, shown in Figure 16 and Figure 18, are specifically designed to maximize the visual effect of the crossover time delay. In many applications, the crossover time does not cause any issues. However, extra care should be taken when there are high frequency signals, fast rise or fall times, or when distortion must be minimized. Output pull down or pull up resistors can be added to keep either the output source or sink driver continually active, thereby preventing time delays.

4.4 First Crossover Example

The first example test circuit in Figure 16 uses the LM324 as a 10-kHz frequency sine wave buffer. The input signal is a ±1-V peak, 10-kHz sine wave. The supply voltage is ±5 V. The load is always 2.7 kΩ, regardless of the switch position. But, the termination voltage for the resistor can be switched between –5 V, 0 V, and 5 V. Ideally, the op amp output would follow the input voltage sine wave as the load current is small and the output slew rate required is well below the typical slew rate specification.

$$SR_{Required} = V_{PP} \times f \times \pi = 2V \times 10kHz \times \pi = 0.063 \frac{V}{\mu s}$$

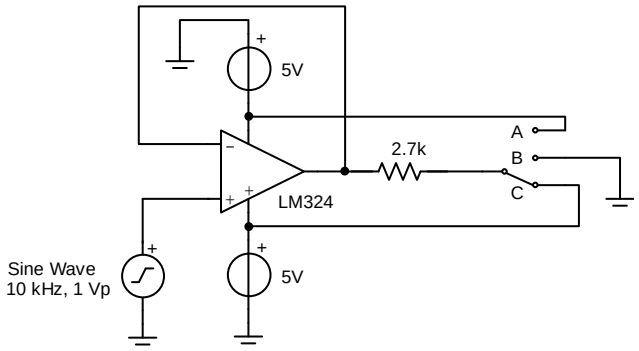

Figure 16. Crossover Test Schematic

Case A: With the switch in position “A”, the load resistor is terminated to –5 V. So, the op amp will always source current. This current will vary from 1.48 mA to 2.22 mA. The output will follow the input as the Darlington NPN driver is always active as seen in the green waveform in Figure 17.

Case B: With the switch in position “B”, the load resistor is terminated to 0 V, or mid-supply. Therefore, the op amp will source and sink current, requiring the output to change drivers. The current will vary from –0.37 mA to 0.37 mA. Since the output driver will switch between PNP and NPN, the green box node voltage in Figure 15 has to slew to a voltage of three times V_{BE} before the output voltage can change. At 25°C, the time needed to switch current polarity is

$$\frac{3 \times V_{BE}}{\text{Slew Rate}} = \frac{2\ V}{0.5\ V/\mu s} = 4\ \mu s \quad (1)$$

The output waveform flattens for 4 µs as only the weak constant current sink is active and neither the Darlington NPN driver nor the PNP emitter follower drivers are active during this time. See the red waveform in Figure 17. The voltage value of this flat time is 2.7 kΩ, or the load resistance, multiplied by the constant current sink value. After the delay, the output voltage changes at the device’s slew rate limit until it assumes the correct value. This happens each time the op amp switches between the source current and sink current drivers. The constant current sink is always on, but it is insufficient current to drive the 2.7-kΩ load resistor to –1 V by itself. Only the newest device simulation models dated 2018 or later include this time delay in the model.

Case C: With the switch in position “C”, the load resistor is terminated to 5 V. Thus, the op amp will always sink current. The current will vary from –1.48 mA to –2.22 mA. The output will follow the input as the PNP emitter follower will always be active. See the purple waveform in Figure 17.

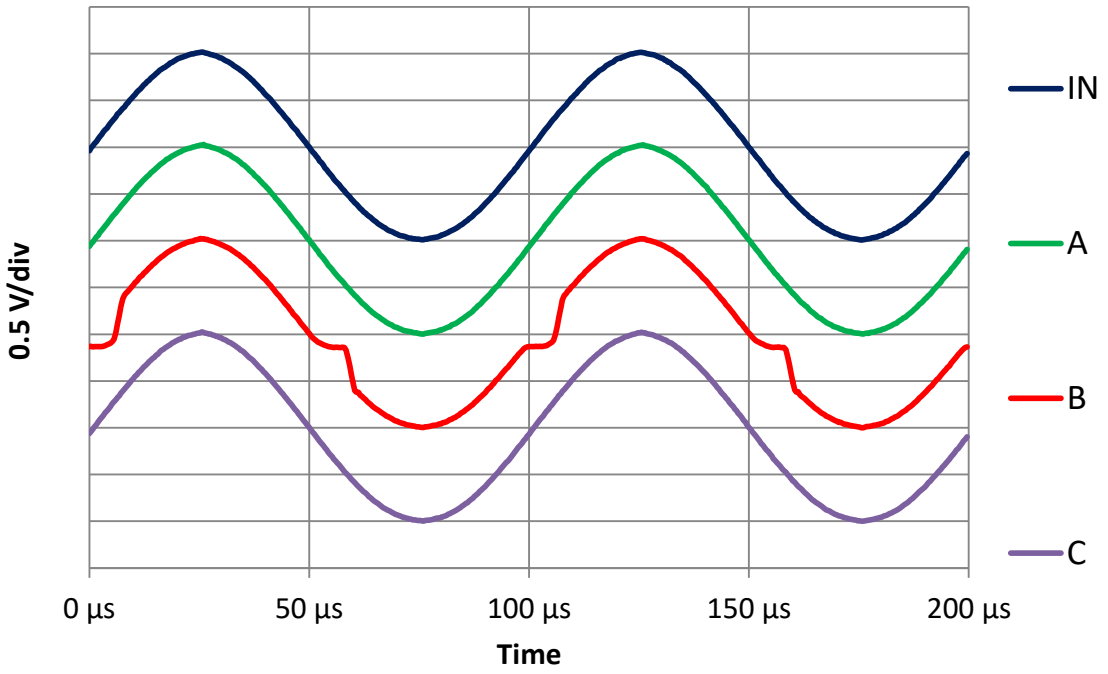

Figure 17. LM324 Crossover Test Waveforms

4.5 Second Crossover Example

Crossover can also occur when the load current changes from an external source as seen in Figure 18. The LM358 is set up as a reference voltage buffer and the load current alternates between 1 mA and –1 mA.

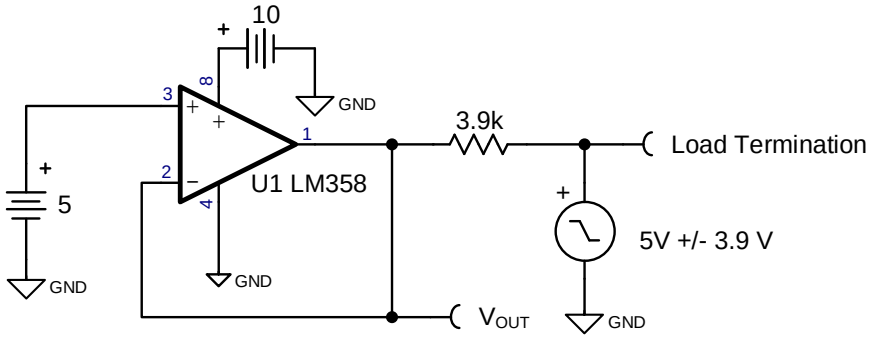

Figure 18. Second Crossover Test Schematic

The LM358 load current is stepped ±1 mA using a pulse generator square wave and a series resistor. Ideally, the output voltage should be constant at 5 V. However the output voltage jumps by 2 V, or about 3 × V_{BE}, before the other output driver can provide current flow. At 25°C, the time needed to correct the output signal back to 5 V is about

$$\frac{2\ \text{V}}{0.3\ \text{V}/\mu\text{s}} = 6.7\ \mu\text{s} \quad (2)$$

The LM358 has a slower typical slew rate than the LM324. Consequently, the time delay is greater in the LM358. The oscilloscope capture in Figure 19 shows as example output waveform in red and a pulse generator output in dotted blue. From this real-world data, we see that output crossover can create output steps and flat waveforms followed by a correction period.

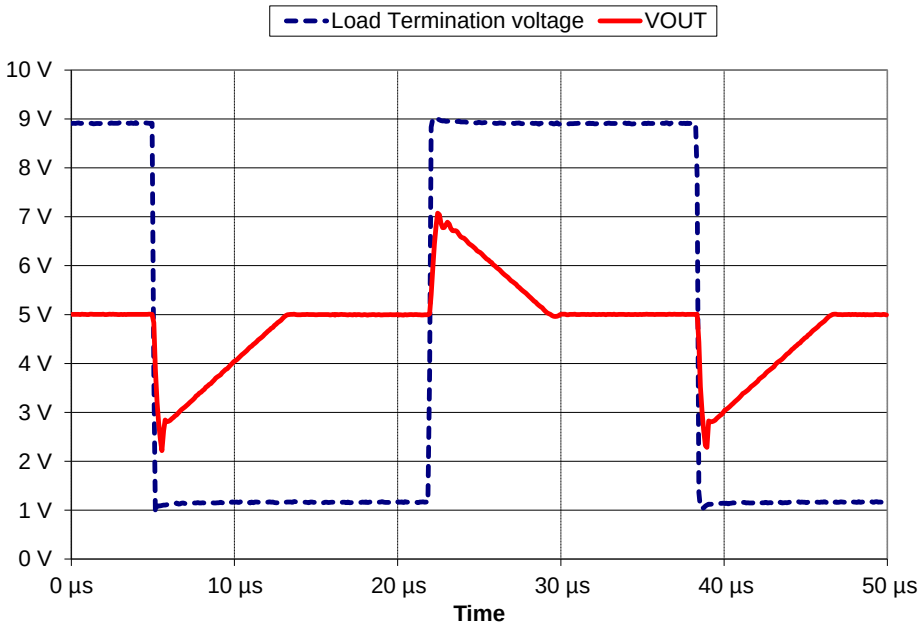

Figure 19. LM358 Crossover Test Waveforms

5 Low V_{cc} Guidance

The minimum V_{CC} for this device family is 3 V and many applications use a 5-V supply with good results. For lower supply voltages, such as those in the range of 3 V to 3.6 V, pay careful attention to the input and output voltage ranges. Note that these are especially limited at the device's lowest operating temperature. For more information on this topic and device family, please consult the General Purpose Amps at Low Voltage blog.

5.1 Low V_{cc} Input Range Supporting –40°C

The input common mode range for the op amp with a 3-V supply at –40°C is 0 V to 1 V, as per the data sheet. This design requirement is easy to meet when the input signal is small. It is also easy to meet when an inverting gain configuration is used because this configuration allows for a fixed common mode voltage to be set between 0 V and 1 V.

5.2 Low V_{cc} Output Range Supporting –40°C

The output range is typically 0.75 V to 1.5 V for a bidirectional load current of 100 µA at –40°C. This output range is just 25% of the supply voltage range. The output range can be increased to 0.1 V to 1.5 V with a bidirectional load current of 12 µA. If all loads terminate to ground, then the output range is 0 V to 1.4 V for a 1-mA load. The largest output range possible requires using an external pull up resistor. For example, using a 5-kΩ resistor gives a typical –40°C output range from 0.8 V to 2.7 V.

Lower resistance gives more design margin and a slightly higher, typical range. V_{OH} improves with lower resistance, but V_{OL} degrades and power consumption increases. The op amp doesn't oppose the pull up resistor other than the constant sink driver current that is always on. The high output level is limited by the pull up resistor, feedback, and other loads. The constant sink current driver will reduce V_{OH} as this current flows through the pull up resistor. All of the output ranges in this section are based on the typical V_{OH} and V_{OL} curves in this application note. Always add design margin when using typical data.

Figure 20 shows typical I_{OH} vs V_{OH} curves given T_a = 25°C and V_{CC} = 3 V. The constant current sink driver from Figure 6 is responsible for this current flow. This current value can vary from device to device and across temperature. Do not pull up the output to a voltage higher than V_{CC} unless an external diode to V_{CC} is used to limit output voltage.

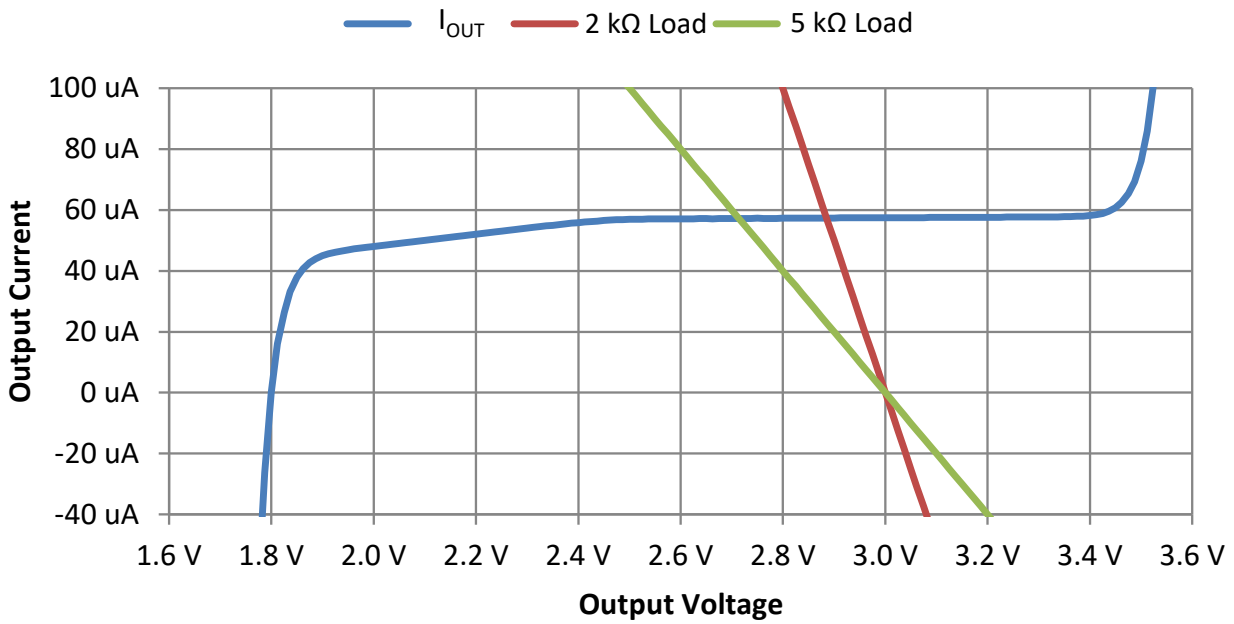

Figure 20. Output Current vs Output Voltage for Pull Up Resistor Usage

The output V_{OH} level will be significantly increased by a pull up resistor that provides at least 100 µA. In Figure 20, output current vs output voltage was measured. Two pull up resistor load lines, 2 kΩ and 5 kΩ, are included on the chart. With no pull up resistor or any other load, the current will be zero and V_{OH} will be 1.8 V. The 5-kΩ resistor load line intersects the output current curve at V_{OH} = 2.73 V and the 2-kΩ load line intersects the output current curve at V_{OH} = 2.88 V. If the output current were 100 µA, then V_{OH} would be reduced to [2.8 V, 2.5 V] for the [2k , 5k] loads. Note that another advantage of unidirectional current or very low bidirectional current is the lack of time delay that occurs when switching between the NPN Darlington and PNP emitter follower drivers.

In this family of devices, TS321, LM358B, and LM2904B typically have higher constant sink currents. Therefore, pull down resistors are recommended instead of pull up resistors for these parts.

5.3 Low V_{CC} Audio Amplifier Example

To demonstrate that 3 V is a usable yet challenging supply voltage, an example involving a 3-V audio pre-amplifier with LM2904DR is considered (see Figure 21). This amplifier has a 40-dB bandpass gain and –3-dB corners at 30 Hz and 10 kHz. Pull up resistors (RP1, RP2) were added to increase the output range to 0.9 V to 2.7 V at the worst case temperature of –40°C. For a maximum output swing without clipping, an output bias point of 1.76 V was used, which is halfway between the expected V_{OL} and V_{OH} values, and the input bias point is was at half of the output, 0.88 V because it is simple and meets the 0-V to 1-V input range. Higher temperature will improve the V_{OL} range and a higher V_{CC} will improve the V_{OH} range. This means there is more design margin against low peak output clipping at warmer temperatures and more design margin against high peak output clipping with a larger V_{CC}.

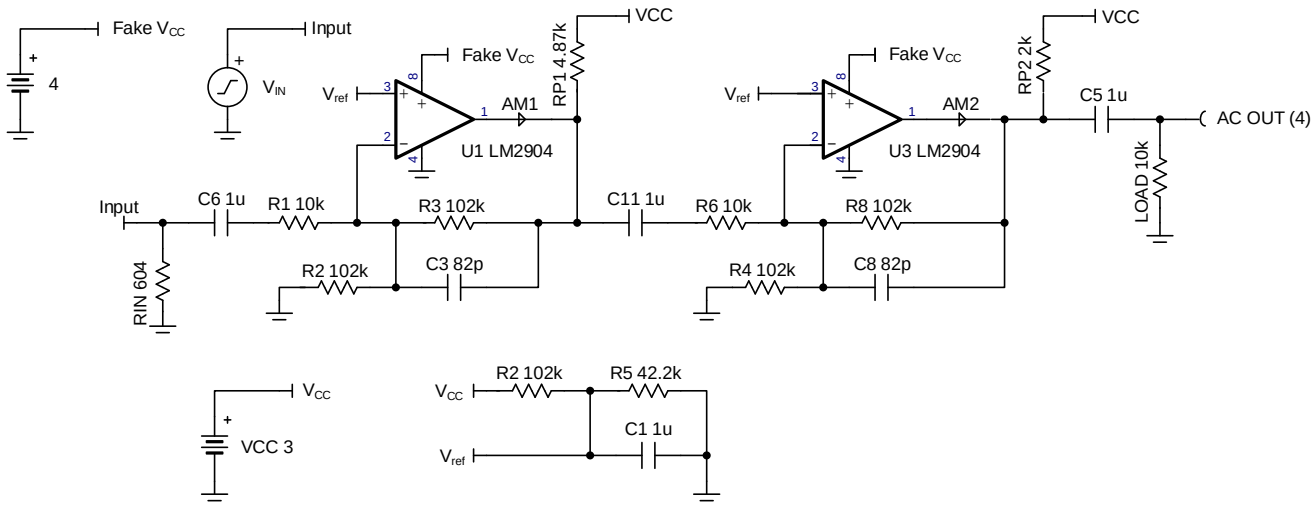

Figure 21. 3-V Audio Bandpass Amplifier Schematic

For the resulting simulation to work correctly, a "fake" V_{CC} set to 4 V was used because the LM2904 model does not support pull up resistors that improve V_{OH}. The model fights the pull up resistor, but real-world devices will not do so. AM1 and AM2 simulation meters are used to check the output current's magnitude and polarity. Ensure the current meters are more negative than –100 µA. The current needs to be greater than a strong constant current sink sample so the PNP emitter follower always conducts some current to prevent crossover time delay. Figure 22 is the simulation result for the output voltage and output currents. The minimum negative output current is more negative than –100 µA with an 8-mV peak input signal.

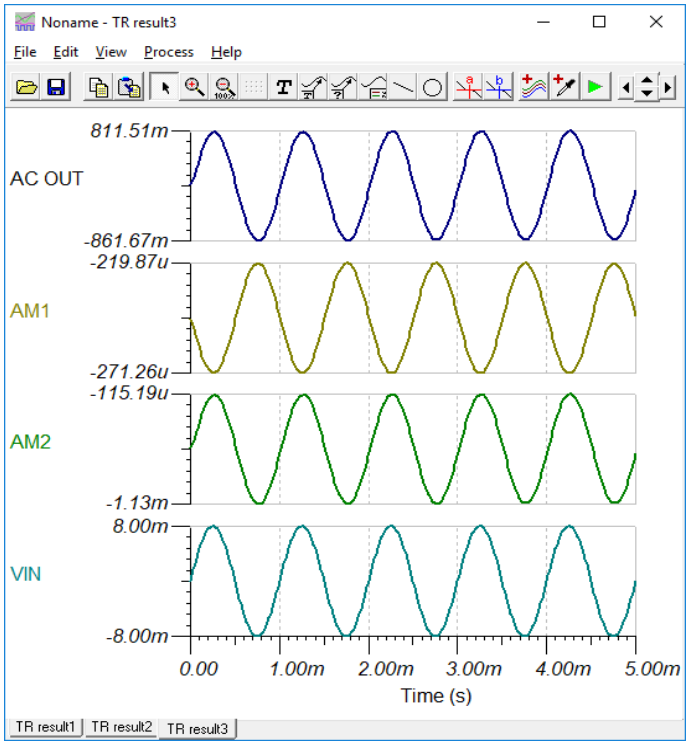

Figure 22. Simulation of 1-kHz Sine Wave Transient

Figure 23 shows the bench test results for V_{CC} = 3 V at T_a = –40°C. From the resulting plots, the maximum output without clipping was 1.82 V_{pp}. The top waveform is the U3 output and the bottom waveform is the input signal. Figure 24 shows the plot of gain vs frequency at V_{CC} = 3 V, T_a = 25°C.

From this discussion we can conclude that 3-V supply designs can be used successfully. However, applications using 5-V or higher supply will be easier to design.

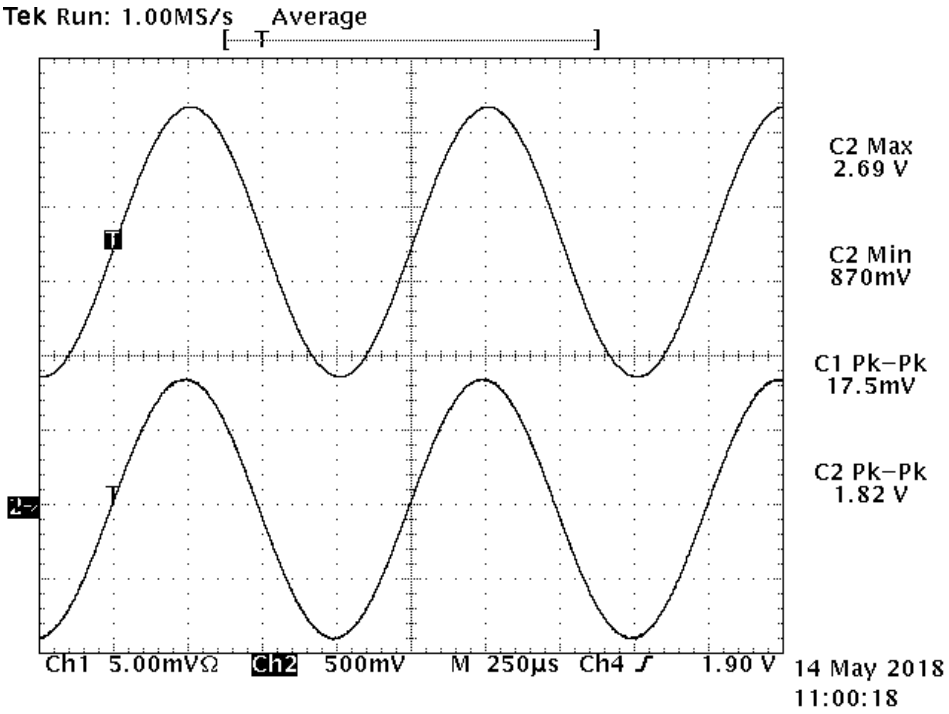

Figure 23. Bench Testing 1-kHz Maximum Amplitude Without Clipping Waveforms

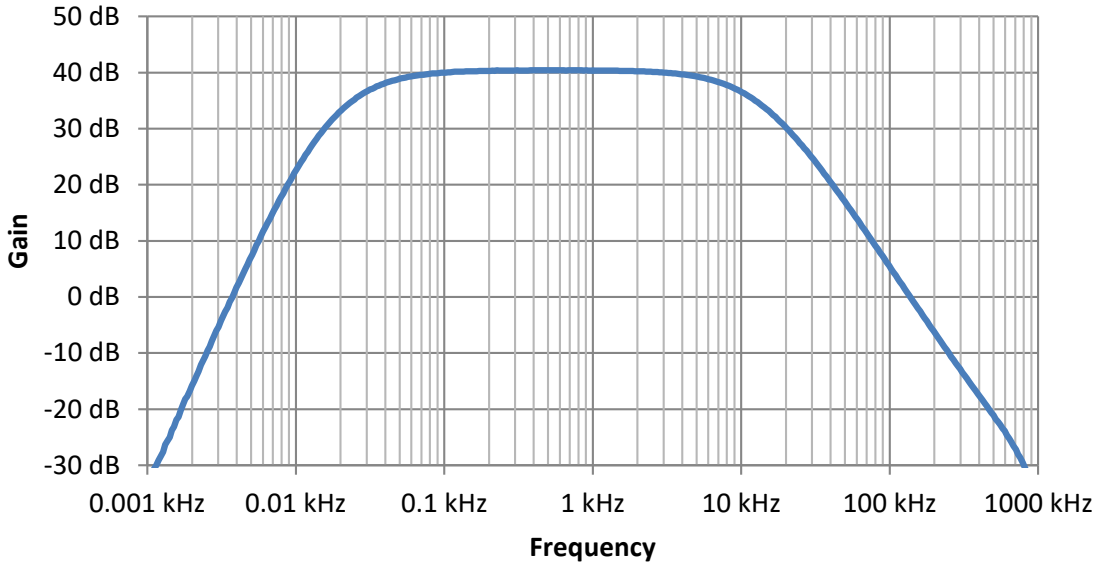

Figure 24. Amplifier Voltage Gain vs Frequency

6 Comparator Usage

6.1 Op Amp Limitations

Op amps generally do not make good comparators. However, there are reasons to occasionally use an op amp as a comparator. These include having an unused amplifier, having no timing requirements, and having inputs that exceed V_{CC}.

6.2 Input and Output Voltage Ranges

When using an op amp as a comparator, the key DC parameters to consider are input offset voltage, input common mode range, low output voltage (V_{OL}) and high output voltage (V_{OH}). It is important to maintain a valid input common mode, otherwise phase reversal may occur as discussed earlier in this document. When used in a comparator application, the input common mode voltage of the op amp will be the same as the least positive input voltage. For example, if one input is 2 V and the other input is 3 V, the common mode voltage would be 2 V. The voltage of the other, higher voltage input doesn't affect the input common mode voltage in this device family and many other PNP and PMOS op amp families.

6.3 Overload Recovery

Overload recovery time is analogous to comparator propagation delay. Overload occurs when an op amp's input voltage difference is large enough such that the output reaches either the V_{OL} or V_{OH} level and the output no longer changes with variations in the input. Some internal node voltages will continue to change even though the op amp output is not changing. The overload condition ends when the input voltage difference is reduced to a point where the op amp returns to a linear operating region or the input voltage polarity is reversed. After the overload condition is removed, there is a finite time delay before the output can change from the V_{OL} or V_{OH} level. This delay is the overload recovery time. The data sheet does not specify an overload recovery time parameter. The recovery time when the output is at the V_{OH} level is approximately 2 µs, regardless of the common mode voltage. The recovery time when the output is at V_{OL} varies with the common mode voltage present at the non-inverting input as seen in Figure 25.

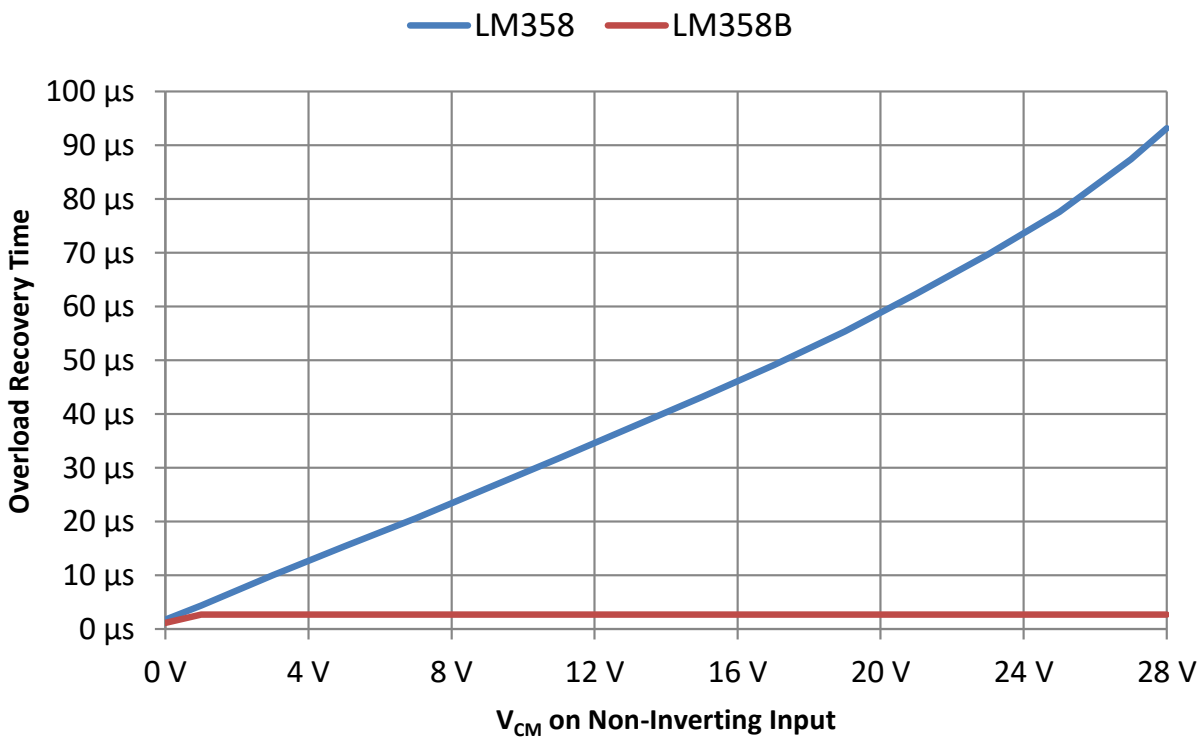

Figure 25. Overload Recovery Time from V_{OL} vs V_{IN+}, V_{ID} = 200 mV, V_{CC} = 30 V

The reason for variable overload recovery time for V_{OL} is shown in Figure 26. The voltage of the difference amplifier stage output (red box node) normally runs near 0.6 V when the op amp is in the linear (normal) operation mode. During a negative (V_{ID} < 0) input overload event where the output is at the V_{OL} level, this node rises to V_{CM} + 1.3 V while the other side of the capacitor is 0 V. This charges the capacitor to a voltage set by the voltage present on IN+ pin.

LM358B and LM2904B limit the red box node's voltage to 1.2 V. Consequently, the overload recovery time does not increase with the IN+ voltage. When the input overload is removed, the difference amp output node voltage returns to 0.6 V. The time for this to happen depends on the input voltage difference and internal factors, such as the current of the leftmost 6-µA current regulator and the capacitance of the internal compensation capacitor highlighted in the blue box in Figure 26.

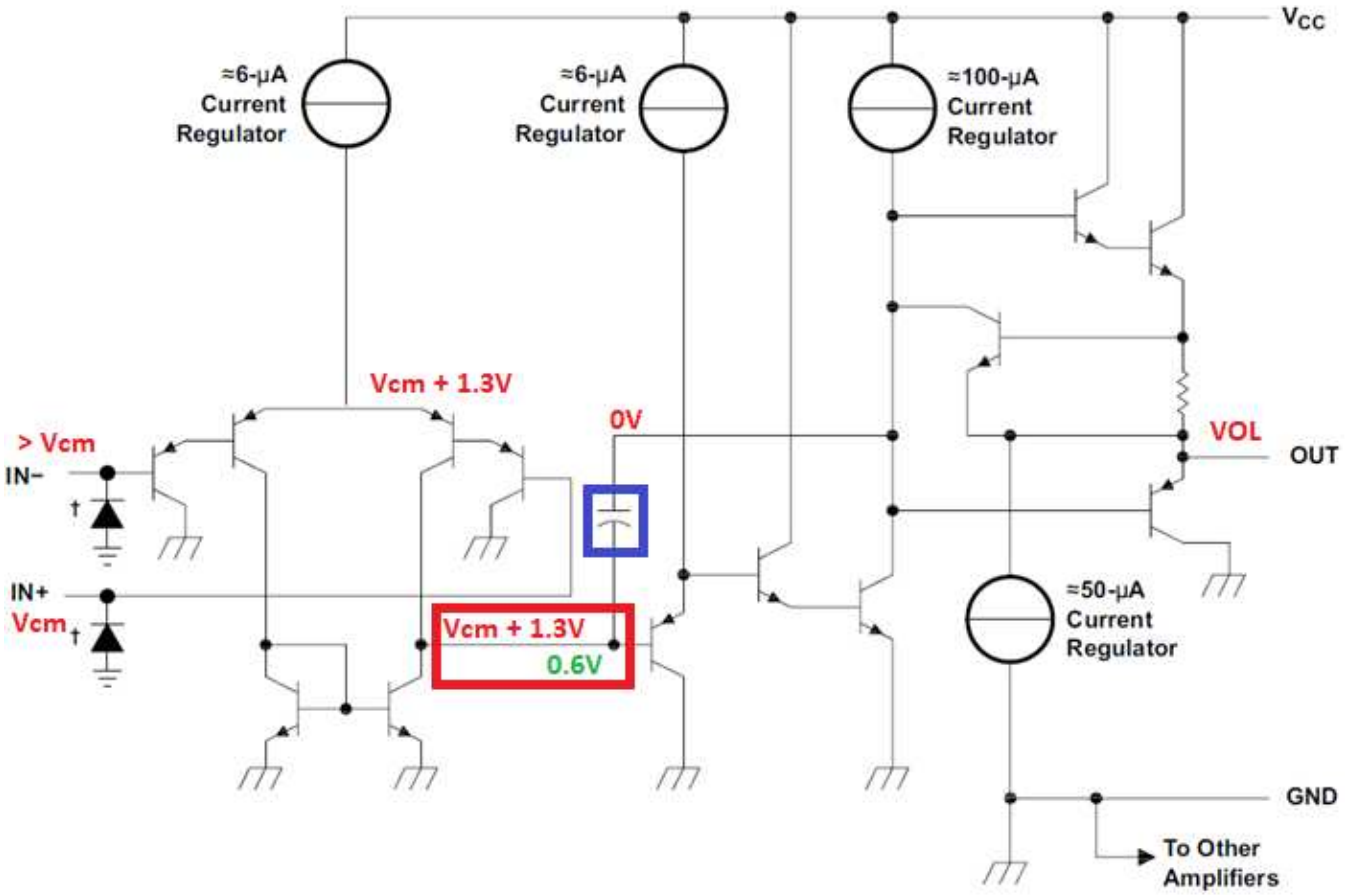

Figure 26. Overload Recovery from V_{OL} State

In addition to the overload recovery time of 2 µs from the V_{OH} state or the overload recovery time in Figure 25 from the V_{OL} state, the input voltage difference applied during the input recovery time is also a factor in the actual recovery time. One can multiply the internal factor time (2 µs or the time from Figure 25) by the scalar value in Figure 27 to get the final expected recovery time. V_{ID} is the voltage applied while waiting for the recovery time.

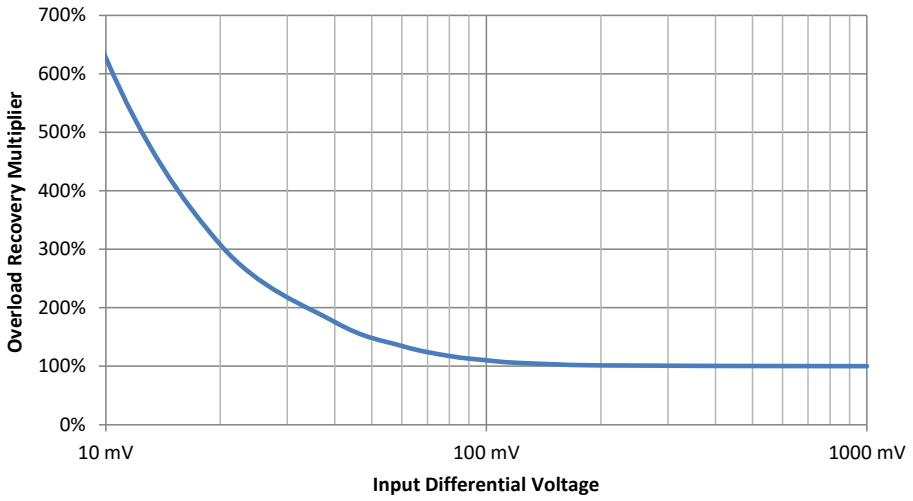

Figure 27. Overload Recovery Multiplier vs Input Differential Voltage (V_{ID})

For example, assume the LM358 output is in a V_{OL} state, the non-inverting input is 10 V, and the inverting input is 10.05 V. If the inverting input suddenly drops to 9.98 V, then the output will start increasing after approximately 90 µs. The input common mode was 10 V, which makes the overload recovery time 30 µs, per Figure 25. The input difference is 10 V – 9.98 V = 20 mV which makes the multiplier 300%, per Figure 27. Multiply the two values; 30 µs × 300% = 90 µs. Later when the inverting input suddenly rises back to 10.05 V, the output will start decreasing after approximately 3 µs. The output was V_{OH}, so the recovery time is 2 µs. The input difference is 10.05 V – 10 V = 50 mV, which makes the multiplier 150%, per Figure 27. Multiply the two values; 2 µs × 150% = 3 µs.

6.4 Slew Rate

Slew rate (SR) limits the output rise and fall times, which are defined as $(V_{OH} – V_{OL})/SR$. Slew rate, as specified in the op amp data sheet, is applicable for large differential input voltages. Dedicated comparator parts, on the other hand, may have much smaller differential input voltages. Note that the slew rate is reduced when the input difference voltage is small. Figure 27 shows that an input difference of 100 mV provides a slew rate 90% as fast as the data sheet setup result and a 10-mV input difference voltage has a slew rate that is only 16% of the data sheet slew rate.

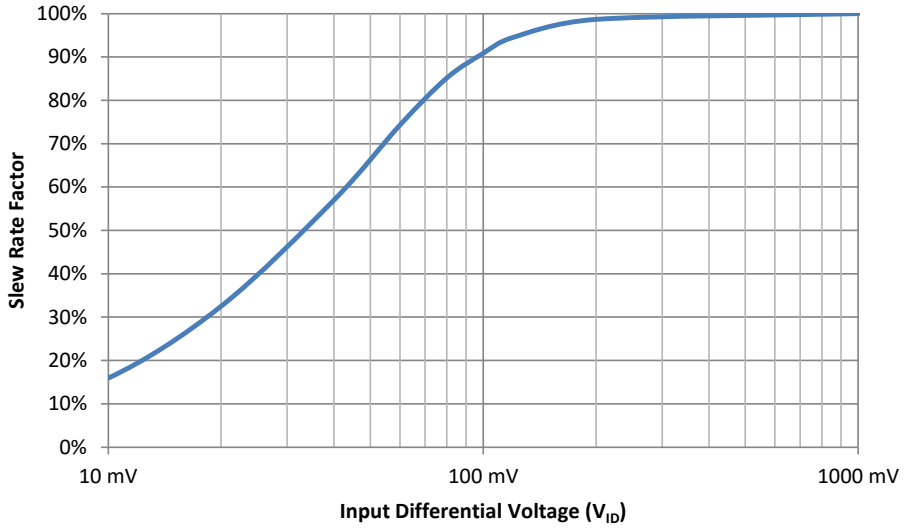

Figure 28. Slew Rate Factor vs Input Differential Voltage (V_{ID})

7 Unused Amp Connections and Inputs Connected Directly to Ground

7.1 Do Not Connect Inputs Directly to Ground

For both used and unused amplifiers, the inputs must not be connected directly to ground or any other low impedance node. Always add some resistance to limit the current to less than 10 mA, regardless of any possible fault condition. All the input pins have a diode from the input to the device's GND, or V–, pin. In dual supply applications, the GND pin will be negative. However, during power up, power down, or supply faults, the GND pin may become positive. If this occurs then a grounded input pin will have potentially damaging current flow due to the input diode. Even if the GND pin is also grounded, such as in single supply applications, there is a possibility that the input ground will be negative relative to the op amp's internal ground node. Ground differences occur when there is poor layout or high current transients, $\Delta i/\Delta t$. Adding 1-kΩ to 10-kΩ series resistors to the input pin is acceptable in most applications.

7.2 Unused Amplifier Connections

Occasionally applications will not need all the amplifiers in a dual or quad package. The unused op amp should be connected in a way that is safe for the unused amplifier and doesn't affect the used amplifiers. The best connection method puts the op amp into the normal linear operation range and no inputs are connected directly to low impedance nodes. The output of the op amp is not a low impedance node. The output by itself cannot provide a harmful voltage and/or current to the input. Therefore, no series resistor is needed between the input and output pins. Figure 29 shows preferred connections for unused amplifiers.

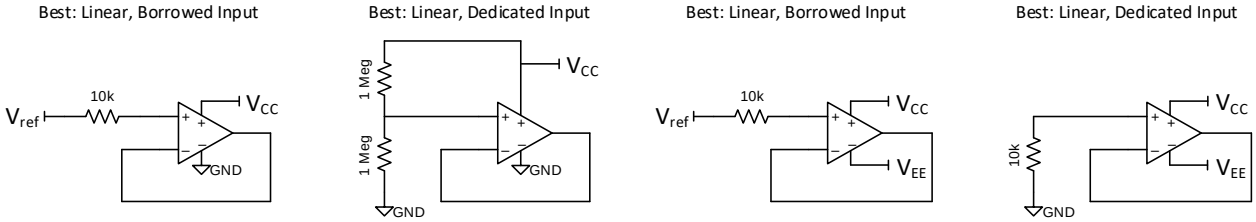

Figure 29. Best Connections Practices for Single and Dual Supplies

Alternatively, the device may be connected in certain, non-linear V_{OH} or V_{OL} configurations, as shown in Figure 30. V_{OL} is preferred over V_{OH} because that provides a small reduction in supply current, I_{CC}. LM358B and LM2904B have slightly lower I_{CC} in the V_{OH} configuration. A soft V_{OL} configuration is sometimes linear if V_{IO} is more positive than 1 mV, but it usually creates a non-linear V_{OL} state. Increasing the input resistor to 10 MΩ would ensure linear operation as the input bias current would raise the non-inverting input voltage beyond the input offset voltage range. "V_{OL} Full V_{ID}" is better suited for lower voltage applications as there is no reason to apply a large input voltage difference even though the op amp allows it. The "V_{OL} (I_{IB} Biased)" method uses the input bias current to raise the voltage on the inverting input. If used, place the 10-MΩ resistor close to the inverting input pin to reduce noise pickup. No inputs may be connected directly to low impedance nodes such as ground, V_{CC} or V_{EE}. V_{OH} alternatives are also acceptable; just swap the input pins. The "soft V_{OL}" connection cannot be input swapped.

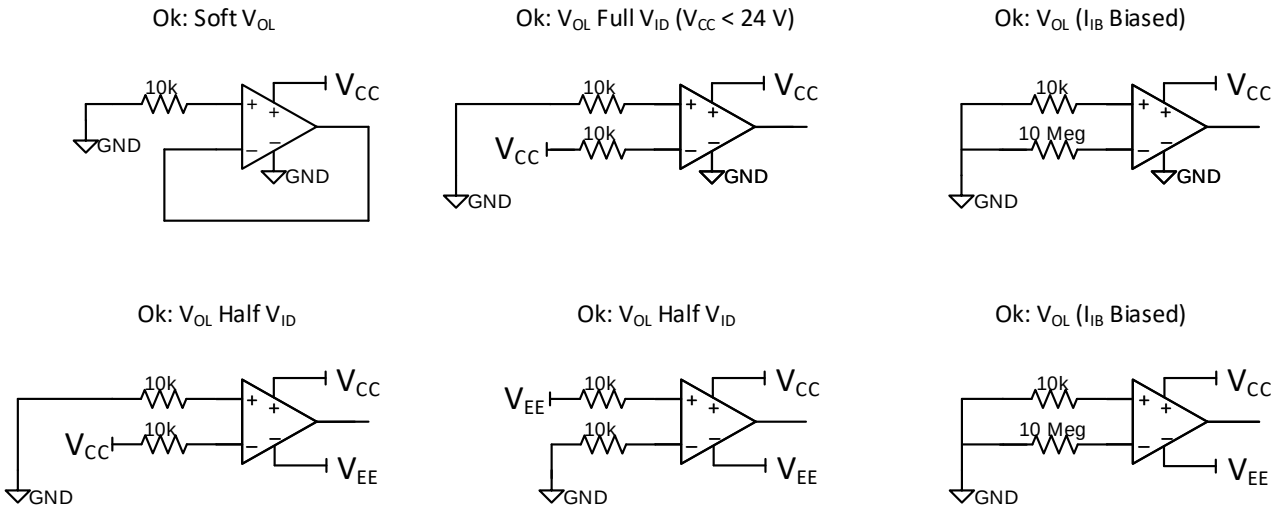

Figure 30. Acceptable Connection Practices for Single and Dual Supplies

The next set of connections in Figure 31 is not recommended, but these configurations are not considered harmful methods of terminating unused channels. The V_{OH} alternatives that swap the inputs are also not recommended methods of terminating unused channels.

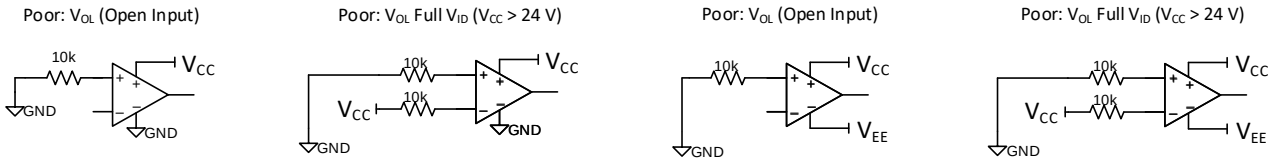

Figure 31. Less Than Acceptable Connection Practices for Single and Dual Supplies

The last set of connections, seen in Figure 32, demonstrates improper setups that could cause output noise chatter or device damage if the GND pin were to ever become positive relative to the input pin.

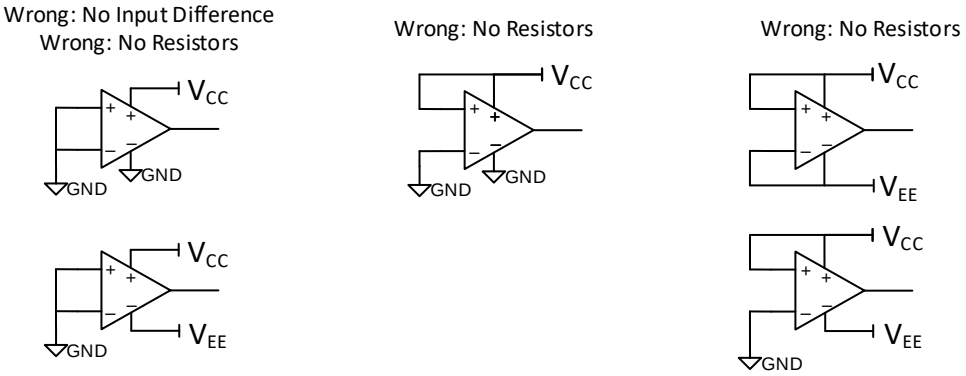

Figure 32. Potentially Harmful Connection Practices for Single and Dual Supplies

8 Conclusion

The LM324, LM358 and their variants are among the most popular, cost effective and long-lived general purpose amplifiers. Using this app note to understand their pros, cons and how they differ from more modern op amps will increase the likelihood of a successful design. Although most analog designers will continue to use these devices, improvements in op amp design, process technology and our understanding of op amp applications over the past four decades have led to the development of better and easier to use op amps.

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