CHAPTER 1: OP AMP BASICS
James Bryant, Walt Jung, Walt Kester

Within Chapter 1, discussions are focused on the basic aspects of op amps. After a brief introductory section, this begins with the fundamental *topology* differences between the two broadest classes of op amps, those using *voltage feedback* and *current feedback*. These two amplifier types are distinguished more by the nature of their internal circuit topologies than anything else. The voltage feedback op amp topology is the classic structure, having been used since the earliest vacuum tube based op amps of the 1940 and 1950's, through the first IC versions of the 1960's, and includes most op amp models produced today. The more recent IC variation of the current feedback amplifier has come into popularity in the mid-to-late 1980's, when higher speed IC op amps were developed. Factors distinguishing these two op amp types are discussed at some length.

Details of op amp input and output *structures* are also covered in this chapter, with emphasis how such factors potentially impact application performance. In some senses, it is logical to categorize op amp types into performance and/or application classes, a process that works to some degree, but not altogether.

In practice, once past those obvious application distinctions such as "high speed" versus "precision," or "single" versus "dual supply," neat categorization breaks down. This is simply the way the analog world works. There is much crossover between various classes, i.e., a high speed op amp can be either single or dual-supply, or it may even fit as a precision type. A low power op amp may be precision, but it need not necessarily be single-supply, and so on. Other distinction categories could include the input stage type, such as FET input (further divided into JFET or MOS, which in turn are further divided into NFET or PFET and PMOS and NMOS, respectively), or bipolar (further divided into NPN or PNP). Then, all of these categories could be further described in terms of the type of input (or output) stage used.

So, it should be obvious that categories of op amps are like an infinite set of analog gray scales; *they don't always fit neatly into pigeonholes, and we shouldn't expect them to*. Nevertheless, it is still very useful to appreciate many of the aspects of op amp design that go into the various structures, as these differences directly influence the optimum op amp choice for an application. Thus structure differences are application drivers, since we choose an op amp to suit the nature of the application, for example single-supply.

In this chapter various op amp performance *specifications* are also discussed, along with those specification differences that occur between the broad distinctions of voltage or current feedback topologies, as well as the more detailed context of individual structures. Obviously, op amp specifications are also application drivers, in fact they are the most important, since they will determine system performance. We choose the best op amp to fit the application, based on for the required bias current, bandwidth, distortion, etc.
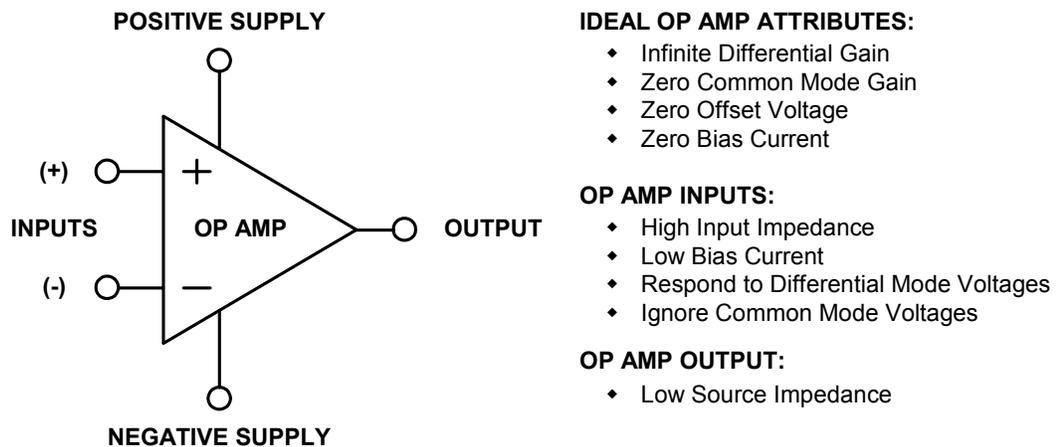
SECTION 1: INTRODUCTION
Walt Jung

As a precursor to more detailed sections following, this introductory chapter portion considers the most basic points of op amp operation. These initial discussions are oriented around the more fundamental levels of op amp applications. They include: *Ideal Op Amp Attributes*, *Standard Op Amp Feedback Hookups, The Non-Ideal Op Amp, Op amp Common Mode Dynamic Range(s),* the various *Functionality Differences of Single and Dual-Supply Operation*, and the *Device Selection* process.

Before op amp applications can be developed, some first requirements are in order. These include an understanding of how the fundamental op amp operating modes differ, and whether dual-supply or single-supply device functionality better suits the system under consideration. Given this, then device selection can begin and an application developed.

POSITIVE SUPPLY

(+)

INPUTS   **OP AMP**   **OUTPUT**

(-)

NEGATIVE SUPPLY

IDEAL OP AMP ATTRIBUTES:
- Infinite Differential Gain
- Zero Common Mode Gain
- Zero Offset Voltage
- Zero Bias Current

OP AMP INPUTS:
- High Input Impedance
- Low Bias Current
- Respond to Differential Mode Voltages
- Ignore Common Mode Voltages

OP AMP OUTPUT:
- Low Source Impedance

Figure 1-1: The ideal op amp and its attributes

First, an *operational amplifier* (hereafter simply op amp) is a differential input, single ended output amplifier, as shown symbolically in Figure 1-1. This device is an amplifier intended for use with *external feedback elements*, where these elements determine the resultant function, or *operation*. This gives rise to the name "operational amplifier," denoting an amplifier that, by virtue of different feedback hookups, can perform a variety of operations.[1] At this point, note that there is no need for concern with any actual technology to implement the amplifier. Attention is focused more on the behavioral nature of this building block device.

An op amp processes small, differential mode signals appearing between its two inputs, developing a single ended output signal referred to a power supply common terminal. Summaries of the various ideal op amp attributes are given in the figure. While real op amps will depart from these ideal attributes, it is very helpful for first-level understanding of op amp behavior to consider these features. Further, although these initial discussions

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[1] The actual *naming* of the operational amplifier occurred in the classic Ragazinni, et al paper of 1947 (see Reference 1). However analog computations using op amps as we know them today began with the work of the Clarence Lovell led group at Bell Labs, around 1940 (acknowledged generally in the Ragazinni paper).

talk in idealistic terms, they are also flavored by pointed mention of typical "real world" specifications— for a beginning perspective.

It is also worth noting that this op amp is shown with five terminals, a number that happens to be a minimum for real devices. While some single op amps may have more than five terminals (to support such functions as frequency compensation, for example), none will ever have less. By contrast, those elusive ideal op amps don't require power, and symbolically function with just four pins. [1]

Ideal Op Amp Attributes

An ideal op amp has infinite gain for *differential* input signals. In practice, real devices will have quite high gain (also called *open-loop gain*) but this gain won't necessarily be precisely known. In terms of specifications, gain is measured in terms of V_{OUT}/V_{IN}, and is given in V/V, the dimensionless numeric gain. More often however, gain is expressed in decibel terms (dB), which is mathematically dB = 20 • log (numeric gain). For example, a numeric gain of 1 million (10^6 V/V) is equivalent to a 120 dB gain. Gains of 100-130 dB are common for precision op amps, while high speed devices may have gains in the 60-70 dB range.

Also, an ideal op amp has zero gain for signals *common* to both inputs, that is, *common mode* (CM) signals. Or, stated in terms of the rejection for these common mode signals, an ideal op amp has infinite *CM rejection* (CMR). In practice, real op amps can have CMR specifications of up to 130 dB for precision devices, or as low as 60-70 dB for some high speed devices.

The ideal op amp also has zero *offset voltage* (V_{OS}=0), and draws zero *bias current* (I_B=0) at both inputs. Within real devices, actual offset voltages can be as low as a μV or less, or as high as several mV. Bias currents can be as low as a few fA, or as high as several μA. This extremely wide range of specifications reflects the different input structures used within various devices, and is covered in more detail later in this chapter.

The attribute headings within Figure 1-1 for INPUTS and OUTPUT summarize the above concepts in more succinct terms. In practical terms, another important attribute is the concept of *low source impedance*, at the output. As will be seen later, low source impedance enables higher useful gain levels within circuits.

To summarize these idealized attributes for a signal-processing amplifier, some of the traits might at first seem strange. However, it is critically important to reiterate that op amps simply are never intended for use without overall feedback! In fact, as noted, the connection of a suitable *external* feedback loop defines the *closed-loop* amplifier's gain and frequency response characteristics.

Note also that all real op amps have a positive and negative power supply terminal, but rarely (if ever) will they have a separate ground connection. In practice, the op amp

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[1] Such an op amp generates its own power, has two input pins, an output pin, and an output common pin.

output voltage becomes referred to a power supply common point. *Note: This key point is further clarified with the consideration of typically used op amp feedback networks.*

The basic op amp hookup of Figure 1-2 below applies a signal to the (+) input, and a (generalized) network delivers a fraction of the output voltage to the (−) input terminal. This constitutes *feedback*, with the op amp operating in *closed-loop* fashion. The feedback network (shown here in general form) can be resistive or reactive, linear or non-linear, or any combination of these. More detailed analysis will show that the circuit gain characteristic as a whole follows the inverse of the feedback network transfer function.
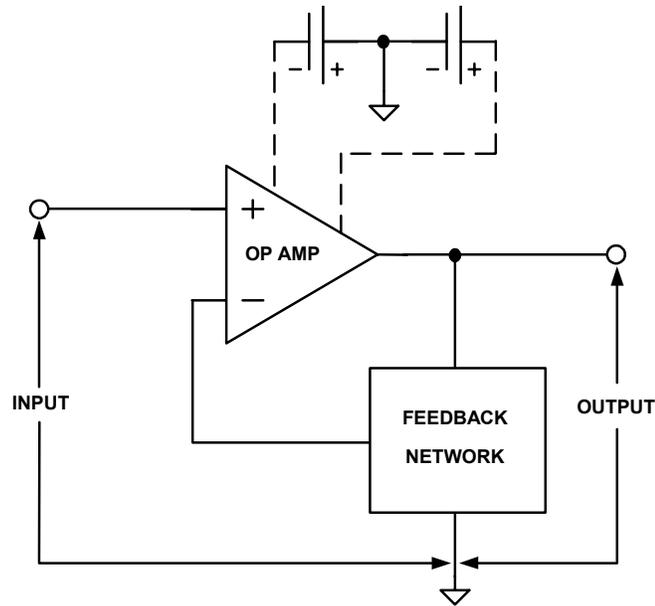
Figure 1-2: *A generalized op amp circuit with feedback applied*

The concept of feedback is both an essential and salient point concerning op amp use. With feedback, the net closed-loop gain characteristics of a stage such as Fig. 1-2 become primarily dependent upon a set of *external components* (usually passive). Thus behavior is less dependent upon the relatively unstable amplifier open-loop characteristics.

Note that within Figure 1-2, the input signal is applied between the op amp (+) input and a *common or reference point*, as denoted by the ground symbol. It is important to note that this reference point is also common to the output and feedback network. By definition, the op amp stage's output signal appears between the output terminal/feedback network input, and this common ground. This single relevant fact answers the "Where is the op amp grounded?" question so often asked by those new to the craft. The answer is simply that it is grounded *indirectly*, by virtue of the commonality of its input, the feedback network, and the power supply, as is shown within Fig. 1-2.

To emphasize how the input/output signals are referenced to the power supply, dual supply connections are shown dotted, with the ± power supply midpoint common to the input/output signal ground. But do note, while all op amp application circuits may not show full details of the power supply connections, every *real* circuit will always use power supplies!

Standard Op Amp Feedback Hookups

Virtually all op amp feedback connections can be categorized into just a few basic types. These include the two most often used, *non-inverting* and *inverting* voltage gain stages, plus a related *differential* gain stage. Having discussed above just the attributes of the ideal op amp, at this point it is possible to conceptually build basic gain stages. Using the concepts of infinite gain, zero input offset voltage, zero bias current, etc., standard op amp feedback hookups can be devised. For brevity, a full mathematical development of these concepts isn't included below (but this follows in a subsequent section). The end-of-section references also include such developments.

The Non-inverting Op Amp Stage

The op amp non-inverting gain stage, also known as a *voltage follower with gain*, or simply *voltage follower*, is shown below in Figure 1-3.
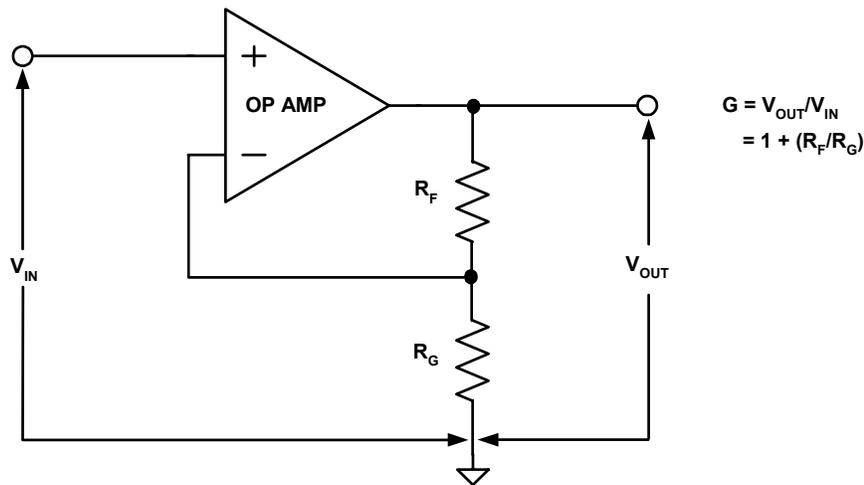
Figure 1-3: *The non-inverting op amp stage (voltage follower)*

This op amp stage processes the input V_{IN} by a gain of G, so a generalized expression for gain is:

$$G = \frac{V_{OUT}}{V_{IN}}$$

<div align="right">Eq. 1-1</div>

Feedback network resistances R_F and R_G set the stage gain of the follower. For an ideal op amp, the gain of this stage is:

$$G = \frac{R_F + R_G}{R_G}$$

<div align="right">Eq. 1-2</div>

For clarity, these expressions are also included in the figure. Comparison of this figure and the more general Figure 1-2 shows R_F and R_G here as a simple feedback network, returning a fraction of V_{OUT} to the op amp (−) input *(note that some texts may show the more general symbols Z_F and Z_G for these feedback components— both are correct, depending upon the specific circumstances).*

In fact, we can make some useful general points about the network $R_F - R_G$. We will define the transfer expression of the network as seen from the top of R_F to the output across R_G as β. Note that this usage is a general feedback network transfer term, *not* to be confused with bipolar transistor forward gain. β can be expressed mathematically as:

$$\beta = \frac{R_G}{R_F + R_G}$$

Eq. 1-3

So, the feedback network returns a fraction of V_{OUT} to the op amp (–) input. Considering the ideal principles of zero offset and infinite gain, this allows some deductions on gain to be made. The voltage at the (–) input is forced by the op amp's feedback action to be equal to that seen at the (+) input, V_{IN}. Given this relationship, it is relatively easy to work out the ideal gain of this stage, which in fact turns out to be simply the inverse of β. This is apparent from a comparison of equations 1-2 and 1-3.

Thus an ideal non-inverting op amp stage gain is simply equal to $1/\beta$, or:

$$G = \frac{1}{\beta}$$

Eq. 1-4

This non-inverting gain configuration is one of the most useful of all op amp stages, for several reasons. Because V_{IN} sees the op amp's high impedance (+) input, it provides an ideal interface to the driving source. Gain can easily be adjusted over a wide range via R_F and R_G, with virtually no source interaction.

A key point is the interesting relationship concerning R_F and R_G. Note that to satisfy the conditions of Equation 1-2, only their *ratio* is of concern. In practice this means that stable gain conditions can exist over a range of actual $R_F - R_G$ values, so long as they provide the same ratio.

If R_F is taken to zero and R_G open, the stage gain becomes unity, and V_{OUT} is then exactly equal to V_{IN}. This special non-inverting gain case is also called a *unity gain follower*, a stage commonly used for buffering a source.

Note that this op amp example shows only a simple resistive case of feedback. As mentioned, the feedback can also be reactive, i.e., Z_F, to include capacitors and/or inductors. In all cases however, it must include a DC path, if we are to assume the op amp is being biased by the feedback (which is usually the case).

To summarize some key points on op amp feedback stages, we paraphrase from Reference 2 the following statements, which will always be found useful:

> *The* summing point *idiom is probably the most used phrase of the aspiring analog artificer, yet the least appreciated. In general, the inverting (–) input is called the* summing point, *while the non-inverting (+) input is represented as the* reference terminal. *However, a vital concept is the fact that, within linear op amp applications,* the inverting input (or summing point) assumes the same absolute potential as the non-inverting input or reference (within the gain error of the amplifier). *In short, the amplifier tries to servo its own summing point to the reference.*
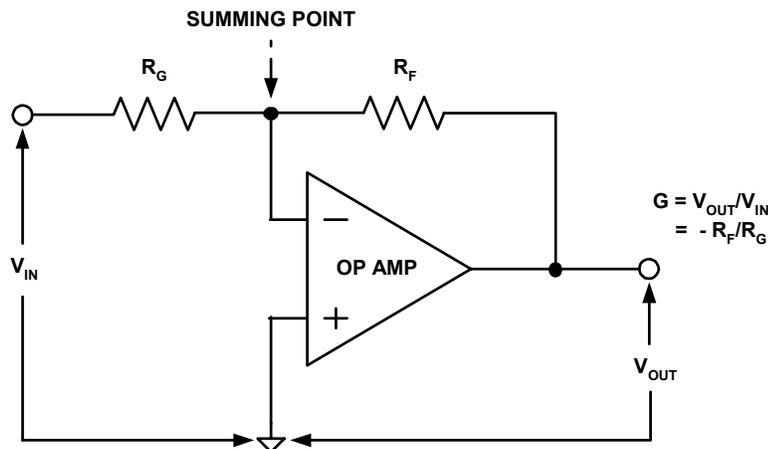
The Inverting Op Amp Stage

The op amp inverting gain stage, also known simply as the *inverter*, is shown in Figure 1-4. As can be noted by comparison of Figures 1-3 and 1-4, the inverter can be viewed as similar to a follower, but with a transposition of the input voltage V_{IN}. In the inverter the signal is applied to R_G of the feedback network, and the op amp (+) input is grounded.

The feedback network resistances, R_F and R_G set the stage gain of the inverter. For an ideal op amp, the gain of this stage is:

$$G = -\frac{R_F}{R_G}$$

Eq. 1-5

For clarity, these expressions are again included in the figure. Note that a major difference between this stage and the non-inverting counterpart is the input-to-output sign reversal, denoted by the minus sign in Equation 1-5. Like the follower stage, applying ideal op amp principles and some basic algebra can derive the gain expression of Eq. 1-5.

Figure 1-4: The inverting op amp stage (inverter)

The inverting configuration is also one of the more useful op amp stages. Unlike a non-inverting stage however, the inverter presents a relatively low impedance input for V_{IN}, i.e., the value of R_G. This factor provides a finite load to the source. While the stage gain can in theory be adjusted over a wide range via R_F and R_G, there is a practical limitation imposed at high gain, when R_G becomes relatively low. If R_F is zero, the gain becomes zero. R_F can also be made variable, in which case the gain is linearly variable over the dynamic range of the element used for R_F. As with the follower gain stage, the gain is ratio dependent, and is relatively insensitive to the exact R_F and R_G values.

The inverter's gain behavior, due to the principles of infinite op amp gain, zero input offset, and zero bias current, gives rise to an effective node of zero voltage at the (−) input. The input and feedback currents sum at this point, which logically results in the term *summing point*. It is also called a *virtual ground*, because of the fact it will be at the same potential as the grounded reference input.

Note that, technically speaking, *all* op amp feedback circuits have a summing point, whether they are inverters, followers, or a hybrid combination. The summing point is always the feedback junction at the (–) input node, as shown in Fig. 1-4. However in follower type circuits this point isn't a virtual ground, since it follows the (+) input.

A special gain case for the inverter occurs when $R_F = R_G$, which is also called a *unity gain inverter*. This form of inverter is commonly used for generating complementary V_{OUT} signals, i.e., $V_{OUT} = -V_{IN}$. In such cases it is usually desirable to match R_F to R_G accurately, which can readily be done by using a well-specified matched resistor pair.

A variation of the inverter is the *inverting summer*, a case similar to Figure 1-4, but with input resistors R_{G2}, R_{G3}, etc (not shown). For a summer individual input resistors are connected to additional sources V_{IN2}, V_{IN3}, etc., with their common node connected to the summing point. This configuration, called a *summing amplifier*, allows linear input current summation in R_F.[1] V_{OUT} is proportional to an inverse sum of input currents.

The Differential Op Amp Stage

The op amp differential gain stage (also known as a *differential amplifier*, or *subtractor*) is shown in Figure 1-5.
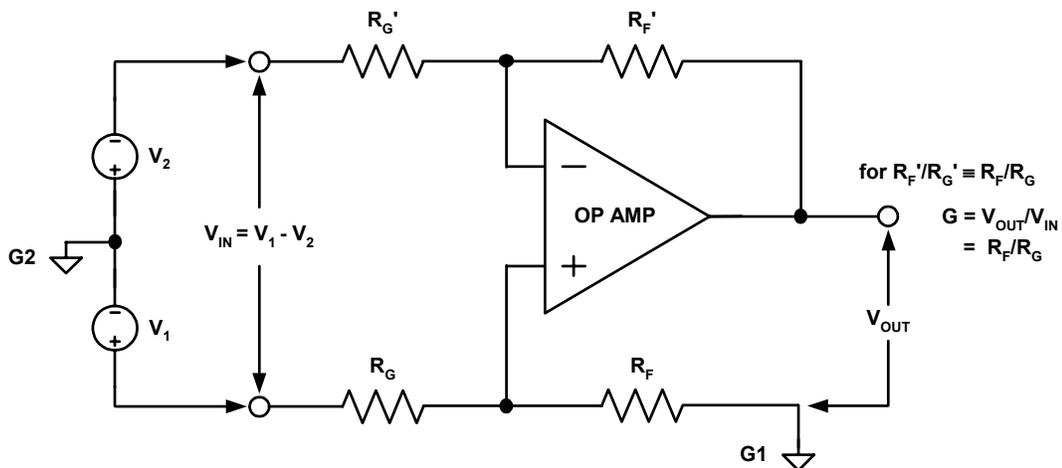
Figure 1-5: The differential amplifier stage (subtractor)

Paired input and feedback network resistances set the gain of this stage. These resistors, $R_F - R_G$ and $R_F' - R_G'$, *must be matched as noted,* for proper operation. Calculation of individual gains for inputs V_1 and V_2 and their linear combination derives the stage gain.

Note that the stage is intended to amplify the *difference* of voltages V_1 and V_2, so the net input is $V_{IN} = V_1 - V_2$. The general gain expression is then:

$$G = \frac{V_{OUT}}{V_1 - V_2}$$

Eq. 1-6

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[1] The very first general-purpose op amp circuit is described by Karl Swartzel in Reference 3, and is titled "Summing Amplifier". This amplifier became a basic building block of the M9 gun director computer and fire control system used by Allied Forces in World War II. It also influenced many vacuum tube op amp designs that followed over the next two decades.

For an ideal op amp and the resistor ratios matched as noted, the gain of this differential stage from V_{IN} to V_{OUT} is:

$$G = \frac{R_F}{R_G}$$

Eq. 1-7

The great fundamental utility that an op amp stage such as this allows is the property of rejecting voltages *common* to V_1-V_2, i.e., common-mode (CM) voltages. For example, if noise voltages appear between grounds G1 and G2, the noise will be suppressed by the common-mode rejection (CMR) of the differential amp. The CMR is however only as good as the matching of the resistor ratios allows, so in practical terms it implies precisely trimmed resistor ratios are necessary. Another disadvantage of this stage is that the resistor networks load the V_1-V_2 sources, potentially leading to additional errors.

The Non-Ideal Op Amp— Static Errors Due to Finite Amplifier Gain

One of the most distinguishing features of op amps is their staggering magnitude of DC voltage gain. Even the least expensive devices have typical voltage gains of 100,000 (100dB), while the highest performance precision bipolar and chopper stabilized units can have gains as high 10,000,000 (140dB), or more. Negative feedback applied around this much voltage gain readily accomplishes the virtues of closed-loop performance, making the circuit dependent only on the feedback components.
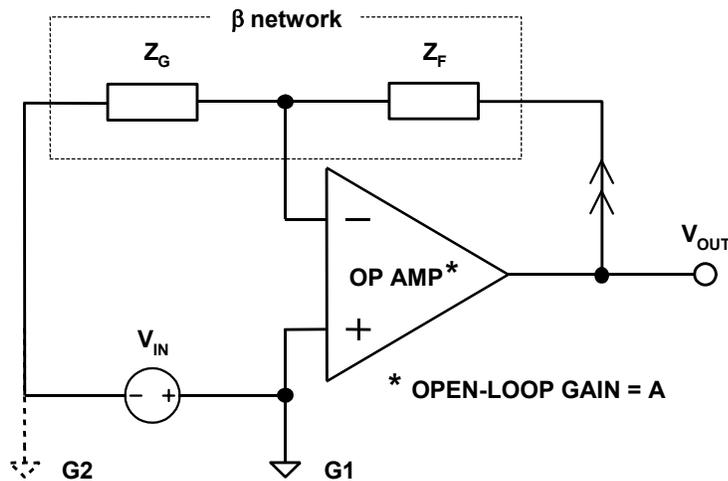
Figure 1-6: Non-ideal op amp stage for gain error analysis

As noted above in the discussion of ideal op amp attributes, the behavioral assumptions follow from the fact that negative feedback, coupled with high open-loop gain, constrains the amplifier input error voltage (and consequently the error current) to infinitesimal values. The higher this gain, the more valid these assumptions become.

But in reality, op amps *do* have finite gain, and errors exist in practical circuits. The op amp gain stage of Figure 1-6 will be used to illustrate how these errors impact performance. In this circuit the op amp is ideal except for the finite open-loop DC voltage gain, A, which is usually stated as A_{VOL}.

Noise Gain (NG)

The first aid to analyzing op amps circuits is to differentiate between *noise gain* and *signal gain*. We have already discussed the differences between non-inverting and inverting stages as to their signal gains, which are summarized in Equations 1-2 and 1-4, respectively. But, as can be noticed from Fig. 1-6, the difference between an inverting and non-inverting stage can be as simple as just where the reference ground is placed. For a ground at point G1, the stage is an inverter; conversely, if the ground is placed at point G2 (with no G1) the stage is non-inverting.

Note however that in terms of the feedback path, *there are no real differences*. To make things more general, the resistive feedback components previously shown are replaced here with the more general symbols Z_F and Z_G, otherwise they function as before. The feedback attenuation, β, is the same for both the inverting and non-inverting stages:

$$\beta = \frac{Z_G}{Z_{G+}Z_F}$$

Eq. 1-8

Noise gain can now be simply defined as: *The inverse of the net feedback attenuation from the amplifier output to the feedback input*. In other words, the inverse of the β network transfer function. This can ultimately be extended to include frequency dependence (covered later in this chapter). Noise gain can be abbreviated as NG.

As noted, the inverse of β is the ideal non-inverting op amp stage gain. Including the effects of finite op amp gain, a modified gain expression for the non-inverting stage is:

$$G_{CL} = \frac{1}{\beta} \bullet \left[\frac{1}{1 + \frac{1}{A_{VOL}\beta}} \right]$$

Eq. 1-9

where G_{CL} is the finite-gain stage's closed-loop gain, and A_{VOL} is the op amp open-loop voltage gain for loaded conditions.

It is important to note that this expression is identical to the ideal gain expression of Eq. 1-4, with the addition of the bracketed multiplier on the right side. Note also that this right-most term becomes closer and closer to unity, as A_{VOL} approaches infinity. Accordingly, it is known in some textbooks as the *error multiplier* term, when the expression is shown in this form. [1]

It may seem logical here to develop another finite gain error expression for an inverting amplifier, but in actuality there is no need. Both inverting and non-inverting gain stages have a common feedback basis, which is the noise gain. So Eq. 1-9 will suffice for gain error analysis for both stages. Simply use the β factor as it applies to the specific case.

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[1] Some early discussions of this finite gain error appear in References 4 and 5. Terman uses the open-loop gain symbol of A, as we do today. West uses Harold Black's original notation of μ for open-loop gain. The form of Eq. 1-9 is identical to Terman's (or to West's, substituting μ for A).

It is useful to note some assumptions associated with the rightmost error multiplier term of Eq. 1-9. For $A_{VOL}\beta \gg 1$, one assumption is:

$$\frac{1}{1 + \dfrac{1}{A_{VOL}\beta}} \approx 1 - \frac{1}{A_{VOL}\beta} \qquad \text{Eq. 1-10}$$

This in turn leads to an estimation of the percentage error, ε, due to finite gain A_{VOL}:

$$\varepsilon(\%) \approx \frac{100}{A_{VOL}\beta} \qquad \text{Eq. 1-11}$$

Gain Stability

The closed-loop gain error predicted by these equations isn't in itself tremendously important, since the ratio Z_F/Z_G could always be adjusted to compensate for this error. But note however that closed-loop gain *stability* is a very important consideration in most applications. Closed-loop gain instability is produced primarily by variations in open-loop gain due to changes in temperature, loading, etc.

$$\frac{\Delta G_{CL}}{G_{CL}} \approx \frac{\Delta A_{VOL}}{A_{VOL}} \bullet \frac{1}{A_{VOL}\beta} \qquad \text{Eq. 1-12}$$

From Eq. 1-12, any variation in open-loop gain (ΔA_{VOL}) is reduced by the factor $A_{VOL}\beta$, insofar as the effect on closed-loop gain. This improvement in closed-loop gain stability is one of the important benefits of negative feedback.

Loop gain

The product $A_{VOL}\beta$ which occurs in the above equations, is called *loop gain*, a well-known term in feedback theory. The improvement in closed-loop performance due to negative feedback is, in nearly every case, proportional to loop gain.

The term "loop gain" comes from the method of measurement. This is done by breaking the closed feedback loop at the op amp output, and measuring the total gain around the loop. In Fig. 1-6 for example, this could be done between the amplifier output and the feedback path (see arrows). Approximately, closed-loop output impedance, linearity, and gain instability errors reduce by the factor $A_{VOL}\beta$, with the use of negative feedback.

Another useful approximation is developed as follows. A rearrangement of Eq. 1-9 is:

$$\frac{A_{VOL}}{G_{CL}} = 1 + A_{VOL}\beta \qquad \text{Eq. 1-13}$$

So, for high values of $A_{VOL}\beta$,

$$\frac{A_{VOL}}{G_{CL}} \approx A_{VOL}\beta \qquad \text{Eq. 1-14}$$

Consequently, in a given feedback circuit the loop gain, $A_{VOL}\beta$, is approximately the numeric ratio (or difference, in dB) of the amplifier open-loop gain to the circuit closed-loop gain.

This loop gain discussion emphasizes that indeed, loop gain is a very significant factor in predicting the performance of closed-loop operational amplifier circuits. The open-loop gain required to obtain an adequate amount of loop gain will, of course, depend on the desired closed-loop gain.

For example, using Equation 1-14, an amplifier with A_{VOL} = 20,000 will have an $A_{VOL}\beta$ ≈ 2000 for a closed-loop gain of 10, but the loop gain will be only 20 for a closed-loop gain of 1000. The first situation implies an amplifier-related gain error the order of ≈0.05%, while the second would result in about 5% error. Obviously, the higher the required gain, the greater will be the required open-loop gain to support an $A_{VOL}\beta$ for a given accuracy.

Frequency Dependence of Loop Gain

Thus far, it has been assumed that amplifier open-loop gain is independent of frequency. Unfortunately, this isn't the case at all. Leaving the discussion of the effect of open-loop response on bandwidth and dynamic errors until later, let us now investigate the general effect of frequency response on loop gain and static errors.
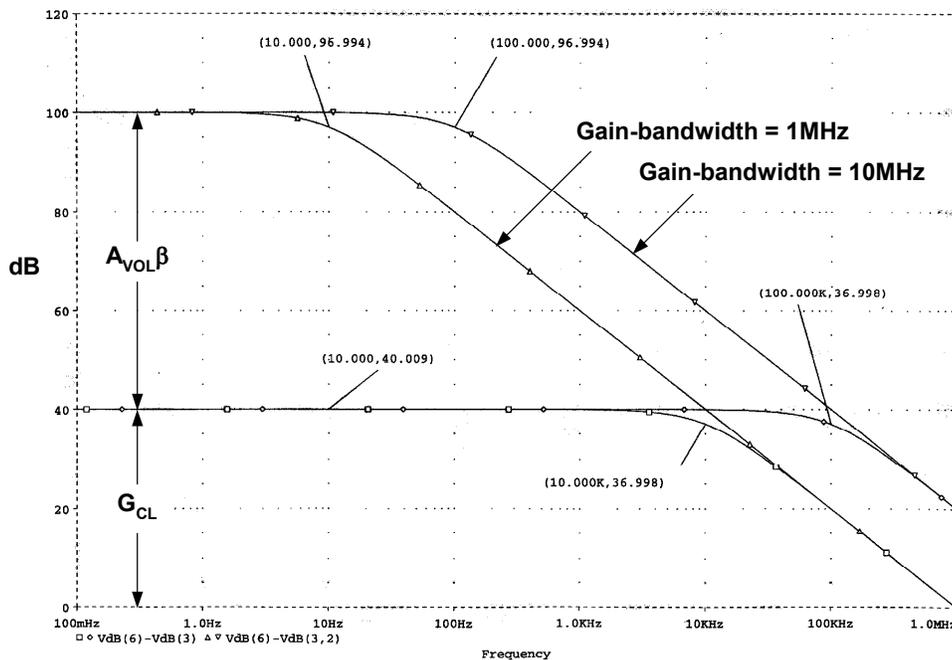
Figure 1-7: *Op amp closed-loop gain and loop gain interactions with typical open-loop responses*

The open-loop frequency response for a typical operational amplifier with superimposed closed-loop amplifier response for a gain of 100 (40dB), illustrates graphically these results, in Figure 1-7. In these Bode plots, subtraction on a logarithmic scale is equivalent

to normal division of numeric data. [1] Today, op amp open-loop gain and loop gain parameters are typically given in dB terms, thus this display method is convenient.

A few key points evolve from this graphic figure, which is a simulation involving two hypothetical op amps, both with a DC/low frequency gain of 100dB (100kV/V). The first has a gain-bandwidth of 1MHz, while the gain-bandwidth of the second is 10MHz.

- The open-loop gain A_{VOL} for the two op amps is noted by the two curves marked 1 and 10MHz, respectively. Note that each has a −3dB corner frequency associated with it, above which the open-loop gain falls at 6dB/octave. These corner frequencies are marked at 10 and 100Hz, respectively, for the two op amps.

- At any frequency on the open-loop gain curve, the numeric product of gain A_{VOL} and frequency, f, is a constant (10,000V/V at 100Hz equates to 1MHz). This, by definition, is characteristic of a constant gain-bandwidth product amplifier. All *voltage feedback* op amps behave in this manner.

- $A_{VOL}\beta$ in dB is the difference between open-loop gain and closed-loop gain, as plotted on log-log scales. At the lower frequency point marked, $A_{VOL}\beta$ is thus 60dB.

- $A_{VOL}\beta$ decreases with increasing frequency, due to the decrease of A_{VOL} above the open-loop corner frequency. At 100Hz for example, the 1MHz gain-bandwidth amplifier shows an $A_{VOL}\beta$ of only 80–40 = 40dB.

- $A_{VOL}\beta$ also decreases for higher values of closed-loop gain. Other, higher closed-loop gain examples (not shown) would decrease $A_{VOL}\beta$ to less than 60dB at low frequencies.

- G_{CL} depends primarily on the ratio of the feedback components, Z_F and Z_G, and is relatively independent of A_{VOL} (apart from the errors discussed above, which are inversely proportional to $A_{VOL}\beta$). In this example 1/β is 100, or 40dB, and is so marked at 10Hz. Note that G_{CL} is flat with increasing frequency, up until that frequency where G_{CL} intersects the open-loop gain curve, and $A_{VOL}\beta$ drops to zero.

- At this point where the closed-loop and open-loop curves intersect, the loop gain is by definition zero, which implies that beyond this point there is no negative feedback. Consequently, closed-loop gain is equal to open-loop gain for further increases in frequency.

- Note that the 10MHz gain-bandwidth op amp allows a 10× increase in closed-loop bandwidth, as can be noted from the −3dB frequencies; that is 100kHz versus 10kHz for the 10MHz versus the 1MHz gain-bandwidth op amp.

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[1] The log-log displays of amplifier gain (and phase) versus frequency are called *Bode* plots. This graphic technique for display of feedback amplifier characteristics, plus definitions for feedback amplifier stability were pioneered by Hendrick W. Bode of Bell Labs (see Reference 6).

Fig. 1-7 illustrates that the high open-loop gain figures typically quoted for op amps can be somewhat misleading. As noted, beyond a few Hz, the open-loop gain falls at 6dB/octave. Consequently, closed-loop gain stability, output impedance, linearity and other parameters dependent upon loop gain are degraded at higher frequencies. One of the reasons for having DC gain as high as 100dB and bandwidth as wide as several MHz, is to obtain adequate loop gain at frequencies even as low as 100Hz.

A direct approach to improving loop gain at high frequencies other than by increasing open-loop gain is to increase the amplifier open-loop bandwidth. Figure 1-7 shows this in terms of two simple examples. It should be borne in mind however that op amp gain-bandwidths available today extend to the hundreds of MHz, allowing video and high-speed communications circuits to fully exploit the virtues of feedback.

Op amp Common Mode Dynamic Range(s)

As a point of departure from the idealized circuits above, some practical basic points are now considered. Among the most evident of these is the allowable input and output dynamic ranges afforded in a real op amp. This obviously varies with not only the specific device, but also the supply voltage. While we can always optimize this performance point with device selection, more fundamental considerations come first.
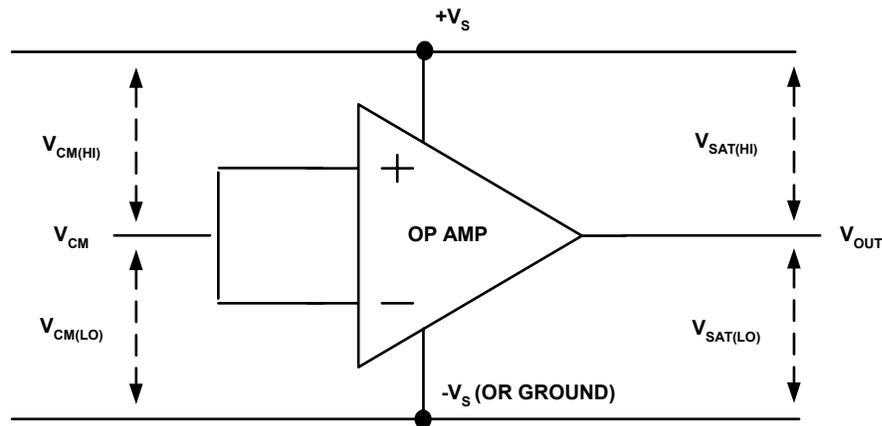
Figure 1-8: Op amp input and output common mode ranges

Any real op amp will have a finite voltage range of operation, at both input and output. In modern system designs, supply voltages are dropping rapidly, and 3-5V total supply voltages are now common. This is a far cry from supply systems of the past, which were typically ±15V (30V total). Obviously, if designs are to accommodate a 3-5V supply, careful consideration must be given to maximizing dynamic range, by choosing a correct device. Choosing a device will be in terms of exact specifications, but first and foremost it should be in terms of the basic topologies used within it.

Output Dynamic Range

Figure 1-8 above is a general illustration of the limitations imposed by input and output dynamic ranges of an op amp, related to both supply rails. Any op amp will always be powered by two supply potentials, indicated by the positive rail, $+V_S$, and the negative

rail, -V_S. We will define the op amp's input and output CM range in terms of how closely it can approach these two rail voltage limits.

At the output, V_{OUT} has two rail-imposed limits, one high or close to +V_S, and one low, or close to $-V_S$. Going high, it can range from an upper saturation limit of +$V_S - V_{SAT(HI)}$ as a positive maximum. For example if +V_S is 5V, and $V_{SAT(HI)}$ is 100mV, the upper V_{OUT} limit or positive maximum is 4.9V. Similarly, going low it can range from a lower saturation limit of $-V_S + V_{SAT(LO)}$. So, if $-V_S$ is ground (0V) and $V_{SAT(LO)}$ is 50mV, the lower limit of V_{OUT} is simply 50mV.

Obviously, the internal design of a given op amp will impact this output CM dynamic range, since, when so necessary, the device itself must be designed to minimize both $V_{SAT(HI)}$ and $V_{SAT(LO)}$, so as to maximize the output dynamic range. Certain types of op amp structures are so designed, and these are generally associated with designs expressly for *single-supply* systems. This is covered in detail later within the chapter.

Input Dynamic Range

At the input, the CM range useful for V_{IN} also has two rail-imposed limits, one high or close to +V_S, and one low, or close to $-V_S$. Going high, it can range from an upper CM limit of +V_S - $V_{CM(HI)}$ as a positive maximum. For example, again using the +V_S = 5V example case, if $V_{CM(HI)}$ is 1V, the upper V_{IN} limit or positive CM maximum is +V_S − $V_{CM(HI)}$, or 4V.
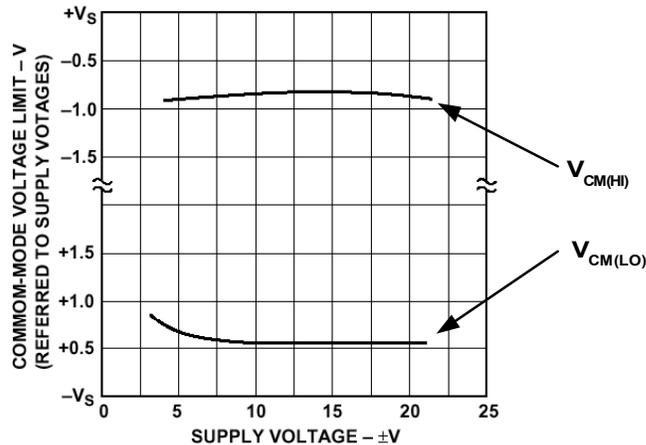
Figure 1-9: A graphical display of op amp input common mode range

Figure 1-9 above illustrates by way of a hypothetical op amp's data how $V_{CM(HI)}$ could be specified, as shown in the upper curve. This particular op amp would operate for V_{CM} inputs *lower* than the curve shown.

In practice the input CM range of real op amps is typically specified as a *range of voltages*, not necessarily referenced to +V_S or -V_S. For example, a typical ±15V operated dual supply op amp would be specified for an operating CM range of ±13V. Going low, there will also be a lower CM limit. This can be generally expressed as -V_S + $V_{CM(LO)}$, which would appear in a graph such as Fig. 1-9 as the lower curve, for $V_{CM(LO)}$. If this were again a ±15V part, this could represent typical performance.

1.16

To use a single-supply example, for the $-V_S = 0V$ case, if $V_{CM(LO)}$ is 100mV, the lower CM limit will be 0V + 0.1V, or simply 0.1V. Although this example illustrates a lower CM range within 100mV of $-V_S$, it is actually much more typical to see single-supply devices with lower or upper CM ranges, which *include* the supply rail.

In other words, $V_{CM(LO)}$ or $V_{CM(HI)}$ is 0V. There are also single-supply devices with CM ranges that include *both* rails. More often than not however, single-supply devices will not offer graphical data such as Fig. 1-9 for CM limits, but will simply cover performance with a tabular range of specified voltage.

Functionality Differences of Dual-Supply and Single-Supply Devices

There are two major classes of op amps, the choice of which determines how well the selected part will function in a given system. Traditionally, many op amps have been designed to operate on a dual power supply system, which has typically been ±15V. This custom has been prevalent since the earliest IC op amps days, dating back to the mid-sixties. Such devices can accommodate input/output ranges of ±10V (or slightly more), but when operated on supplies of appreciably lower voltage, for example ±5V or less, they suffer either loss of performance, or simply don't operate at all. This type of device is referenced here as a *dual-supply* op amp design. This moniker indicates that it performs optimally on dual voltage systems only, typically ±15V. It may or may not also work at appreciably lower voltages.

PERFORMANCE PARAMETER	DUAL SUPPLY	SINGLE SUPPLY
♦ SUPPLY LIMITATIONS	Best >10V, Limited <10V	Best <10V, Limited >10V
♦ OUTPUT V RANGE	- Limited	+ Greatest
♦ INPUT V RANGE	- Limited	+ Greatest
♦ TOTAL DYNAMIC RANGE	+ Greatest	- Least
♦ V & I OUTPUT	+ Greater	- Less
♦ PRECISION	+ Greatest	- Less (growing)
♦ LOAD IMMUNITY	+ Greatest	- Least
♦ VARIETY AVAILABLE	+ Greater	- Less (growing)

Figure 1-10: Comparison of relative functional performance differences between single and dual-supply op amps

Figure 1-10 above illustrates in a broad overview the relative functional performance differences that distinguish the dual-supply vs. single-supply op amp classes. This table is arranged to illustrate various general performance parameters, with an emphasis on the contrast between single and dual-supply devices. Which particular performance area is more critical will determine what type of device will be the better system choice.

More recently, with increasing design attention to lower overall system power and the use of single rail power, the single-supply op amp has come into vogue. This has not been without good reason, as the virtues of using single supply rails can be quite compelling. A review of Fig. 1-10 illustrates key points of the dual vs. single supply op amp question.

In terms of *supply voltage limitations*, there is a crossover region in terms of overall utility, which occurs around 10V of total supply voltage.

For example, single-supply devices tend to excel in terms of their *input and output voltage dynamic ranges*. Note that in Figure 1-10 a maximum range is stated as a % of available supply. Single-supply parts operate better in this regard, because they are internally designed to maximize these respective ranges. For example, it is not unusual for a device operating from 5V to swing 4.8V at the output, and so on.

But, rather interestingly, such devices are also usually restricted to lower supply ranges (only), so their upper dynamic range in absolute terms is actually more limited. For example, a traditional ±15V dual-supply device can typically swing 20Vp-p, or more than four times that of a 5V single-supply part. If the *total dynamic range* is considered (assuming an identical input noise), the dual-supply operated part will have 4 times (or 12 dB) greater dynamic range than that of the 5V operated part. Or, stated in another way, the input errors of a real part such as noise, drift etc., become 4 times more critical (relatively speaking), when the output dynamic range is reduced by a factor of 4. Note that these comparisons do not involve any actual device specifications, *they are simply system-based observations*. Device specifications are covered later in this chapter.

In terms of total *voltage and current output*, dual-supply parts tend to offer more in absolute terms, since single-supply parts usually are usually designed not just for low operating voltage ranges, but also more modest current outputs.

In terms of *precision*, the dual-supply op amp has been long favored by designers for highest overall precision. However, this status quo is now beginning to be challenged, by such single-supply parts as the truly excellent chopper-stabilized op amps. With more and more new op amps being designed for single-supply use, high precision is likely to become an ever-increasing strength of this category.

Load immunity is often an application problem with single-supply parts, as many of them use common-emitter or common-source output stages, to maximize signal swing. Such stages are typically much more load sensitive than the classic common-collector stages generally used in dual-supply op amps.

There are now a greater *variety* of dual-supply op amps available. However, this is at least in part due to the ~30-year head start they have been enjoying. Currently, new op amp designs are increasingly oriented around one or more aspects of single-supply compatibility, with strong trends toward lower supply voltages, smaller packages, etc.

Device Selection Drivers

As the op amp design process is begun, it is useful to keep in mind the fact that there are several selection *drivers,* which can dictate priorities. This is illustrated by Figure 1-11.

Actually, any *single* heading along the top of this chart can in fact be the dominant selection driver, and take precedence over all of the others. In the early days of op amp design, when such things as supply range, package type etc. were fairly narrow in spread, performance was usually the major driver. Of course, it is still very much so, and will always be. But, today's systems are much more compact and lower in power, so things like package type, size, supply range, and multiple devices can often be major drivers of selection. As one example, if the only available supply voltage is 3V, you look at 3V compatible devices first, and then fill other performance parameters as you can.

FUNCTION	PERFORM	PACKAGE	MARKET
Single, Dual, Quad	Precision	Type	Cost
Single Or Dual Supply	Speed	Size	Availability
Supply Voltage	Distortion, Noise	Footprint	
	Low Bias Current		
	Power		

Figure 1-11: Some op amp selection drivers

As another example, one coming from another perspective, sometimes all-out performance can drive everything else. An ultra low, non-negotiable input current requirement can drive not only the type of amplifier, but also its package (a FET input device in a glass-sealed hermetic package may be optimum). Then, everything else follows from there. Similarly, high power output may demand a package capable of several watts dissipation, in which case you find the power handling device and package first, and then proceed accordingly.

At this point, the concept of these "selection drivers" is still quite general. The following sections of the chapter introduce device types, which supplements this with further details of a realistic selection process.

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7. Ray Stata, "Operational Amplifiers-Parts I and II," **Electromechanical Design**, September, November 1965.

8. Dan Sheingold, Ed., **Applications Manual for Operational Amplifiers for Modeling, Measuring, Manipulating, and Much Else**, George A. Philbrick Researches, Inc., Boston, MA, 1965. See also **Applications Manual for Operational Amplifiers for Modeling, Measuring, Manipulating, and Much Else, 2nd Ed.,** Philbrick/Nexus Research, Dedham, MA, 1966, 1984.

9. Walter G. Jung, **IC Op Amp Cookbook, 3rd Ed.**, Prentice-Hall PTR, 1986, 1997, ISBN: 0-13-889601-1.

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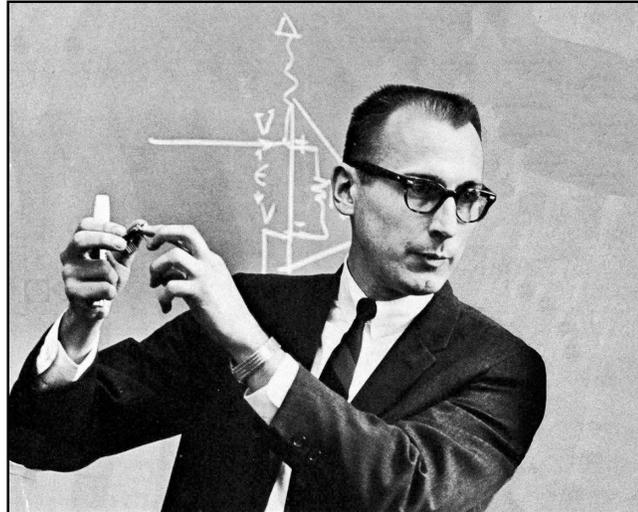
ACKNOWLEDGEMENTS:

Classic Cameo
Ray Stata Publications Establish ADI Applications Work

In January of 1965 Analog Devices Incorporated (ADI) was founded by Matt Lorber and Ray Stata. Operating initially from Cambridge, MA, modular op amps were the young ADI's primary product. In those days, Ray Stata did more than administrative tasks. He served in sales and marketing roles, and wrote many op amp applications articles. Even today, some of these are still available to ADI customers.

One very early article set was a two part series done for **Electromechanical Design**, which focused on clear, down-to-earth explanation of op amp principles. [1]

A second article for the new ADI publication **Analog Dialogue**, was entitled "Operational Integrators," and outlined various errors that plague integrators (including capacitor errors). [2]

A third impact article was also done for **Analog Dialogue**, titled "User's Guide to Applying and Measuring Operational Amplifier Specifications". [3] As the title denotes, this was a comprehensive guide to aid the understanding of op amp specifications, and also showed how to test them.

Ray authored an Applications Manual for the 201, 202, 203 and 210 series of chopper op amps. [4]

Ray was also part of the **EEE** "Speaks Out" series of article-interviews, where he outlined some of the subtle ways that op amp specs and behavior can trap unwary users (above photo from that article). [5]

So, although ADI today makes many other products, those early op amps were the company's roots.

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[1] Ray Stata, "Operational Amplifiers - Parts I and II," **Electromechanical Design**, Sept., Nov., 1965.

[2] Ray Stata, "Operational Integrators," **Analog Dialogue,** Vol. 1, No. 1, April, 1967**.** See also ADI AN357

[3] Ray Stata, "User's Guide to Applying and Measuring Operational Amplifier Specifications," **Analog Dialogue,** Vol. 1, No. 3, September 1967. See also ADI AN356.

[4] Ray Stata, **Applications Manual for 201, 202, 203 and 210 Chopper Op Amps**, ADI, 1967.

[5] "Ray Stata Speaks Out on 'What's Wrong with Op Amp Specs'," **EEE**, July 1968.

NOTES:

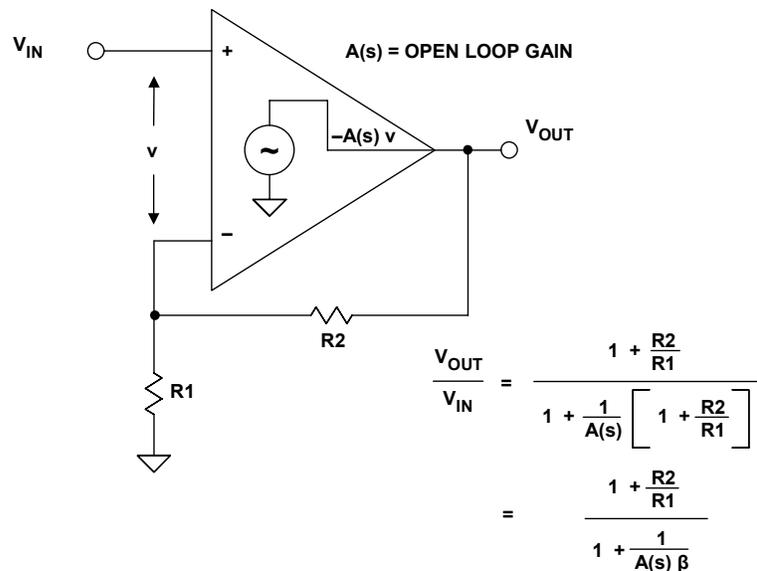# SECTION 1-2: OP AMP TOPOLOGIES
Walt Kester, Walt Jung, James Bryant

The previous section examined op amps without regard to their internal circuitry. In this section the two basic op amp topologies—voltage feedback (VFB) and current feedback (CFB)— are discussed in more detail, leading up to a detailed discussion of the actual circuit structures in Section 1-3.
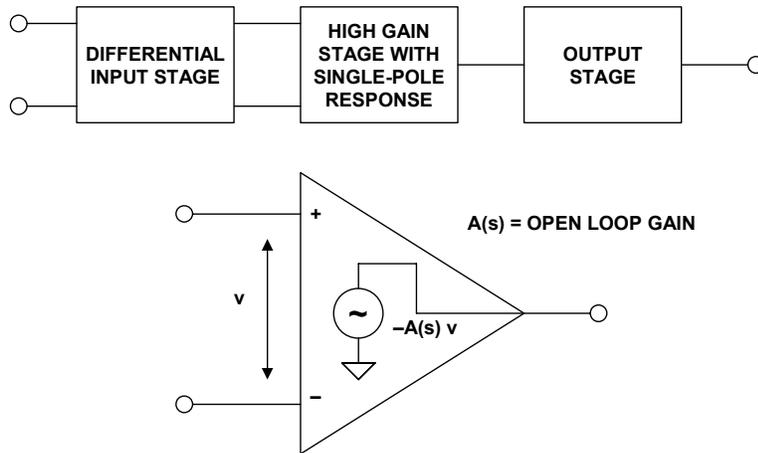
Figure 1-12: Voltage feedback (VFB) op amp

Although not explicitly stated, the previous section focused on the voltage feedback op amp and the related equations. In order to reiterate, the basic voltage feedback op amp is repeated here in Figure 1-12 above (without the feedback network) and in Figure 1-13 below (with the feedback network).

$$\frac{V_{OUT}}{V_{IN}} = \frac{1 + \dfrac{R2}{R1}}{1 + \dfrac{1}{A(s)}\left[1 + \dfrac{R2}{R1}\right]}$$

$$= \frac{1 + \dfrac{R2}{R1}}{1 + \dfrac{1}{A(s)\,\beta}}$$

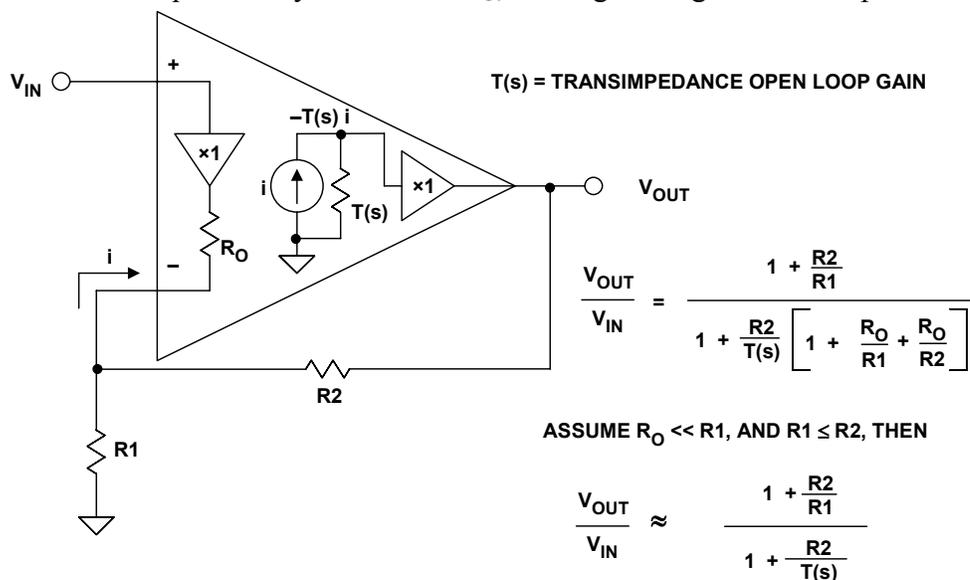*Figure 1-13: Voltage feedback op amp with feedback network connected*

It is important to note that the error signal developed because of the feedback network and the finite open-loop gain A(s) is in fact a small voltage, v.

Current Feedback Amplifier Basics

The basic *current feedback* amplifier topology is shown in Figure 1-14 below. Notice that within the model, a unity gain buffer connects the non-inverting input to the inverting input. In the ideal case, the output impedance of this buffer is zero ($R_O = 0$), and the error signal is a small current, i, which flows into the inverting input. The error current, i, is mirrored into a high impedance, T(s), and the voltage developed across T(s) is equal to T(s)·i. (The quantity T(s) is generally referred to as the *open-loop transimpedance gain*.)

This voltage is then buffered, and is connected to the op amp output. If R_O is assumed to be zero, it is easy to derive the expression for the closed-loop gain, V_{OUT}/V_{IN}, in terms of the R1-R2 feedback network and the *open-loop* transimpedance gain, T(s). The equation can also be derived quite easily for a finite R_O, and Fig. 1-14 gives both expressions.

T(s) = TRANSIMPEDANCE OPEN LOOP GAIN

$$\frac{V_{OUT}}{V_{IN}} = \frac{1 + \dfrac{R2}{R1}}{1 + \dfrac{R2}{T(s)}\left[1 + \dfrac{R_O}{R1} + \dfrac{R_O}{R2}\right]}$$

ASSUME $R_O \ll R1$, AND $R1 \leq R2$, THEN

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1 + \dfrac{R2}{R1}}{1 + \dfrac{R2}{T(s)}}$$

Figure 1-14: Current feedback (CFB) op amp topology

At this point it should be noted that current feedback op amps are often called *transimpedance* op amps, because the *open-loop* transfer function is in fact an impedance as described above. However, the term *transimpedance amplifier* is often applied to more general circuits such as current-to-voltage (I/V) converters, where either CFB or VFB op amps can be used. Therefore, some caution is warranted when the term *transimpedance* is encountered in a given application. On the other hand, the term *current feedback op amp* is rarely confused and is the preferred nomenclature when referring to op amp topology.

From this simple model, several important CFB op amp characteristics can be deduced.

- Unlike VFB op amps, CFB op amps *do not have balanced inputs.* Instead, the non-inverting input is high impedance, and the inverting input is low impedance.

- The open-loop gain of CFB op amps is measured in units of Ω (transimpedance gain) rather than V/V as for VFB op amps.

- For a fixed value feedback resistor R2, the closed-loop gain of a CFB can be varied by changing R1, without significantly affecting the closed-loop bandwidth. This can be seen by examining the simplified equation in Fig. 1-14. The denominator determines the overall frequency response; and if R2 is constant, then R1 of the numerator can be changed (thereby changing the gain) without affecting the denominator— hence the bandwidth remains relatively constant.

The CFB topology is primarily used where the ultimate in high speed and low distortion is required. The fundamental concept is based on the fact that in bipolar transistor circuits currents can be switched faster than voltages, all other things being equal. A more detailed discussion of CFB op amp AC characteristics can be found in Section 1-5.

Figure 1-15 below shows a simplified schematic of an early IC CFB op amp, the AD846— introduced by Analog Devices in 1988 (see Reference 1). Notice that full advantage is taken of the complementary bipolar (CB) process which provides well matched high f_t PNP and NPN transistors.
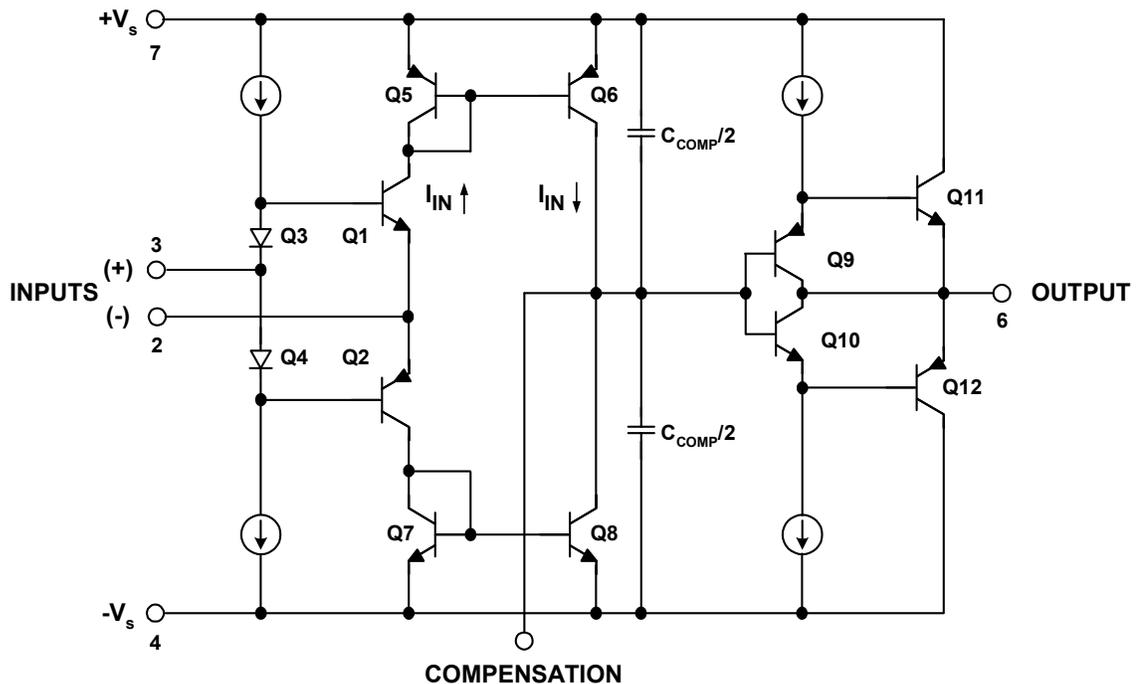
Figure 1-15: *AD846 current feedback op amp (1988)*

Transistors Q1-Q2 buffer the non-inverting input (pin 3) and drive the inverting input (pin 2). Q5-Q6 and Q7-Q8 act as current mirrors that drive the high impedance node. The C_{COMP} capacitor provides the dominant pole compensation; and Q9, Q10, Q11, and Q12 comprise the output buffer. In order to take full advantage of the CFB architecture, a high speed complementary bipolar (CB) IC process is required. With modern IC processes, this is readily achievable, allowing direct coupling in the signal path of the amplifier.

However, the basic concept of current feedback can be traced all the way back to early vacuum tube feedback circuitry, which used negative feedback to the input tube cathode. This use of the cathode for feedback would be analogous to the CFB op amp's low impedance (-) input, in Fig. 1-15.

1.25

Current Feedback Using Vacuum Tubes

Figure 1-16 below is an adaptation from a 1937 article on feedback amplifiers by Frederick E. Terman (see Reference 2). Notice that the AC-coupled R2 feedback resistor for this two-stage amplifier is connected to the low impedance cathode of T1, the pentode vacuum tube input stage. Similar examples of early tube circuits using cathode feedback can be found in Reference 3.

DC-coupled op amp design using vacuum tubes was difficult for numerous reasons. One reason was a lack of suitable level shifters. Multi-stage op amps either required extremely high supply voltages or suffered gain loss because of resistive level shifters. In a 1941 article, Stewart E. Miller describes how to use gas discharge tubes as level shifters in several vacuum tube amplifier circuits (see Reference 4). A circuit of particular interest is shown in Figure 1-17 (opposite).
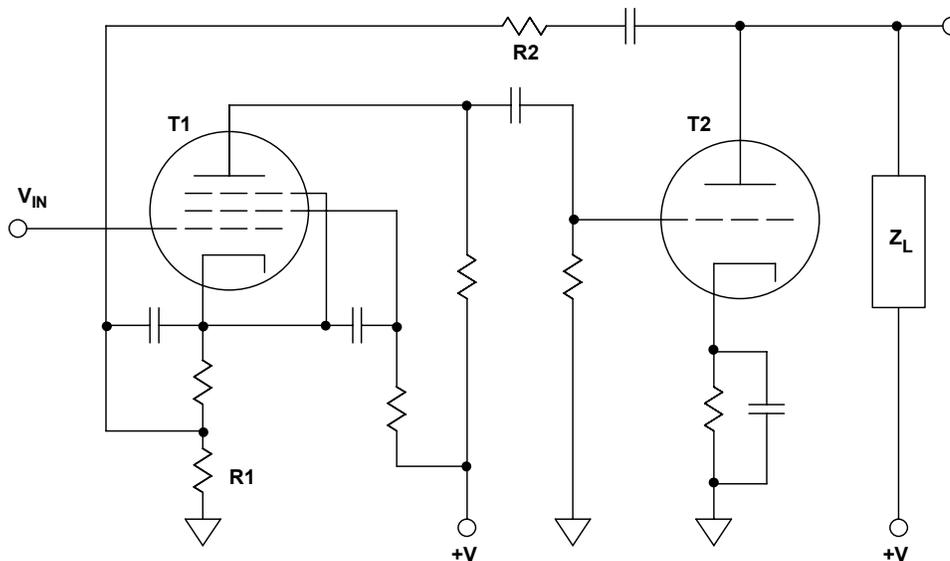
Adapted from: Frederick E. Terman, "Feedback Amplifier Design,"
Electronics, January 1937, pp. 12-15, 50.

Figure 1-16: *A 1937 vacuum tube feedback circuit designed by Frederick E. Terman, using current feedback to the low impedance input cathode (adapted from Reference 2)*

In the Fig. 1-17 reproduction of Miller's circuit, the R2 feedback resistor and the R1 gain setting resistor are labeled for clarity, and it can be seen that feedback is to the low impedance cathode of the input tube. The author suggests that the closed-loop gain of the amplifier can be adjusted from 72dB-102dB, by varying the R1 gain-setting resistor from 37.4Ω to 1.04Ω.

What is really interesting about the Miller circuit is its frequency response, which is reproduced in Figure 1-18 (opposite). Notice that the closed-loop bandwidth is nearly independent of the gain setting, and the circuit certainly does not exhibit a constant gain-bandwidth product as would be expected for a traditional VFB op amp.

For a gain of 72dB, the bandwidth is about 30kHz, and for a gain of 102dB (30dB increase), the bandwidth only drops to ~15kHz. With a 72dB gain at 30kHz VFB op amp, bandwidth would be expected to drop 5 octaves to ~0.9kHz for 102dB of gain.
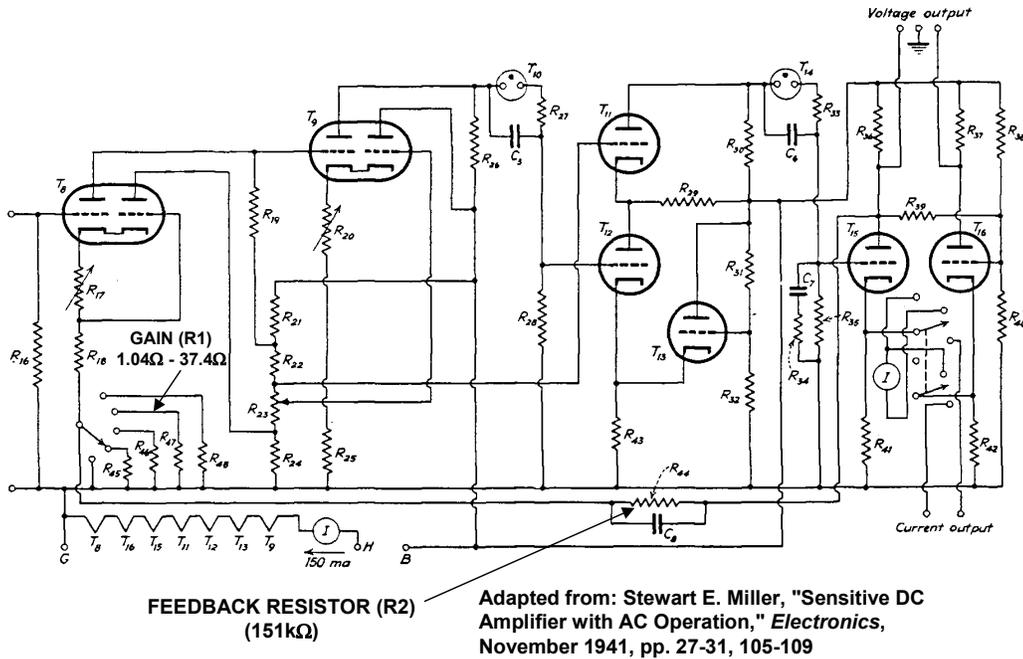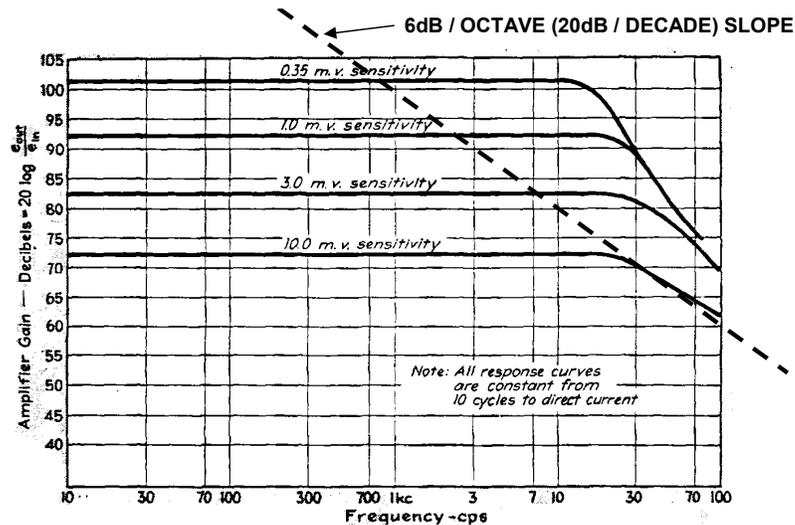

FEEDBACK RESISTOR (R2)
(151kΩ)

Adapted from: Stewart E. Miller, "Sensitive DC
Amplifier with AC Operation," *Electronics*,
November 1941, pp. 27-31, 105-109

Figure 1-17: *A 1941 vacuum tube feedback circuit using current feedback*

To clarify this point on bandwidth, a standard VFB op amp 6dB/octave (20dB/decade) slope has been added to Fig. 1-18 for reference.

Adapted from: Stewart E. Miller, "Sensitive DC Amplifier with AC Operation,"
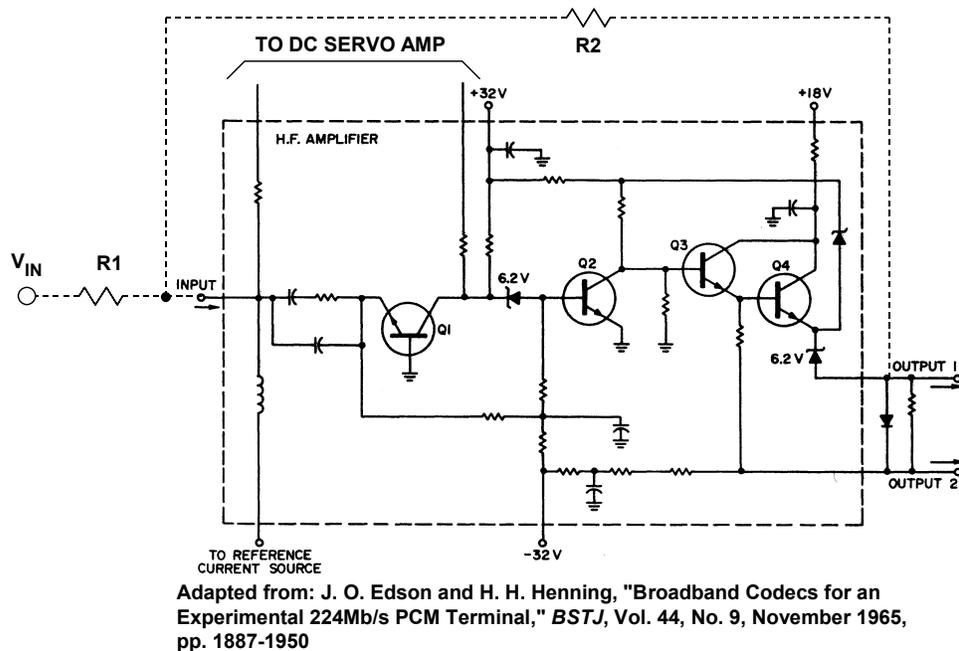*Electronics,* November 1941, pp. 27-31, 105-109

Figure 1-18: *A 1941 feedback circuit shows characteristic CFB gain-bandwidth relationship*

Although there is no mention of the significance of this within the text of the actual article, it nevertheless illustrates a popular application of CFB behavior, in the design of high speed programmable gain amplifiers with relatively constant bandwidth.

When transistor circuits ultimately replaced vacuum tube circuits between the late 1950s and the mid-1960s, the current feedback architecture became popular for certain high speed op amps. Figure 1-19 below shows a fast-settling op amp designed at Bell Labs in 1965, for use as a building block in high speed A/D converters (see Reference 5).

The circuit shown is a composite amplifier containing a high speed AC amplifier (shown inside the dotted outline) and a separate DC servo amplifier loop (not shown). The feedback resistor R2 is AC coupled to the low-impedance emitter of transistor Q1. The circuit design was somewhat awkward because of the lack of good high frequency PNP transistors, and it also required zener diode level shifters, and non-standard supplies.

Adapted from: J. O. Edson and H. H. Henning, "Broadband Codecs for an Experimental 224Mb/s PCM Terminal," *BSTJ*, Vol. 44, No. 9, November 1965, pp. 1887-1950

Figure 1-19: A 1965 solid state current feedback op amp design from Bell Labs

Hybrid circuit manufacturing technology, which was well established by the 1980s, allowed the use of fast, relatively well-matched NPN and PNP transistors, to realize CFB op amps. The Analog Devices' AD9610 and AD9611 hybrids were good examples of these devices introduced in the mid-1980s.

With the development of high speed complementary bipolar IC processes in the 1980s (see Reference 6) it became possible to realize completely DC-coupled current feedback op amps using PNP and NPN transistors such as the Analog Devices' AD846, introduced in 1988 (Fig. 1-15, again). Device matching and clever circuit design techniques give these modern IC CFB op amps excellent AC and DC performance without a requirement for separate level shifters, awkward supply voltages, or separate DC servo loops.

Various patents have been issued for these types of designs (see References 7 and 8, for example), but it should be remembered that the fundamental concepts were established decades earlier.

REFERENCES: OP AMP TOPOLOGIES

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3. Edward L. Ginzton, "DC Amplifier Design Techniques," **Electronics**, March 1944, pp. 98-102.

4. Stewart E. Miller, "Sensitive DC Amplifier with AC Operation," **Electronics**, November 1941, pp. 27-31, 105-109.

5. J. O. Edson and H. H. Henning, "Broadband Codecs for an Experimental 224Mb/s PCM Terminal," **Bell System Technical Journal**, Vol. 44, No. 9, November 1965, pp. 1887-1950.

6. "Op Amps Combine Superb DC Precision and Fast Settling," **Analog Dialogue**, Vol. 22, No. 2, pp. 12-15.

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8. Royal A. Gosser, "DC-Coupled Transimpedance Amplifier," **US Patent 4,970,470**, Filed October 10, 1989, Issued November 13, 1990.

NOTES:

SECTION 1-3: OP AMP STRUCTURES
Walt Kester, Walt Jung, James Bryant

This section describes op amps in terms of their *structures*, and Section 1-4 discusses op amp *specifications*. It is hard to decide which to discuss first, since discussion of specifications, to be useful, entails reference to structures, and discussion of structures likewise requires reference to the performance feature that they are intended to optimize.

Since the majority of readers will have at least some familiarity with operational amplifiers and their specifications, we shall discuss structures first, and assume that readers will have at least a first-order idea of the definitions of the various specifications. Where this assumption proves ill-founded, the reader should look ahead to the next section to verify any definitions required.

Because single-supply devices permeate practically all modern system designs, the related design issues are integrated into the following op amp structural discussions.

Single-Supply Op Amp Issues

Over the last several years, single-supply operation has become an increasingly important requirement because of market demands. Automotive, set-top box, camera/cam-corder, PC, and laptop computer applications are demanding IC vendors to supply an array of linear devices that operate on a single-supply rail, with the same performance of dual supply parts. Power consumption is now a key parameter for line or battery operated systems, and in some instances, more important than cost. This makes low-voltage/low supply current operation critical; at the same time, however, accuracy and precision requirements have forced IC manufacturers to meet the challenge of "doing more with less" in their amplifier designs.

In a single-supply application, the most immediate effect on the performance of an amplifier is the reduced input and output signal range. As a result of these lower input and output signal excursions, amplifier circuits become more sensitive to internal and external error sources. Precision amplifier offset voltages on the order of 0.1mV are less than a 0.04 LSB error source in a 12-bit, 10V full-scale system. In a single-supply system, however, a "rail-to-rail" precision amplifier with an offset voltage of 1mV represents a 0.8LSB error in a 5V fullscale system (or 1.6LSB for 2.5V fullscale).

To keep battery current drain low, larger resistors are usually used around the op amp. Since the bias current flows through these larger resistors, they can generate offset errors equal to or greater than the amplifier's own offset voltage.

Gain accuracy in some low voltage single-supply devices is also reduced, so device selection needs careful consideration. Many amplifiers with ~120dB open-loop gains typically operate on dual supplies— for example OP07 types. However, many single-supply/rail-to-rail amplifiers for precision applications typically have open-loop gains between 25,000 and 30,000 under light loading (>10kΩ). Selected devices, like the

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OP113/213/413 family, do have high open-loop gains (>120dB), for use in demanding applications. Another example would be the AD855x chopper-stabilized op amp series.

Many trade-offs are possible in the design of a single-supply amplifier circuit— speed versus power, noise versus power, precision versus speed and power, etc. Even if the noise floor remains constant (highly unlikely), the signal-to-noise ratio will drop as the signal amplitude decreases.

Besides these limitations, many other design considerations that are otherwise minor issues in dual-supply amplifiers now become important. For example, signal-to-noise (SNR) performance degrades as a result of reduced signal swing. "Ground reference" is no longer a simple choice, as one reference voltage may work for some devices, but not others. Amplifier voltage noise increases as operating supply current drops, and bandwidth decreases. Achieving adequate bandwidth and required precision with a somewhat limited selection of amplifiers presents significant system design challenges in single-supply, low-power applications.

Most circuit designers take "ground" reference for granted. Many analog circuits scale their input and output ranges about a ground reference. In dual-supply applications, a reference that splits the supplies (0V) is very convenient, as there is equal supply headroom in each direction, and 0V is generally the voltage on the low impedance ground plane.

In single-supply/rail-to-rail circuits, however, the ground reference can be chosen anywhere within the supply range of the circuit, since there is no standard to follow. The choice of ground reference depends on the type of signals processed and the amplifier characteristics. For example, choosing the negative rail as the ground reference may optimize the dynamic range of an op amp whose output is designed to swing to 0V. On the other hand, the signal may require level shifting in order to be compatible with the input of other devices (such as ADCs) that are not designed to operate at 0V input.

Very early single-supply "zero-in, zero-out" amplifiers were designed on bipolar processes, which optimized the performance of the NPN transistors. The PNP transistors were either lateral or substrate PNPs with much less bandwidth than the NPNs. Fully complementary processes are now required for the new-breed of single-supply/rail-to-rail operational amplifiers. These new amplifier designs don't use lateral or substrate PNP transistors within the signal path, but incorporate parallel NPN and PNP input stages to accommodate input signal swings from ground to the positive supply rail. Furthermore, rail-to-rail output stages are designed with bipolar NPN and PNP common-emitter, or N-channel/P-channel common-source amplifiers whose collector-emitter saturation voltage or drain-source channel on-resistance determine output signal swing, as a function of the load current.

The characteristics of a single-supply amplifier input stage (common-mode rejection, input offset voltage and its temperature coefficient, and noise) are critical in precision, low-voltage applications. Rail-rail input operational amplifiers must resolve small signals, whether their inputs are at ground, or in some cases near the amplifier's positive supply. Amplifiers having a minimum of 60dB common-mode rejection over the entire

input common-mode voltage range from 0V to the positive supply are good candidates. It is not necessary that amplifiers maintain common-mode rejection for signals beyond the supply voltages. *But, what* is *required is that they do not self-destruct for momentary overvoltage conditions!* Furthermore, amplifiers that have offset voltages less than 1mV and offset voltage drifts less than 2µV/°C are also very good candidates for precision applications. Since *input* signal dynamic range and SNR are equally if not more important than *output* dynamic range and SNR, precision single-supply/rail-to-rail operational amplifiers should have noise levels referred-to-input (RTI) less than 5µVp-p in the 0.1Hz to 10Hz band.

The need for rail-to-rail amplifier output stages is also driven by the need to maintain wide dynamic range in low-supply voltage applications. A single-supply/rail-to-rail amplifier should have output voltage swings that are within at least 100mV of either supply rail (under a nominal load). The output voltage swing is very dependent on output stage topology and load current.

◆ **Single Supply Offers:**
  ● **Lower Power**
  ● **Battery Operated Portable Equipment**
  ● **Requires Only One Voltage**

◆ **Design Tradeoffs:**
  ● **Reduced Signal Swing Increases Sensitivity to Errors Caused by Offset Voltage, Bias Current, Finite Open-Loop Gain, Noise, etc.**
  ● **Must Usually Share Noisy Digital Supply**
  ● **Rail-to-Rail Input and Output Needed to Increase Signal Swing**
  ● **Precision Less than the best Dual Supply Op Amps but not Required for All Applications**
  ● **Many Op Amps Specified for Single Supply, but do not have Rail-to-Rail Inputs or Outputs**

Figure 1-20: Single-supply op amp design issues

Generally, the voltage swing of a good rail-to-rail output stage should maintain its rated swing for loads down to 10kΩ. The smaller the V_{OL} and the larger the V_{OH}, the better. System parameters, such as "zero-scale" or "full-scale" output voltage, should be determined by an amplifier's V_{OL} (for zero-scale) and V_{OH} (for full-scale).

Since the majority of single-supply data acquisition systems require at least 12- to 14-bit performance, amplifiers which exhibit an open-loop gain greater than 30,000 for all loading conditions are good choices in precision applications. Single-supply op amp design issues are summarized in Figure 1-20 above.

Op Amp Input Stages

It is extremely important to understand input and output structures of op amps in order to properly design the required interfaces. For ease of discussion, the two can be examined separately, as there is no particular reason to relate them at this point.

Bipolar Input Stages

The very common and basic bipolar input stage of Figure 1-21 below consists of a "long-tailed pair" built with bipolar transistors. It has a number of advantages: it is simple, has very low offset, the bias currents in the inverting and non-inverting inputs are well-matched and do not vary greatly with temperature. In addition, minimizing the initial offset voltage of a bipolar op amp by laser trimming also minimizes its drift over temperature. This architecture was used in the very earliest monolithic op amps such as the μA709. It is also used with modern high speed types, like the AD829 and AD8021. Although NPN bipolars are shown, the concept also applies with the use of PNP bipolars.
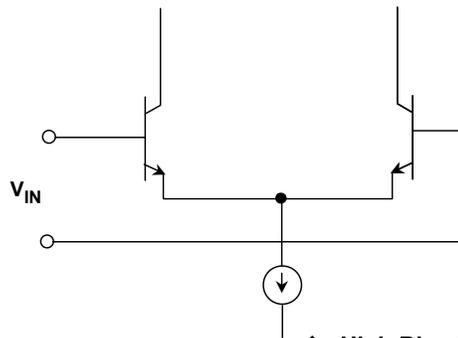
◆ **Low Offset: As low as 10μV**

◆ **Low Offset Drift: As low as 0.1μV/°C**

◆ **Temperature Stable I_B**

◆ **Well-Matched Bias Currents**

◆ **Low Voltage Noise: As low as 1nV/√Hz**

◆ **High Bias Currents: 50nA - 10μA**

◆ **(Except Super-Beta: 50pA - 5nA, More Complex and Slower)**

◆ **Medium Current Noise: 1pA/√Hz**

◆ **Matching source impedances minimize offset error due to bias current**

Figure 1-21: A bipolar transistor input stage

The AD829, introduced in 1990, is shown in Figure 1-22 (opposite). This op amp uses a bipolar differential input stage, Q1-Q2, which drives a "folded cascode" gain stage which consists of a fast pair of PNP transistors, Q3-Q4 (see Reference 1). These PNPs drive a current mirror that provides the differential-to-single-ended conversion. The output stage is a two-stage complementary emitter follower.

The AD829 is a wideband video amplifier with a 750MHz uncompensated gain-bandwidth product, and it operates on ±5V to ±15V supplies. For added flexibility, the AD829 provides access to the internal compensation node (C_{COMP}). This allows the user to customize frequency response characteristics for a particular application where the closed-loop gain is less than 20. The RC network connected between the output and the high impedance node helps maintain stability, when driving capacitive loads.

Input bias current is 7μA maximum at +25°C, input voltage noise is 1.7nV/√Hz, and input current noise is 1.5pA/√Hz. Laser wafer trimming reduces the input offset voltage to 0.5mV maximum for the "A" grade. Typical input offset voltage drift is 0.3μV/°C.

In an op amp input circuit such as Fig. 1-22, the input bias current is the base current of the transistors comprising the long-tailed pair, Q1-Q2. It can be quite high, especially in high speed amplifiers, because the collector currents are high. It is typically ~3μA, for the AD829. In amplifiers where the bias current is *uncompensated* (as true in this case), the bias current will be equal to ½ the Q1-Q2 emitter current, divided by the H_{FE}.

The bias current of a simple bipolar input stage can be reduced by a couple of measures. One is by means of *bias current compensation*, to be described further below.

BIAS CURRENT FOR AD829 = 7μA MAX @ +25°C
INPUT VOLTAGE NOISE = 1.7nV/√Hz
INPUT CURRENT NOISE = 1.5pA/√Hz
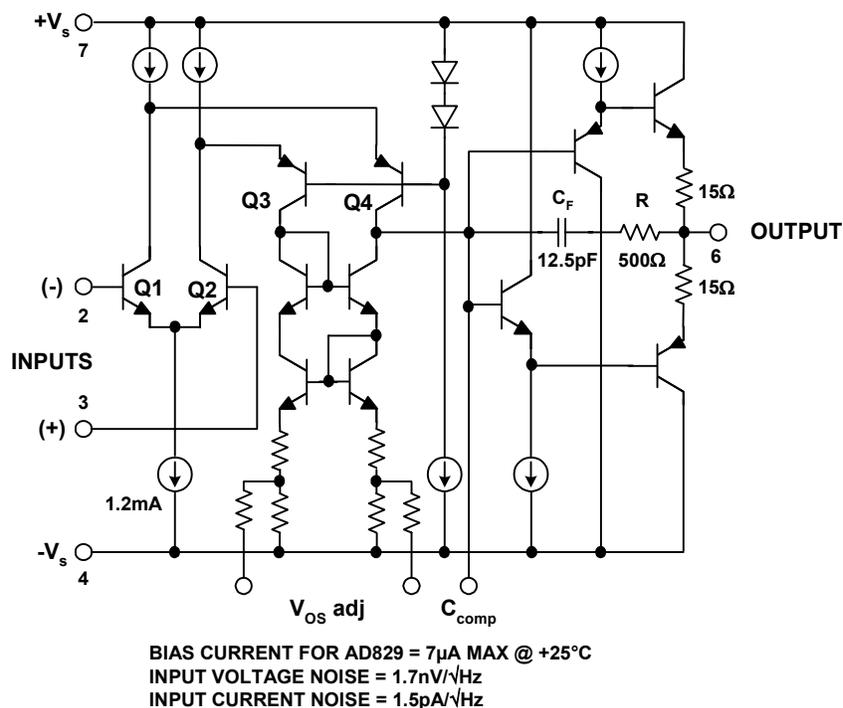
Figure 1-22: AD829 op amp simplified schematic

Another method of reducing bias current is by the use of *super-beta* transistors for Q1-Q2. Super-beta transistors are specially processed devices with a very narrow base region. They typically have a current gain of thousands or tens of thousands (rather than the more usual hundreds). Op amps with super-beta input stages have much lower bias currents, but they also have more limited frequency response.

Since the breakdown voltages of super-beta devices are quite low, they also require additional circuitry to protect the input stage from damage caused by over-voltage (for example, they wouldn't operate in the circuit of Fig. 1-22).

Some examples of super-beta input bipolar op amps are the AD704/705/706 series, and the OP97/297/497 series (single, dual, quad). These devices have typical 25°C bias currents of 100pA or less.
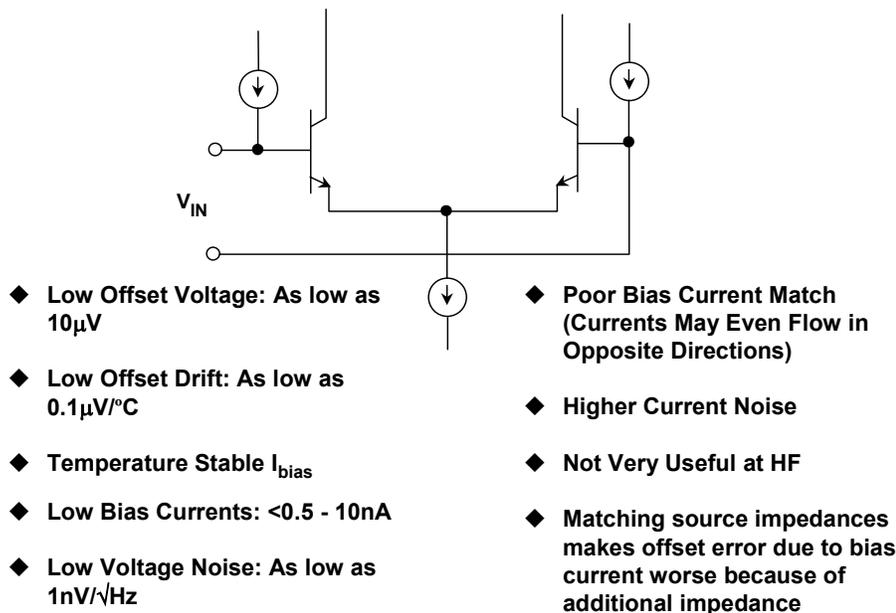
Bias Current Compensated Bipolar Input Stage

A simple bipolar input stage such as used in Fig. 1-22 exhibits high bias current because the currents seen externally are in fact the base currents of the two input transistors.

By providing this necessary bias currents via an internal current source, as in Figure 1-23 below, the only *external* current then flowing in the input terminals is the difference current between the base current and the current source, which can be quite small.

Most modern precision op amps use some means of internal bias current compensation, examples would be the familiar OP07 and OP27 series.

- ◆ **Low Offset Voltage: As low as 10μV**
- ◆ **Low Offset Drift: As low as 0.1μV/°C**
- ◆ **Temperature Stable I$_{bias}$**
- ◆ **Low Bias Currents: <0.5 - 10nA**
- ◆ **Low Voltage Noise: As low as 1nV/√Hz**

- ◆ **Poor Bias Current Match (Currents May Even Flow in Opposite Directions)**
- ◆ **Higher Current Noise**
- ◆ **Not Very Useful at HF**
- ◆ **Matching source impedances makes offset error due to bias current worse because of additional impedance**

Figure 1-23: A bias current compensated bipolar input stage

The well-known OP27 op amp family is good example of bias compensated op amps (see References 2 and 3). The simplified schematic of the OP27, shown in Figure 1-24 (opposite), shows that the multiple-collector transistor Q6 provides the bias current compensation for the input transistors Q1 and Q2. The "G" grade of the OP27 has a maximum input bias current specification of ±80nA at 25°C. Input voltage noise is 3nV/√Hz, and input current noise is 0.4pA/√Hz. Offset voltage trimming by "Zener-zapping" reduces the input offset voltage of the OP27 to 50μV maximum at +25°C for the "E" grade device (see Reference 4 for details of this trim method).

Bias current compensated input stages have many of the good features of the simple bipolar input stage, namely: low voltage noise, low offset, and low drift. Additionally, they have low bias current which is fairly stable with temperature. However, their current noise is not very good, and their bias current matching is poor.

These latter two undesired side effects result from the external bias current being the *difference* between the compensating current source and the input transistor base current. Both of these currents inevitably have noise. Since they are uncorrelated, the two noises add in a root-sum-of-squares fashion (even though the DC currents subtract).

Since the resulting external bias current is the difference between two nearly equal currents, there is no reason why the net current should have a defined polarity. As a result, the bias currents of a bias-compensated op amp may not only be mismatched, they can actually flow in opposite directions! In most applications this isn't important, but in some it can have unexpected effects (for example the droop of a sample-and-hold (SHA) built with a bias-compensated op amp may have either polarity).

In many cases, the bias current compensation feature is not mentioned on an op amp data sheet, and a simplified schematic isn't supplied. It is easy to determine if bias current compensation is used by examining the bias current specification. If the bias current is specified as a "±" value, the op amp is most likely compensated for bias current.

BIAS CURRENT FOR OP27G = ±80nA MAX @ +25°C
INPUT VOLTAGE NOISE = 3nV/√Hz
INPUT CURRENT NOISE = 0.4pA/√Hz
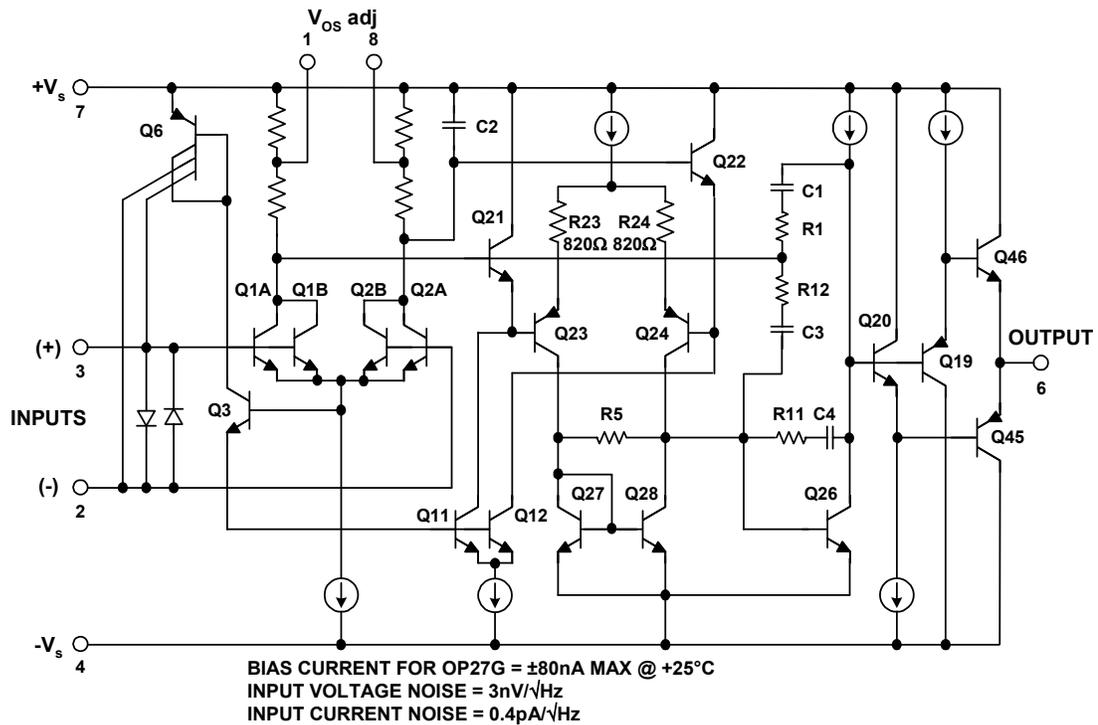
Figure 1-24: OP27 op amp uses bias current compensated input stage

Note that this can easily be verified, by examining the *offset current* specification (the difference in the bias currents). If internal bias current compensation exists, the offset current will be of the same magnitude as the bias current. Without bias current compensation, the offset current will generally be at least a factor of 10 smaller than the bias current. Note that these relationships generally hold, regardless of the exact magnitude of the bias currents.

It is also a well-known fact that, within an op amp application circuit, the effects of bias current on the output offset voltage of an op amp can often be cancelled by making the source resistances at the two inputs equal. But, there is an important caveat here. The validity of this practice only holds true for bipolar input op amps *without* bias current compensation, that is, where the input currents are well matched. In a case of an op amp using internal bias current compensation, adding an extra resistance to either input will usually make the output offset worse!

Bias Current Compensated Super-Beta Bipolar Input Stage

As mentioned above, the OP97/297/497-series are high performance super-beta op amps, which also use input bias current compensation. As a result, their input bias currents are ±150pA max at 25°C. Note that in this case the "±" prefix to the bias current magnitude indicates that the amplifier uses internal bias current compensation.

A simplified schematic of an OP97 (or ¼ of the OP497) is shown in Figure 1-25 below. Note that the Q1-Q2 super-beta pair is protected against large destructive differential input voltages, by the use of both back-to-back diodes, and series current-limiting resistors. Note also that Q1-Q2 super-beta pair is also protected against excessive collector voltage, by an elaborate bias and bootstrapping network.

BIAS CURRENT FOR OP497F = ±150pA MAX @ +25°C
INPUT VOLTAGE NOISE = 15nV/√Hz
INPUT CURRENT NOISE = 20fA/√Hz
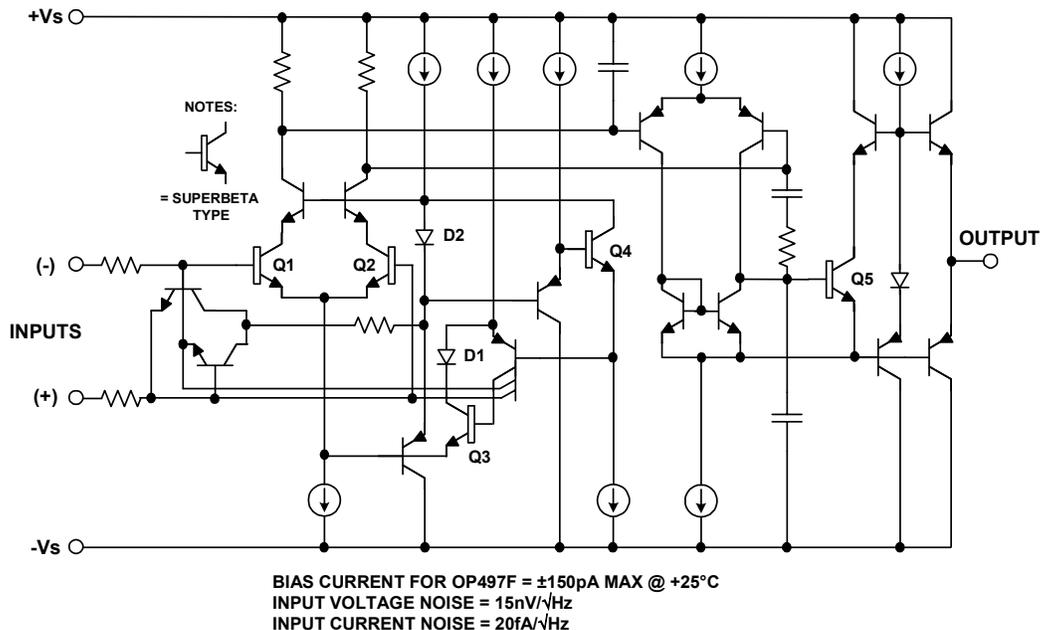
Figure 1-25: The OP97, OP297 and OP497 op amp series uses super-beta input stage transistors and bias current compensation

As a result of these clamping and protection circuits, the input common-mode voltage of this op amp series can safely vary over the full range of the supply voltages used.

FET Input Stages

Field-Effect Transistors (FETs) have much higher input impedance than do bipolar junction transistors (BJTs) and would therefore seem to be ideal devices for op amp input stages. However, they cannot be manufactured on all bipolar IC processes, and when a process does allow their manufacture, they often have their own problems.

FETs have high input impedance, low bias current, and good high frequency performance (in an op amp, the lower g_m of the FET devices allows higher tail currents, thereby increasing the maximum slew rate). FETs also have much lower current noise.

On the other hand, the input offset voltage of FET long-tailed pairs, however, is not as good as the offset of corresponding BJTs, and trimming for minimum offset does not simultaneously minimize drift. A separate trim is needed for drift, and as a result, offset and drift in a JFET op amp, while good, aren't as good as the best BJT ones. A simplified trim procedure for an FET input op amp stage is shown in Figure 1-26 below.

It is possible to make JFET op amps with very low voltage noise, but the devices involved are very large and have quite high input capacitance, which varies with input voltage, and so a trade-off is involved between voltage noise and input capacitance.

The bias current of an FET op amp is the leakage current of the gate diffusion (or the leakage of the gate protection diode, which has similar characteristics for a MOSFET). Such leakage currents double with every 10°C increase in chip temperature so that a FET op amp bias current is *one thousand times greater* at 125°C than at 25°C. Obviously this can be important when choosing between a bipolar or FET input op amp, especially in high temperature applications where bipolar op amp input bias current actually decreases.
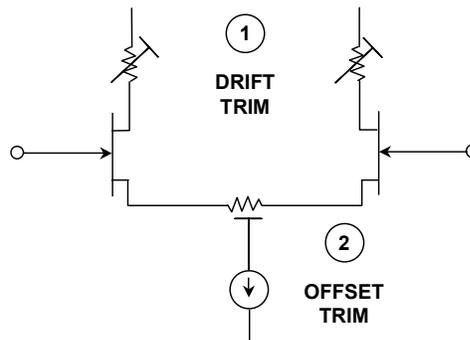
◆ Offset as Low as 50µV

◆ Offset TC ~ 5µV/°C

◆ Low Current Noise

◆ Bias Current as Low as 20fA

◆ I_B doubles every 10°C

◆ Tradeoff Between Voltage Noise and Input Capacitances

Figure 1-26: *Junction field effect transistor (JFET) input op amp stage showing offset and drift trims*

Thus far, we have spoken generally of all kinds of FETs, that is junction (JFETs) and MOS (MOSFETs). In practice, combined bipolar/JFET technology op amps (i.e., BiFET) achieve better performance than op amps using purely MOSFET or CMOS technology. While ADI and others make high performance op amps with MOS or CMOS input stages, in general these op amps have worse offset and drift, voltage noise, high-frequency performance than the bipolar counterparts. The power consumption is usually somewhat lower than that of bipolar op amps with comparable, or even better, performance.

JFET devices require more headroom than do BJTs, since their pinchoff voltage is typically greater than a BJTs base-emitter voltage. Consequently, they are more difficult to operate at very low power supply voltages (1-2V). In this respect, CMOS has the advantage of requiring less headroom than JFETs.

Rail-Rail Input Stages

Today, there is common demand for op amps with input CM voltage that includes *both* supply rails, i.e., *rail-to-rail* CM operation. While such a feature is undoubtedly useful in some applications, engineers should recognize that there are still relatively few applications where it is absolutely essential. These applications should be distinguished from the many more applications where a CM range *close* to the supplies, or one that includes *one* supply is necessary, but true input rail-to-rail operation is not.

In many single-supply applications, it is required that the input CM voltage range extend to one of the supply rails (usually ground). High-side or low-side current-sensing applications are examples of this. Many amplifiers can handle 0V CM inputs, and they are easily designed using PNP differential pairs (or N-channel JFET pairs) as shown in Figure 1-27 below. The input CM range of such an op amp generally extends from about 200mV below the negative rail (-V$_S$ or ground), to about 1-2V of the positive rail, +V$_S$.
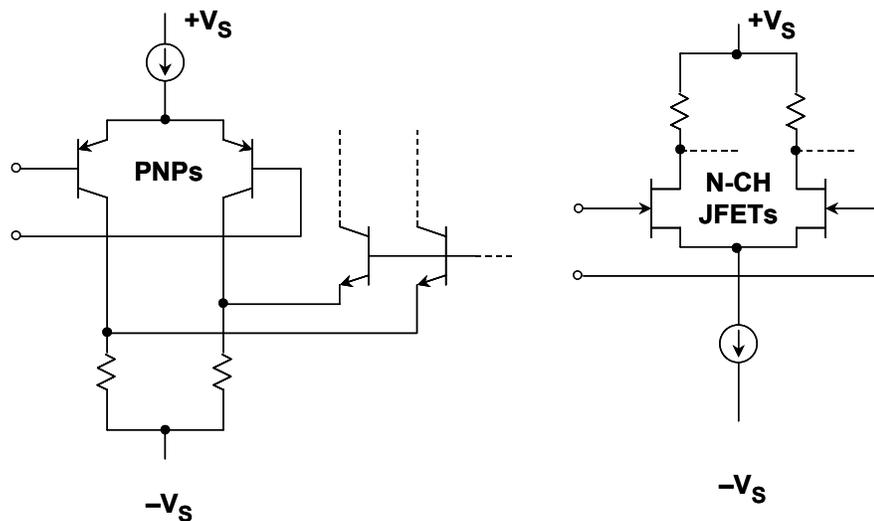
Figure 1-27: *PNP or N-channel JFET stages allow CM inputs to the negative rail*

An input stage could also be designed with NPN transistors (or P-channel JFETs), in which case the input CM range would include the positive rail, and go to within about 1-2V of the negative rail. This requirement typically occurs in applications such as high-side current sensing. The OP282/OP482 input stage uses a P-channel JFET input pair whose input CM range includes the positive rail, making it suitable for high-side sensing.

The AD823 is a dual 16MHz (G = +1) op amp with an N-channel JFET input stage (as in Fig. 1-27 right). A simplified schematic of the AD823 is shown in Figure 1-28 (opposite). This device can operate on single-supply voltages from +3 to +36V. This range also allows operation on traditional ±5V, or ±15V dual supplies if desired. Similar devices in a related (but lower power) family include the AD820, the AD822, and the AD824.

The AD823 JFET input stage allows the input common-mode voltage to range from 200mV below the negative supply to within about 1.5V of the positive supply. Input offset voltage is 0.8mV maximum at +25°C, input bias current is 25pA maximum at +25°C, offset voltage drift is 2μV/°C, and input voltage noise is 16nV/√Hz. Current noise

is only 1fA/√Hz. The AD823 is laser wafer trimmed for both offset voltage and offset voltage drift as described above.

BIAS CURRENT = 25pA MAX @ +25°C
INPUT OFFSET VOLTAGE = 0.8mV MAX @ +25°C
INPUT VOLTAGE NOISE = 15nV/√Hz
INPUT CURRENT NOISE = 1fA/√Hz
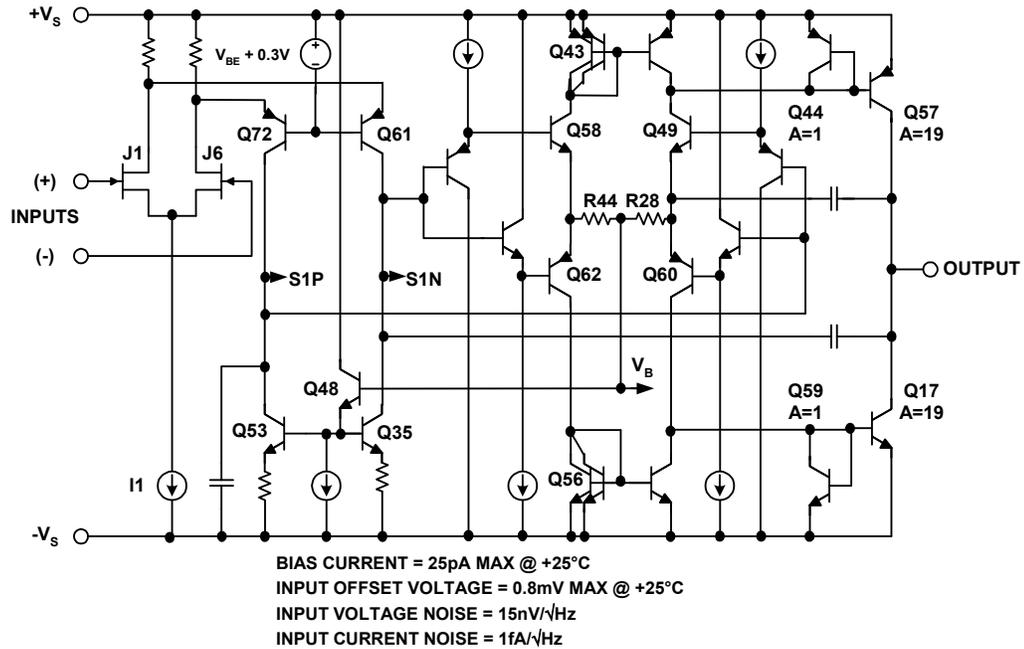
Figure 1-28: AD823 JFET input op amp simplified schematic

A simplified diagram of a true rail-to-rail input stage is shown in Figure 1-29 below. Note that this requires use of *two* long-tailed pairs, one of PNP bipolar transistors Q1-Q2, the other of NPN transistors Q3-Q4. Similar input stages can also be made with CMOS pairs.
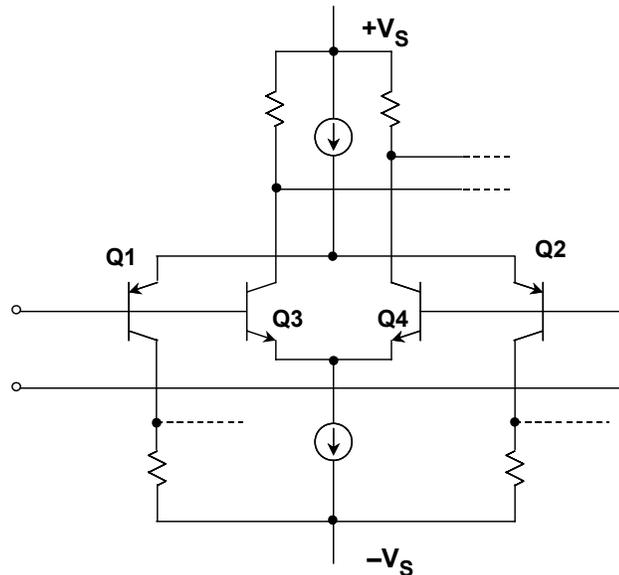
Figure 1-29: A true rail-to-rail bipolar transistor input stage

It should be noted that these two pairs will exhibit *different* offsets and bias currents, so when the applied CM voltage changes, the amplifier input offset voltage and input bias current does also. In fact, when both current sources remain active throughout most of the entire input common-mode range, amplifier input offset voltage is the *average* offset voltage of the two pairs. In those designs where the current sources are alternatively

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switched off at some point along the input common-mode voltage, amplifier input offset voltage is dominated by the PNP pair offset voltage for signals near the negative supply, and by the NPN pair offset voltage for signals near the positive supply. As noted, a true rail-to-rail input stage can also be constructed from CMOS transistors, for example as in the case of the CMOS AD8531/8532/8534 op amp family.

Amplifier input bias current, a function of transistor current gain, is also a function of the applied input common-mode voltage. The result is relatively poor common-mode rejection (CMR), and a changing common-mode input impedance over the CM input voltage range, compared to familiar dual-supply devices. These specifications should be considered carefully when choosing a rail-to-rail input op amp, especially for a non-inverting configuration. Input offset voltage, input bias current, and even CMR may be quite good over *part* of the common-mode range, but much worse in the region where operation shifts between the NPN and PNP devices, and vice versa.

True rail-to-rail amplifier input stage designs must transition from one differential pair to the other differential pair, somewhere along the input CM voltage range. Some devices like the OP191/291/491 family and the OP279 have a common-mode crossover threshold at approximately 1V below the positive supply (where signals do not often occur). The PNP differential input stage is active from about 200mV below the negative supply to within about 1V of the positive supply. Over this common-mode range, amplifier input offset voltage, input bias current, CMR, input noise voltage/current are primarily determined by the characteristics of the PNP differential pair. At the crossover threshold, however, amplifier input offset voltage becomes the average offset voltage of the NPN/PNP pairs and can change rapidly.

Also, as noted previously, amplifier bias currents are dominated by the PNP differential pair over most of the input common-mode range, and change polarity and magnitude at the crossover threshold when the NPN differential pair becomes active.

Op amps like the OP184/284/484 family, shown in Figure 1-30 opposite, utilize a rail-to-rail input stage design where both NPN and PNP transistor pairs are active throughout most of the entire input CM voltage range. With this approach to biasing, there is no CM crossover threshold. Amplifier input offset voltage is the average offset voltage of the NPN and the PNP stages, and offset voltage exhibits a smooth transition throughout the entire input CM range, due to careful laser trimming of input stage resistors.

In the same manner, through careful input stage current balancing and input transistor design, the OP184 family input bias currents also exhibit a smooth transition throughout the entire CM input voltage range. The exception occurs at the very extremes of the input range, where amplifier offset voltages and bias currents increase sharply, due to the slight forward-biasing of parasitic p-n junctions. This occurs for input voltages within approximately 1V of either supply rail.

When *both* differential pairs are active throughout most of the entire input common-mode range, amplifier transient response is faster through the middle of the common-mode range by as much as a factor of 2 for bipolar input stages and by a factor of √2 for JFET input stages. This is due to the higher transconductance of two operating input stages.

Input stage g_m determines the slew rate and the unity-gain crossover frequency of the amplifier, hence response time degrades slightly at the extremes of the input common-mode range when either the PNP stage (signals approaching the positive supply rail) or the NPN stage (signals approaching the negative supply rail) are forced into cutoff. The thresholds at which the transconductance changes occur are approximately within 1V of either supply rail, and the behavior is similar to that of the input bias currents.
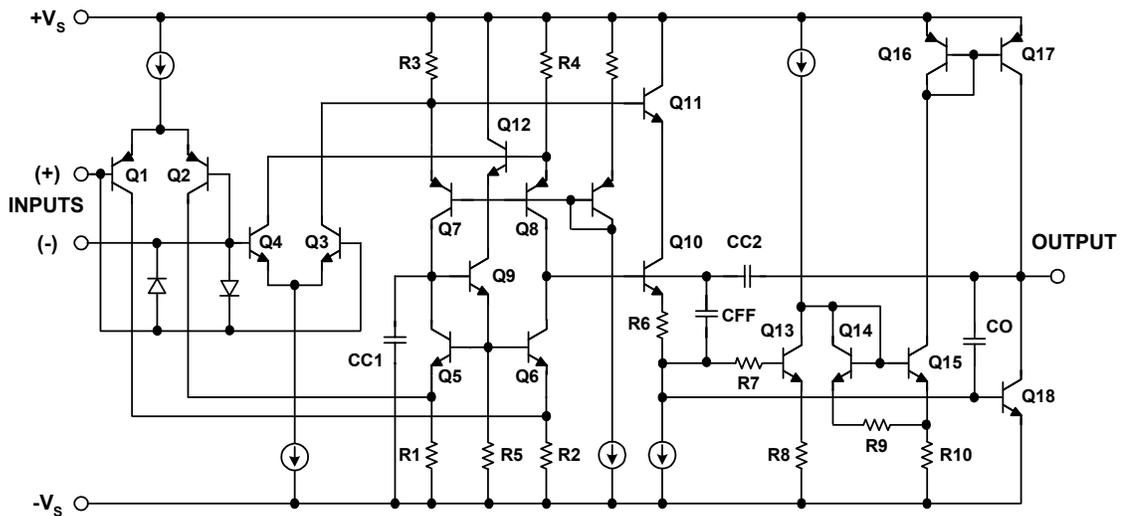
*Figure 1-30: OP284 op amp simplified schematic shows
true rail-to-rail input stage*

In light of the many quirks of true rail-to-rail op amp input stages, applications which do require true rail-to-rail inputs should be carefully evaluated, and an amplifier chosen to ensure that its input offset voltage, input bias current, common-mode rejection, and noise (voltage and current) are suitable.

Don't forget Input Overvoltage Considerations

In order to achieve the performance levels required, it is sometimes not possible to provide complete overdrive protection within IC op amps. Although most op amps have some type of input protection, care must still be taken to prevent possible damage against both CM and differential voltage stress.

This is most likely to occur when the input signal comes from an external sensor, for example. Rather than present a cursory discussion of this topic here, the reader is instead referred to Chapter 7, Section 7-4 for a detailed examination of this important issue.

Output Stages

The earliest IC op amp output stages were NPN emitter followers with NPN current sources or resistive pull-downs, as shown in Figure 1-31A below. Naturally, the slew rates were greater for positive-going than they were for negative-going signals.

While all modern op amps have push-pull output stages of some sort, many are still asymmetrical, and have a greater slew rate in one direction than the other. Asymmetry tends to introduce distortion on AC signals and generally results from the use of IC processes with faster NPN than PNP transistors. It may also result in an ability of the output to approach one supply more closely than the other in terms of saturation voltage.
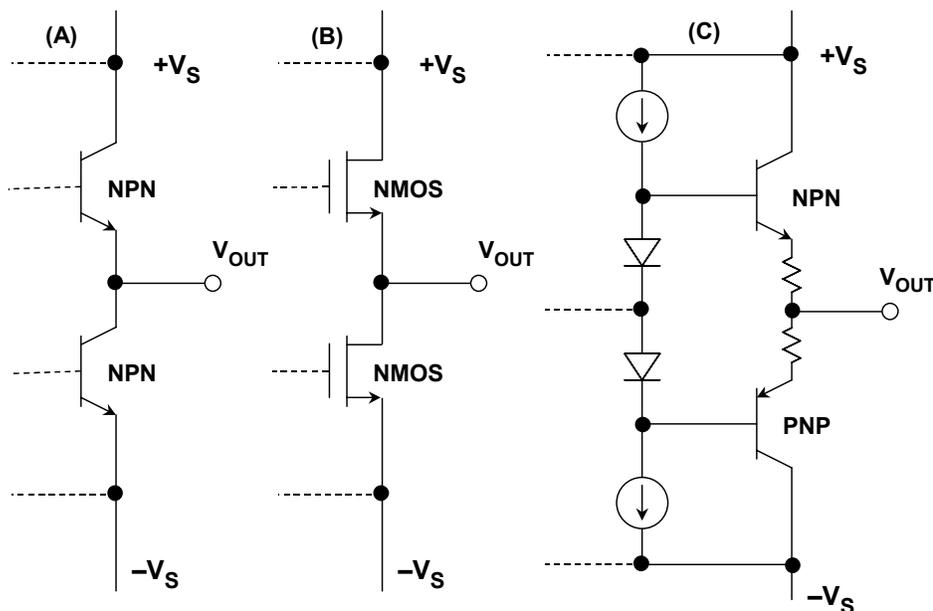
Figure 1-31: *Some traditional op amp output stages*

In many applications, the output is required to swing only to one rail, usually the negative rail (i.e., ground in single-supply systems). A pulldown resistor to the negative rail will allow the output to approach that rail (provided the load impedance is high enough, or is also grounded to that rail), but only slowly. Using an FET current source instead of a resistor can speed things up, but this adds complexity, as shown in Fig. 1-31B.

With modern complementary bipolar (CB) processes, well matched high speed PNP and NPN transistors are readily available. The complementary emitter follower output stage shown in Fig. 1-31C has many advantages, but the most outstanding one is the low output impedance. However, the output voltage of this stage can only swing within about one V_{BE} drop of either rail. Therefore an output swing of +1V to +4V is typical of such a stage, when operated on a single +5V supply.

The complementary common-emitter/common-source output stages shown in Figure 1-32A and B (opposite) allow the op amp output voltage to swing much closer to the rails, but these stages have much higher open-loop output impedance than do the emitter follower-based stages of Fig. 1-31C.

In practice, however, the amplifier's high open-loop gain and the applied feedback can still produce an application with low output impedance (particularly at frequencies below 10Hz). What should be carefully evaluated with this type of output stage is the loop gain within the application, with the load in place. Typically, the op amp will be specified for a minimum gain with a load resistance of 10kΩ (or more). Care should be taken that the application loading doesn't drop lower than the rated load, or gain accuracy may be lost.

It should also be noted these output stages can cause the op amp to be more sensitive to capacitive loading than the emitter-follower type. Again, this will be noted on the device data sheet, which will indicate a maximum of capacitive loading before overshoot or instability will be noted.

The complementary common emitter output stage using BJTs (Fig. 1-32A) cannot swing completely to the rails, but only to within the transistor saturation voltage (V_{CESAT}) of the rails. For small amounts of load current (less than 100μA), the saturation voltage may be as low as 5 to 10mV, but for higher load currents, the saturation voltage can increase to several hundred mV (for example, 500mV at 50mA).
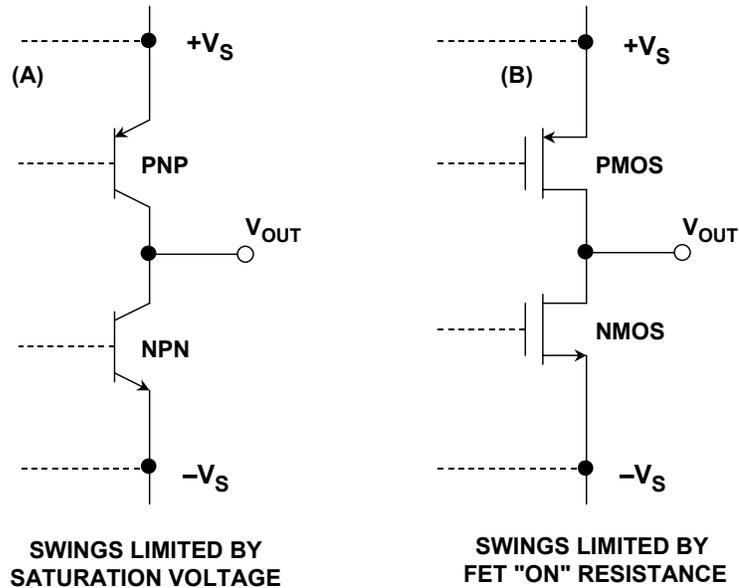
*Figure 1-32: "Almost" rail-to-rail output structures*

On the other hand, an output stage constructed of CMOS FETs (Fig. 1-32B) can provide nearly true rail-to-rail performance, but only under no-load conditions. If the op amp output must source or sink substantial current, the output voltage swing will be reduced by the I×R drop across the FETs internal "on" resistance. Typically this resistance will be on the order of 100Ω for precision amplifiers, but it can be less than 10Ω for high current drive CMOS amplifiers.

For the above basic reasons, it should be apparent that there is no such thing as a *true* rail-to-rail output stage, hence the caption of Fig. 1-32 ("Almost" Rail-to-Rail Output Structures). The best any op amp output stage can do is an almost rail-to-rail swing, when it is lightly loaded.

Op amps built on foundry CMOS processes have a primary advantage of low cost. Also, it is relatively straightforward to design rail-to-rail input and output stages with these CMOS devices, which will operate on low supply voltages.

Figure 1-33 below shows a simplified schematic of the AD8531/8532/8534 (single/dual/quad) op amp, which is typical of these design types. The AD8531/8532/8534 operates on a single 2.7V to 6.0V supply and can drive 250mA. Input offset voltage is 25mV maximum at +25°C, and voltage noise is 45nV/√Hz.
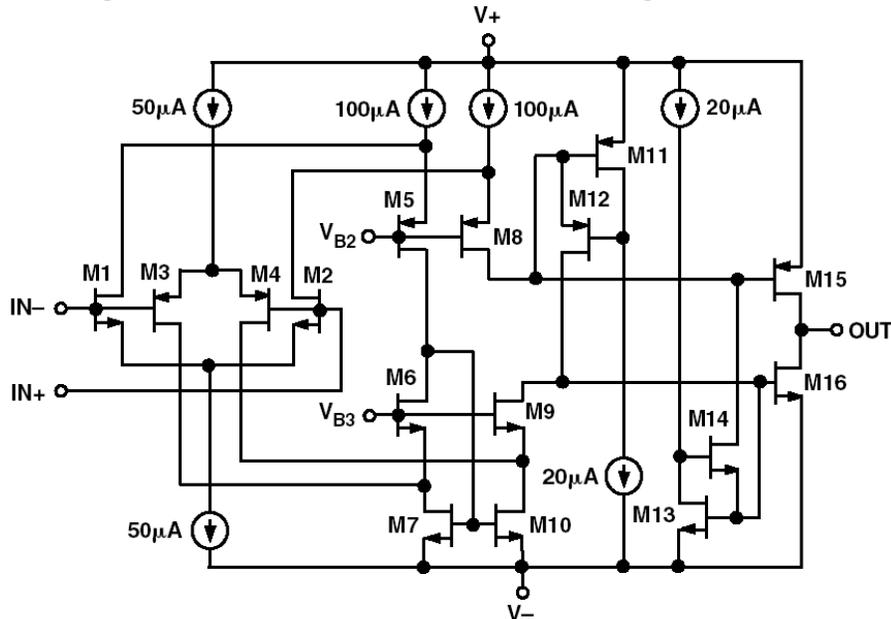
Figure 1-33: *AD8531/8532/8534 CMOS rail-to-rail op amp simplified schematic*

This type of op amp is simple and cost effective, and the lack of high DC precision is often no disadvantage. To the contrary, the high output drive available can be an overriding plus, particularly in AC-coupled applications.

Output Stage Surge Protection

Most low speed, high precision op amps generally have output stages which are protected against short circuits to ground or to either supply. Their output current is limited to a little more than 10mA. This has the additional advantage that it minimizes self-heating of the chip (and thus minimizes DC errors due to chip temperature differentials).

If an op amp is required to deliver both high precision and a large output current, it is advisable to use a separate output stage (within the loop) to minimize self-heating of the precision op amp. A simple buffer amplifier such as the BUF04, or a section of a non-precision op amp can be used.

Note that high speed op amps cannot have output currents limited to low values, as it would affect their slew rate and load drive ability. Thus most high speed op amps will source/sink between 50-100mA. Although many high speed op amps have internal protection for *momentary* shorts, their junction temperatures can be exceeded with sustained shorts. The user needs to be wary, and consult the specific device ratings.

Offset Voltage Trim Processes

The AD860x CMOS op amp family exploits the advantages of digital technology, so as to minimize the offset voltage normally associated with CMOS amplifiers. Offset voltage trimming is done after the devices are packaged. A digital code is entered into the device to adjust the offset voltage to less than 1mV, depending upon the grade. Wafer testing is not required, and the patented ADI technique called DigiTrim™ requires no extra pins to accomplish the function. These devices have rail-to-rail inputs and outputs (similar to Fig. 1-33), and the NMOS and PMOS parallel input stages are trimmed separately using DigiTrim to minimize the offset voltage in both pairs. A functional diagram of the AD8602 DigiTrim op amp is shown in Figure 1-34 below.
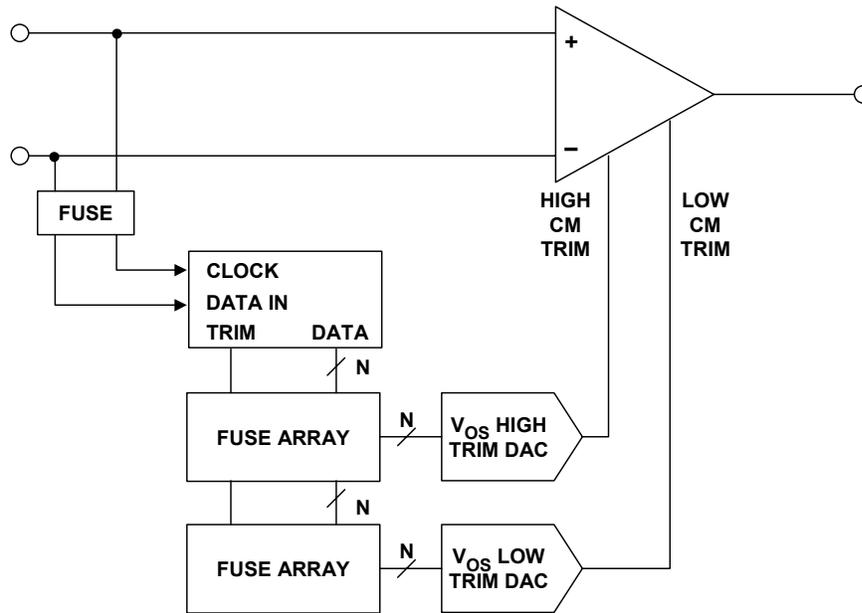
Figure 1-34: AD8602 (1/2) CMOS op amp showing DigiTrim™

DigiTrim adjusts the offset voltage by programming digitally weighted current sources. The trim information is entered through existing pins using a special digital sequence. The adjustment values can be temporarily programmed, evaluated, and readjusted for optimum accuracy before permanent adjustment is performed. After the trim is completed, the trim circuit is locked out to prevent the possibility of any accidental re-trimming by the end user.

The physical trimming, achieved by blowing polysilicon fuses, is very reliable. No extra pads or pins are required, and no special test equipment is needed to perform the trimming. The trims can be done after packaging so that assembly-related shifts can be eliminated. No testing is required at the wafer level because of high die yields.

The first devices to use this new technique are the Analog Devices' AD8601/02/04 (single, dual, quad) rail-to-rail CMOS amplifiers. The offset is trimmed for both high and low common-mode conditions so that the offset voltage is under 500μV over the full common-mode input voltage range. The bandwidth of the op amps is 8MHz, slew rate is 5V/μs, and supply current is only 640μA per amplifier.

At this point it is useful to review the other popular trim methods. Analog Devices pioneered the use of thin film resistors and laser wafer trimming for precision amplifiers, references, data converters, and other linear ICs (see Reference 5). Up to 16-bit accuracy can be achieved with trimming, and the thin film resistors themselves are very stable with temperature and can add to the thermal stability and accuracy of a device, even without trimming. Thin film deposition and patterning are processes that must be tightly controlled. The laser trimming systems are also quite expensive. In-package trimming is not possible, so assembly-related shifts cannot be easily compensated. Nevertheless, thin film trimming at the wafer level provides continuous fine trim resolution in precision integrated circuits where high accuracy and stability are required.

Zener zapping uses a voltage to create a metallic short circuit across the base-emitter junction of a transistor to remove a circuit element (see References 4 and 6). The base-emitter junction is commonly referred to as a zener, although the mechanism is actually avalanche breakdown of the junction. During the avalanche breakdown across the base-emitter junction, the very high current densities and localized heating generate rapid metal migration between the base and emitter connections, leading to a metallic short across the junction. With proper biasing (current, voltage, and time), this short will have a very low resistance value. If a series of these base-emitter junctions are arranged in parallel with a string of resistors, zapping selected junctions will short out portions of the resistor string, thereby adjusting the total resistance value.

It is possible to perform zener zap trimming in the packaged IC to compensate for assembly-related shifts in the offset voltage. However, trimming in the package requires extra package pins. Alternately, trimming at the wafer level requires additional probe pads. Probe pads do not scale effectively as the process features shrink. So, the die area required for trimming is relatively constant regardless of the process geometries. Some form of bipolar transistor is required for the trim structures, therefore a purely MOS-based process may not have zener zap capability. The nature of the trims is discrete since each zap removes a predefined resistance value. Increasing trim resolution requires additional transistors and pads or pins, which rapidly increase the total die area and/or package cost. This technique is most cost-effective for fairly large-geometry processes where the trim structures and probe pads make up a relatively small percentage of the overall die area.

It was in the process of creating the industry standard OP07 in 1975 that Precision Monolithics Incorporated pioneered zener zap trimming (Reference 6, again). The OP07 and other similar parts must be able to operate from over ±15V supplies. As a result, they utilize relatively large device geometries to support the high voltage requirements, and extra probe pads don't significantly increase die area.

Link trimming is the cutting of metal or poly-silicon links to remove a connection. In link trimming, either a laser or a high current is used to destroy a "shorted" connection across a parallel resistive element. Removing the connection increases the effective resistance of the combined element(s). Laser cutting works similar to laser trimming of thin films. The high local heat from the laser beam causes material changes that lead to a non-conductive area, effectively cutting a metal or conductive polysilicon connector.

The high-current link trim method works as an inverse to zener zapping—the conductive connection is destroyed, rather than created by a zener-zap.

Link trim structures tend to be somewhat more compact than laser trimmed resistor structures. No special processes are required in general, although the process may have to be tailored to the laser characteristics if laser cutting is used. With the high-current trimming method, testing at the wafer level may not be required if die yields are good. The laser cutting scheme doesn't require extra contact pads, but the trim structures don't scale with the process feature sizes. Laser cutting of links cannot be performed in the package, and requires additional probe pads on the die. In addition, it can require extra package pins for in-package high-current trims. Like zener zapping, link trimming is discrete. Resolution improvements require additional structures, increasing area and cost.

PROCESS	TRIMMED AT:	SPECIAL PROCESSING	RESOLUTION
DigiTrim™	Wafer or Final Test	None	Discrete
Laser Trim	Wafer	Thin Film Resistor	Continuous
Zener Zap Trim	Wafer	None	Discrete
Link Trim	Wafer	Thin Film or Poly Resistor	Discrete
EEPROM Trim	Wafer or Final Test	EEPROM	Discrete

Figure 1-35: Summary of ADI trim processes

EEPROM trimming utilizes special, non-volatile digital memory to store trim data. The stored data bits control adjustment currents through on-chip D/A converters. Memory cells and D/A converters scale with the process feature size. In-package trimming and even trimming in the customer's system is possible so that assembly-related shifts can be trimmed out. Testing at the wafer level is not required if yields are reasonable. No special hardware is required for the trimming beyond the normal mixed-signal tester system, although test software development may be more complicated. Since the trims can be overwritten, it is possible to periodically reprogram the system to account for long-term drifts or to modify system characteristics for new requirements. The number of reprogram cycles possible depends on the process, and is finite. Most EEPROM processes provide enough rewrite cycles to handle routine re-calibration.

This trim method does require special processing. Stored trim data can be lost under certain conditions, especially at high operating temperatures. At least one extra digital contact pad/package pin is required to input the trim data to the on-chip memory. This technique is only available on MOS-based processes due to the very thin oxide requirements. The biggest drawback is that the on-chip D/A converters are large—often larger than the amplifier circuits they are adjusting. For this reason, EEPROM trimming is mostly used for data converter or system-level products where the trim D/A converters represent a much smaller percentage of the overall die area.

Figure 1-35 above summarizes the key features of each ADI trim method. It can be seen from that all trim methods have their respective places in producing high performance linear integrated circuits.

1.49

Op Amp Process Technologies

The wide variety of op amp processes is shown in Figure 1-36 below. The early 1960's op amps used standard NPN-based bipolar processes. The PNP transistors of these processes were extremely slow and were used primarily for current sources and level shifting.

The ability to produce matching high speed PNP transistors on a bipolar process added great flexibility to op amp circuit designs. The first p-epi complementary bipolar (CB) process was introduced by ADI in the mid-1980s. The f_ts of the PNP and NPN transistors were approximately 700MHz and 900MHz, respectively, and had 30V breakdowns. Since its original introduction in 1985, several additional CB processes have been developed at ADI designed for higher speeds and lower breakdowns. For example, a current 5V CB process has 9GHZ PNPs and 16GHz NPNs. These CB processes are used in today's precision op amps, as well as those requiring wide bandwidths.

- ◆ **BIPOLAR (NPN-BASED): This is Where it All Started!!**

- ◆ **COMPLEMENTARY BIPOLAR (CB): Rail-to-Rail, Precision, High Speed**

- ◆ **BIPOLAR + JFET (BiFET): High Input Impedance, High Speed**

- ◆ **COMPLEMENTARY BIPOLAR + JFET (CBFET): High Input Impedance, Rail-to-Rail Output, High Speed**

- ◆ **COMPLEMENTARY MOSFET (CMOS): Low Cost Op Amps (ADI DigiTrim™ Minimizes Offset Voltage and Drift in CMOS op amps)**

- ◆ **BIPOLAR (NPN) + CMOS (BiCMOS): Bipolar Input Stage adds Linearity, Low Power, Rail-to-Rail Output**

- ◆ **COMPLEMENTARY BIPOLAR + CMOS (CBCMOS): Rail-to-Rail Inputs, Rail-to-Rail Outputs, Good Linearity, Low Power, Higher Cost**

Figure 1-36: Op amp process technology summary

The JFETs available on the Analog Devices' complementary bipolar processes allow high input impedance op amps to be designed suitable for such applications as photodiode or electrometer preamplifiers. These processes are sometimes designated as *CBFET*.

CMOS op amps, generally have higher offset voltages and offset voltage drift than trimmed bipolar or BiFET op amps, however the Analog Devices' DigiTrim™ process described above yields low offset voltage, while keeping costs low. Voltage noise for CMOS op amps tends to be larger, however, the input bias current is very low. They offer low power and cost (foundry CMOS processes are typically used).

The addition of bipolar or complementary devices to a CMOS process (BiMOS or CBCMOS) adds greater flexibility, better linearity, and low power as well as additional cost. The bipolar devices are typically used for the input stage to provide good gain and linearity, and CMOS devices for the rail-to-rail output stage.

In summary, there is no single IC process which is optimum for all op amps. Process selection and the resulting op amp design depends on the targeted applications and ultimately should be transparent to the customer.

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ACKNOWLEDGEMENTS:

NOTES:

SECTION 1-4: OP AMP SPECIFICATIONS
Walt Kester, Walt Jung, James Bryant

In this section, basic op amp specifications are discussed. The importance of any given specification depends of course upon the application. For instance offset voltage, offset voltage drift, and open-loop gain are very critical in precision sensor signal conditioning circuits, but not as important in high speed applications where bandwidth, slew rate, and distortion are the key specifications.

Most op amp specifications are largely topology independent. However, although voltage feedback and current feedback op amps have similar error terms and specifications, the application of each part warrants discussing some of the specifications separately. In the following discussions, this will be done where significant differences exist.

Input Offset Voltage, V_{OS}

Ideally, if both inputs of an op amp are at exactly the same voltage, then the output should be at zero volts. In practice, a small differential voltage must be applied to the inputs to force the output to zero. This is known as the *input offset voltage*, V_{OS}.
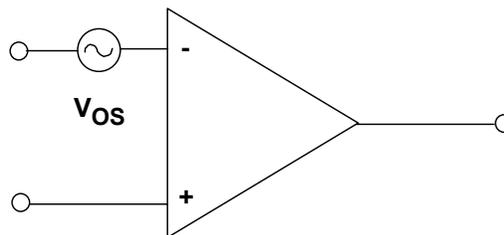
◆ **Offset Voltage: The differential voltage which must be applied to the input of an op amp to produce zero output.**

◆ **Ranges:**

- **Chopper Stabilized Op Amps:**   **<1µV**
- **General Purpose Precision Op Amps:**   **50-500µV**
- **Best Bipolar Op Amps:**   **10-25µV**
- **Best FET Op Amps:**   **100-1,000µV**
- **High Speed Op Amps:**   **100-2,000µV**
- **Untrimmed CMOS Op Amps:**   **5,000-50,000µV**
- **DigiTrim™ CMOS Op Amps:**   **<1,000µV**
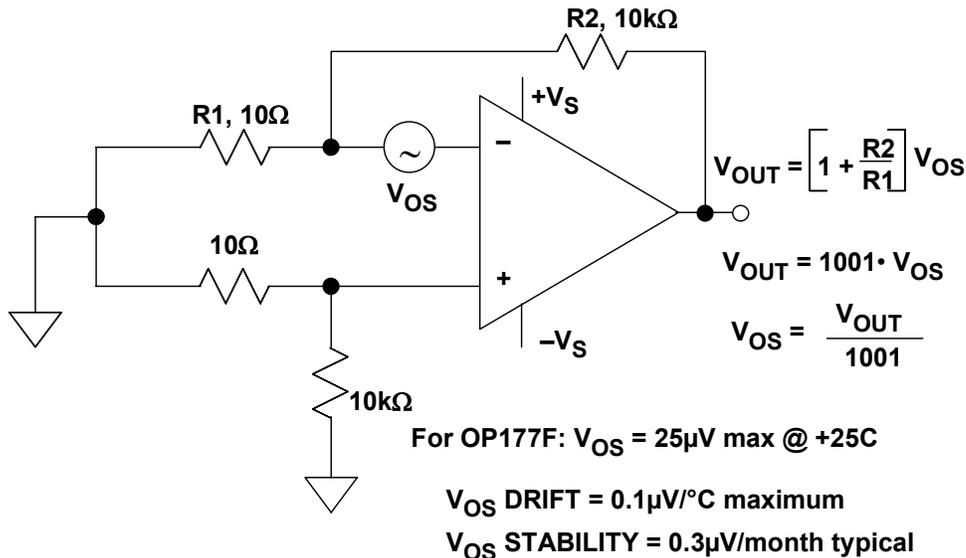
Figure 1-37: Input offset voltage

Input offset voltage is modeled as a voltage source, V_{OS}, in series with the inverting input terminal of the op amp as shown in Figure 1-37 above. The corresponding output offset voltage (due to V_{OS}) is obtained by multiplying the input offset voltage by the DC noise gain of the circuit (see Fig. 1-3 and Eq. 1-2, again).

Chopper stabilized op amps have a V_{OS} which is less than 1μV (AD8551 series), and the best precision bipolar op amps (super-beta or bias stabilized) can have offsets as low as 25μV (OP177F). The very best trimmed FET types have about 100μV of offset (AD8610B), and untrimmed CMOS op amps can range from 5 to 50mV. However, the ADI DigiTrim™ CMOS op amps have offset voltages less than 1mV (AD8605). Generally speaking, "precision" op amps will have $V_{OS} < 0.5$mV, although some high speed amplifiers may be a little worse than this.

Measuring input offset voltages of a few microvolts requires that the test circuit does not introduce more error than the offset voltage itself. Figure 1-38 below shows a standard circuit for measuring offset voltage. The circuit amplifies the input offset voltage by the noise gain of 1001. The measurement is made at the amplifier output using an accurate digital voltmeter. The offset referred to the input (RTI) is calculated by dividing the output voltage by the noise gain. The small source resistance seen by the inputs results in negligible bias current contribution to the measured offset voltage. For example, 2nA bias current flowing through the 10Ω resistor produces a 0.02μV error referred to the input.

Figure 1-38: *Measuring input offset voltage*

As simple as this circuit looks, it can give inaccurate results when testing precision op amps, unless care is taken in implementation. The largest potential error source comes from parasitic thermocouple junctions, formed where two different metals are joined. This thermocouple voltage can range from 2μV/°C to more than 40μV/°C. Note that in this circuit additional "dummy" resistors have been added to the non-inverting input, in order to exactly match/balance the thermocouple junctions in the inverting input path.

The accuracy of the measurement also depends on the mechanical layout of the components and exactly how they are placed on the PC board. Keep in mind that the two connections of a component such as a resistor create two equal, but opposite polarity thermoelectric voltages (assuming they are connected to the same metal, such as the copper trace on a PC board). These will cancel each other, *assuming both are at exactly the same temperature*. Clean connections and short lead lengths help to minimize

temperature gradients and increase the accuracy of the measurement. Note— see the Chapter 7 discussions on this general topic for more detail.

In the test circuit, airflow should be minimal so that all the thermocouple junctions stabilize at the same temperature. In some cases, the circuit should be placed in a small closed container to eliminate the effects of external air currents. The circuit should be placed flat on a surface so that convection currents flow up and off the top of the board, not across the components, as would be the case if the board were mounted vertically.

Measuring the offset voltage shift over temperature is an even more demanding challenge. Placing the printed circuit board containing the amplifier being tested in a small box or plastic bag with foam insulation prevents the temperature chamber air current from causing thermal gradients across the parasitic thermocouples. If cold testing is required, a dry nitrogen purge is recommended. Localized temperature cycling of the amplifier itself using a Thermostream-type heater/cooler may be an alternative, however these units tend to generate quite a bit of airflow that can be troublesome.
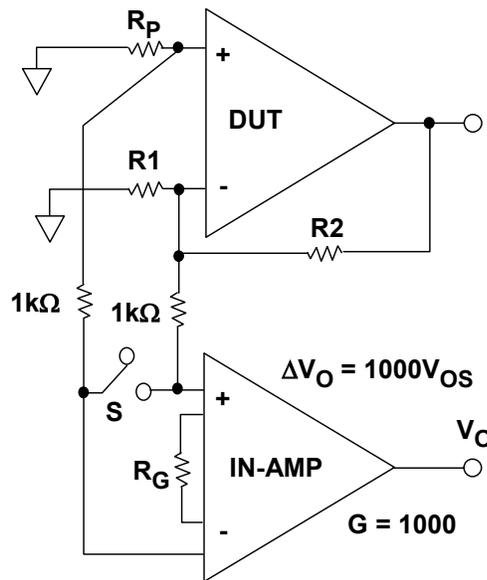
Figure 1-39: Alternate input offset voltage measurement using an in-amp

Generally, the test circuit of Fig. 1-38 can be made to work for many amplifiers. Low absolute values for the small resistors (such as 10Ω) will minimize bias current induced errors. An alternate V_{OS} measurement method is shown in Fig. 1-39, and is suitable for cases of high and/or unequal bias currents (as in the case of current feedback op amps).

In this measurement method, an in-amp is connected to the op amp input terminals through isolation resistors, and provides the gain for the measurement. The offset voltage of the in-amp (measured with S closed) must then be subtracted from the final V_{OS} measurement. Also, the circuit shown below in Figure 1-44 for measuring input bias currents can also be used to measure input offset voltage independent of bias currents.

Offset Adjustment (Internal Method)

Many single op amps have pins available for optional offset null. To make use of this feature, two pins are joined by a potentiometer, and the wiper goes to one of the supplies through a resistor, as shown generally in Figure 1-40 below. Note that if the wiper is accidentally connected to the wrong supply, the op amp will probably be destroyed— this is a common problem, when one op amp type is replaced by another. The range of offset adjustment in a well-designed op amp is no more than two or three times the maximum V_{OS} of the lowest grade device, in order to minimize sensitivity. Nevertheless, the voltage gain of an op amp at its offset adjustment pins may actually be greater than the gain at its signal inputs! It is therefore very important to keep these pins noise-free. Note that it is *never* advisable to use long leads from an op amp to a remote nulling potentiometer.
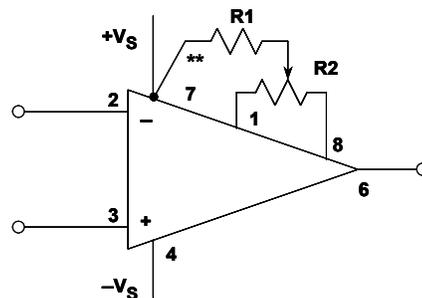
◆ ** Wiper connection may be to either +V_S or –V_S depending on op amp

◆ R values depend on op amp. Consult data sheet

◆ Use to null out input offset voltage, <u>not</u> system offsets!

◆ There may be high gain from offset pins to output — Keep them quiet!

◆ Nulling offset causes increase in offset temperature coefficient, approximately 4μV/°C for 1mV offset null for FET inputs

Figure 1-40: Offset adjustment pins

As was mentioned above, the offset drift of an op amp with temperature will vary with the setting of its offset adjustment. The internal adjustment terminals should therefore be used only to adjust the op amp's own offset, *not to correct any system offset errors*, since doing so would be at the expense of increased temperature drift. The drift penalty for a FET input op amp is in the order of 4μV/°C for each millivolt of nulled offset voltage. It is generally better to control offset voltage by proper device/grade selection.

Offset Adjustment (External Methods)

If an op amp doesn't have offset adjustment pins (popular duals and all quads do not), and it is still necessary to adjust the amplifier and system offsets, an external method can be used. This method is also most useful if the offset adjustment is to be done with a system programmable voltage, such as a DAC.

With an inverting op amp configuration, injecting current into the inverting input is the simplest method, as shown in Figure 1-41A (opposite). The disadvantage of this method is that there is some increase in noise gain possible, due to the parallel path of R3 and the

potentiometer resistance. The resulting increase in noise gain may be reduced by making $\pm V_R$ large enough so that the R3 value is much greater than R1||R2. Note that if the power supplies are stable and noise-free, they can be used as $\pm V_R$.
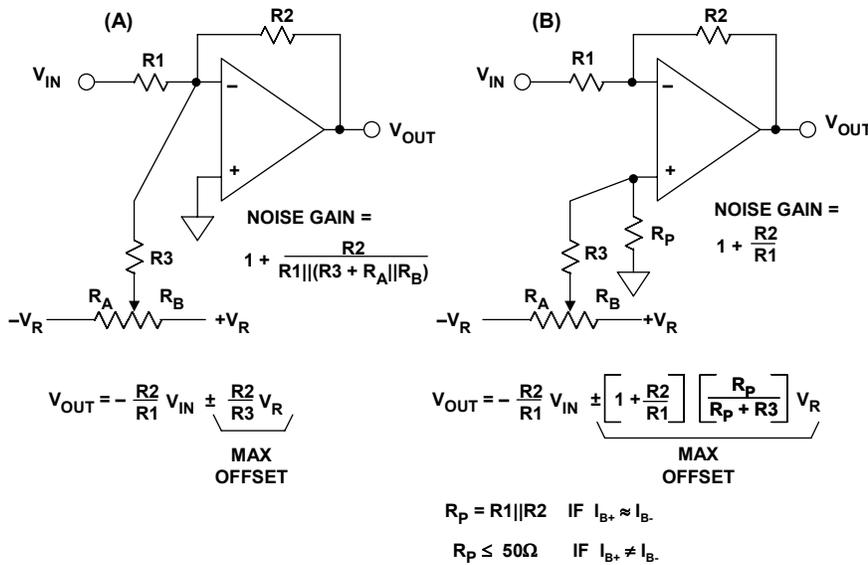
Figure 1-41: *Inverting op amp external offset trim methods*

Fig. 1-41B shows how to implement offset trim by injecting a small offset voltage into the non-inverting input. This circuit is preferred over 1-41A, as it results in no noise gain increase (but it requires adding R_P). If the op amp has matched input bias currents, then R_P should equal R1|| R2 (to minimize the added offset voltage). Otherwise, R_P should be less than 50Ω. For higher values, it may be advisable to bypass R_P at high frequencies.
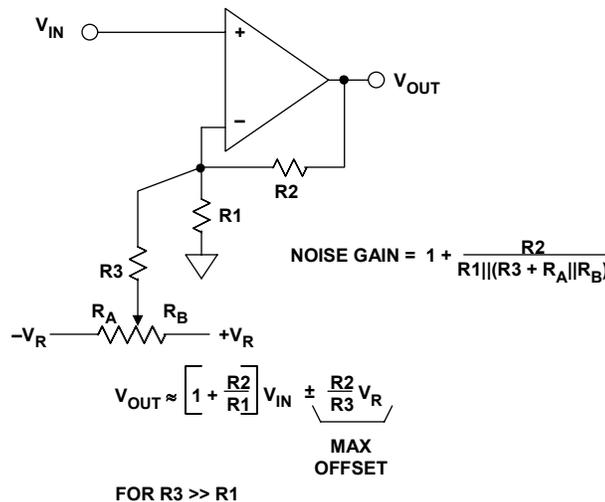
Figure 1-42: *Non-inverting op amp external offset trim methods*

The circuit shown in Figure 1-42 above can be used to inject a small offset voltage when using an op amp in the non-inverting mode. This circuit works well for small offsets, where R3 can be made much greater than R1. Note that otherwise, the signal gain might be affected as the offset potentiometer is adjusted. The gain may be stabilized, however, if R3 is connected to a fixed low impedance reference voltage sources, $\pm V_R$.

**1.57**

Input Offset Voltage Drift and Aging Effects

Input offset voltage varies with temperature, and its temperature coefficient is known as TCV_{OS}, or more commonly, *drift*. As we have mentioned, offset drift is affected by offset adjustments to the op amp, but when it has been minimized, it may be as low as 0.1μV/°C (typical value for OP177F). More typical drift values for a range of general purpose precision op amps lie in the range 1-10μV/°C. Most op amps have a specified value of TCV_{OS}, but some, instead, have a second value of maximum V_{OS} that is guaranteed over the operating temperature range. Such a specification is less useful, because there is no guarantee that TCV_{OS} is constant or monotonic.

The offset voltage also changes as time passes, or *ages*. Aging is generally specified in μV/month or μV/1000 hours, but this can be misleading. Since aging is a "drunkard's walk" phenomenon it is proportional to the *square root* of the elapsed time. An aging rate of 1μV/1000 hour therefore becomes about 3μV/year (not 9μV/year).

Long-term stability of the OP177F is approximately 0.3μV/month. This refers to a time period *after* the first 30 days of operation. Excluding the initial hour of operation, changes in the offset voltage of these devices during the first 30 days of operation are typically less than 2μV.

Input Bias Current, I_B

Ideally, no current flows into the input terminals of an op amp. In practice, there is always two *input bias currents*, I_{B+} and I_{B-} (see Figure 1-43 below).
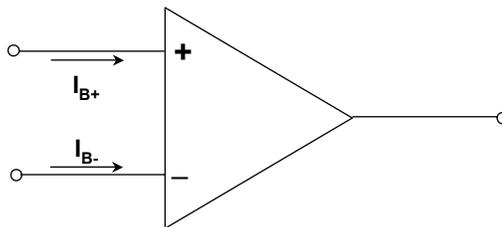

◆ **A very variable parameter!**

◆ **I_B can vary from 60 fA (1 electron every 3 μs) to many μA, depending on the device.**

◆ **Some structures have well-matched I_B, others do not.**

◆ **Some structures' I_B varies little with temperature, but a FET op amp's I_B doubles with every 10°C rise in temperature.**

◆ **Some structures have I_B which may flow in either direction.**

Figure 1-43: Op amp input bias current

Values of I_B range from 60fA (about one electron every three microseconds) in the AD549 electrometer, to tens of microamperes in some high speed op amps. Op amps with simple input structures using BJT or FET long-tailed pair have bias currents that flow in one direction. More complex input structures (bias-compensated and current feedback op amps) may have bias currents that are the difference between two or more internal current sources, and may flow in either direction.

Bias current is a problem to the op amp user because it flows in external impedances and produces voltages, which add to system errors. Consider a non-inverting unity gain buffer driven from a source impedance of 1MΩ. If I_B is 10nA, it will introduce an additional 10mV of error. This degree of error is not trivial in any system.

Or, if the designer simply forgets about I_B and uses capacitive coupling, the circuit won't work— at all! Or, if I_B is low enough, it may work momentarily while the capacitor charges, giving even more misleading results. The moral here is not to neglect the effects of I_B, in any op amp circuit. The same admonition goes for in-amp circuits.

$R_S \gg 100\Omega$ (100kΩ TO 1GΩ)
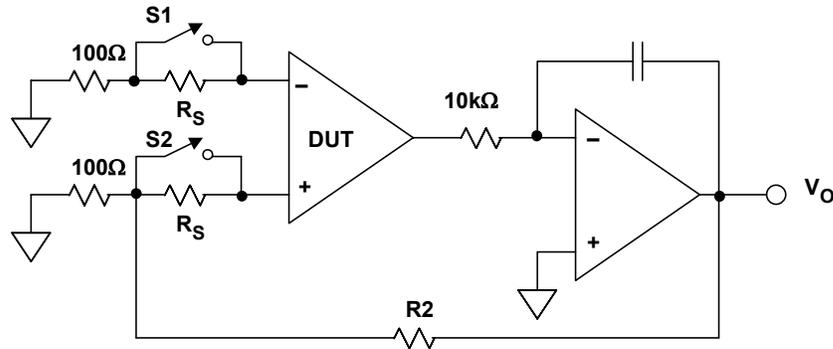
S1 CLOSED TO TEST I_{B+}

S2 CLOSED TO TEST I_{B-}

BOTH CLOSED TO TEST V_{OS}

BOTH OPEN TO TEST I_{OS}

$$V_O = \left[1 + \frac{R2}{100} \right] V_{OS}$$

$$+ \left[1 + \frac{R2}{100} \right] I_{B+}R_S$$

$$- \left[1 + \frac{R2}{100} \right] I_{B-}R_S$$
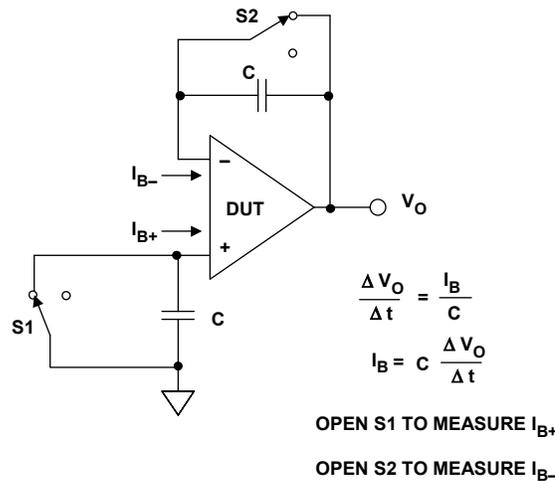
Figure 1-44: Measuring input bias current

Input bias current (or input offset voltage) may be measured using the test circuit of Figure 1-44 above. To measure I_B, a large resistance, R_S, is inserted in series with the input under test, creating an apparent additional offset voltage equal to $I_B \times R_S$. If the actual V_{OS} has previously been measured and recorded, the change in apparent V_{OS} due to the change in R_S can be determined, and I_B is then easily computed. This yields values for I_{B+} and I_{B-}. The rated value of I_B is the average of the two currents, or $I_B = (I_{B+} + I_{B-})/2$.

The *input offset current,* I_{OS}, may also be calculated, by taking the difference between I_{B-} and I_{B+}, or $I_{OS} = I_{B+} - I_{B-}$. Typical useful R_S values vary from 100kΩ for bipolar op amps to 1000MΩ for some FET input devices.

Note also that I_{OS} is only meaningful where the two individual bias currents are fundamentally reasonably well-matched, to begin with. This is true for most VFB op amps. However, it wouldn't for example be meaningful to speak of I_{OS} for a CFB op amp, as the currents are radically un-matched.

Extremely low input bias currents must be measured by integration techniques. The bias current in question is used to charge a capacitor, and the rate of voltage change is measured. If the capacitor and general circuit leakage is negligible (this is very difficult for currents under 10fA), the current may be calculated directly from the rate of change of the output of the test circuit. Figure 1-45 below illustrates the general concept. With one switch open and the opposite closed, either I_{B+} or I_{B-} is measured.


$$\frac{\Delta V_O}{\Delta t} = \frac{I_B}{C}$$

$$I_B = C \frac{\Delta V_O}{\Delta t}$$

OPEN S1 TO MEASURE I_{B+}

OPEN S2 TO MEASURE I_{B-}

Figure 1-45: *Measuring very low bias currents*

It should be obvious that only a premium capacitor dielectric can be used for C, for example Teflon or polypropylene types.

Canceling the Effects of Bias Current (External to the Op Amp)

When the bias currents of an op amp are well matched (the case with simple bipolar op amps, but *not* internally bias compensated ones, as noted previously), a bias compensation resistor, R3, (R3=R1‖R2) introduces a voltage drop in the non-inverting input to match and thus compensate the drop in the parallel combination of R1 and R2 in the inverting input. This minimizes additional offset voltage error, as in Figure 1-46.


$$V_O = R2 (I_{B-} - I_{B+})$$

$$= R2\, I_{OS}$$

$$= 0, \text{ IF } I_{B+} = I_{B-}$$

NEGLECTING V_{OS}
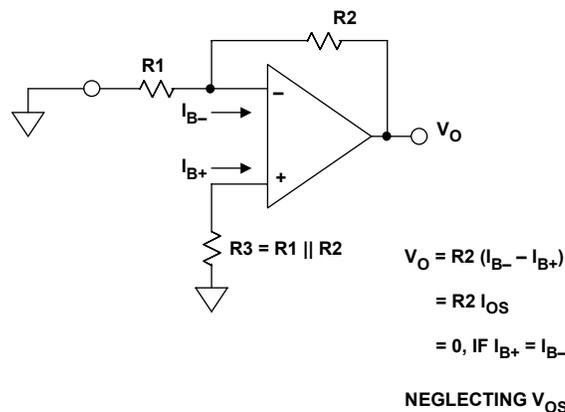
Figure 1-46: *Canceling the effects of input bias current within an application*

Note that if R3 is more than 1kΩ or so, it should be bypassed with a capacitor to prevent noise pickup. Also note that this form of bias cancellation is useless where bias currents are not well-matched, and will, in fact, make matters worse.

1.60

Calculating Total Output Offset Error Due to I_B and V_{OS}

The equations shown in Figure 1-47 below are useful in referring all the offset voltage and induced offset voltage from bias current errors to the either the input (RTI) or the output (RTO) of the op amp. The choice of RTI or RTO is a matter of preference.
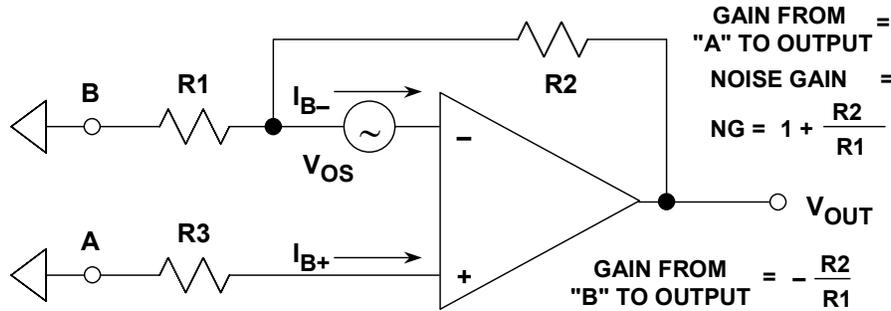
- OFFSET (RTO) $= V_{OS} \left[1 + \dfrac{R2}{R1} \right] + I_{B+} \cdot R3 \left[1 + \dfrac{R2}{R1} \right] - I_{B-} \cdot R2$

- OFFSET (RTI) $= V_{OS} + I_{B+} \cdot R3 - I_{B-} \left[\dfrac{R1 \cdot R2}{R1 + R2} \right]$

FOR BIAS CURRENT CANCELLATION:

OFFSET (RTI) $= V_{OS}$ IF $I_{B+} = I_{B-}$ AND $R3 = \dfrac{R1 \cdot R2}{R1 + R2}$

Figure 1-47: *Op amp total offset voltage model*

The RTI value is useful in comparing the cumulative op amp offset error to the input signal. The RTO value is more useful if the op amp drives additional circuitry, to compare the net errors with that of the next stage.

In any case, the RTO value is simply obtained by multiplying the RTI value by the stage noise gain, which is $1 + R2/R1$.

Before departing the topic of offset errors, some simple rules towards minimization might bear repetition:

- Keep input/feedback resistance values low, to minimize offset voltage due to bias current effects.
- Use a bias compensation resistance with VFB op amps *not* using internal bias compensation. Bypass this resistance, for lowest noise pickup.
- If a VFB op amp *does* use internal bias current compensation, *don't* use the compensation resistance.
- When necessary, use *external* offset trim networks, for lowest induced drift.
- Select an appropriate precision op amp specified for low offset and drift, as opposed to trimming.
- For high performance, low drift circuitry, watch out for thermocouple effects and used balanced, low thermal error layouts.
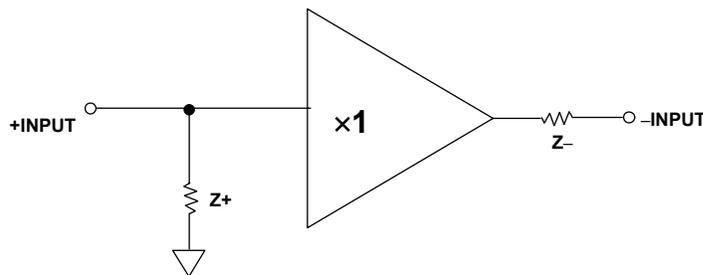
Input Impedance

VFB op amps normally have both differential and common-mode input impedances specified. Current feedback op amps normally specify the impedance to ground at each input. Different models may be used for different voltage feedback op amps, but in the absence of other information, it is usually safe to use the model in Figure 1-48 below. In this model the bias currents flow into the inputs from infinite impedance current sources.
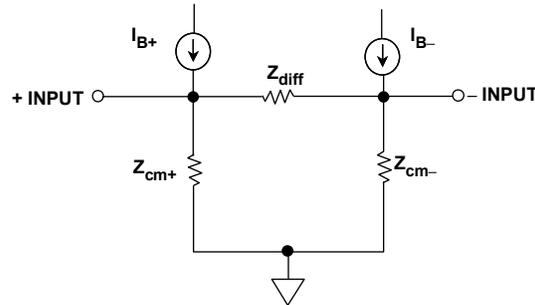
◆ Z_{cm+} and Z_{cm-} are the common-mode input impedance. The figure on the data sheet is for one, not both, but they are approximately equal. Z_{diff} is the differential input impedance.

◆ They are high resistance (10^5 - $10^{12}\Omega$) in parallel with a small shunt capacitance (sometimes as high as 25pF).

◆ In most practical circuits, Z_{cm-} is swamped by negative feedback.

Figure 1-48: *Input impedance (voltage feedback op amp)*

The common-mode input impedance data sheet specification (Z_{cm+} and Z_{cm-}) is the impedance from either input to ground (NOT from both to ground). The differential input impedance (Z_{diff}) is the impedance between the two inputs. These impedances are usually resistive and high (10^5-$10^{12}\Omega$) with some shunt capacitance (generally a few pF, sometimes 20-25 pF). In most op amp circuits, the inverting input impedance is reduced to a very low value by negative feedback, and only Z_{cm+} and Z_{diff} are of importance.

◆ Z+ is high resistance (10^5 - $10^9\Omega$) with little shunt capacitance.

◆ Z- is low and may be reactive (L or C). The resistive component is 10-100Ω.

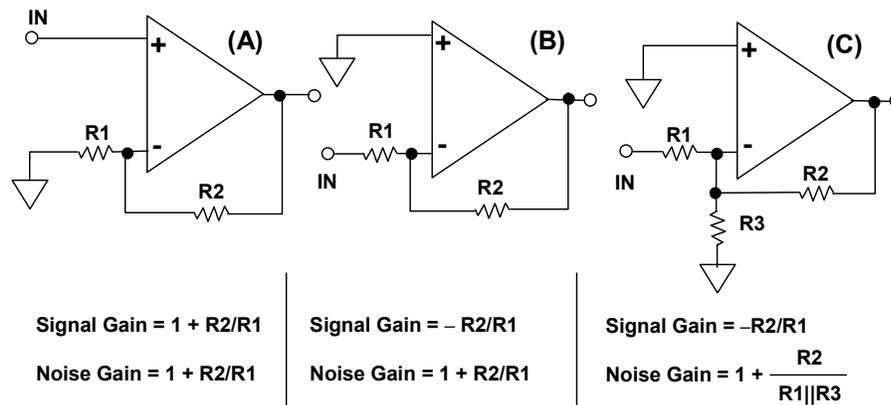***Figure 1-49:*** *Input impedance (current feedback op amp)*

A current feedback op amp is even more simple, as shown in Figure 1-49 above. Z+ is resistive, generally with some shunt capacitance, and high (10^5-$10^9\Omega$) while Z– is reactive (L or C, depending on the device) but has a resistive component of 10-100Ω, varying from type to type.

1.62

Manipulating Op Amp Noise Gain and Signal Gain

Consider an op amp and two resistors, R1 and R2, arranged as shown in the series of figures of Figure 1-50 below. Note that R1 and R2 need not be resistors; they could also be complex impedances, Z1 and Z2.

If we ground R1 and apply a signal to the non-inverting input, we see a signal gain of $1 + R2/R1$, as in Fig. 1-50A. If we ground the non-inverting input and apply the signal to R1, we see a signal gain of $-R2/R1$, as in Fig. 1-50B. In both cases, the voltage noise of the op amp itself (as well as the input offset voltage) sees a gain of $1 + R2/R1$, i.e., the *noise gain* of the op amp, as discussed earlier in this chapter.

This discussion is aimed at making the point that a stage's noise gain and signal gain *need not necessarily be equal*. Some times it can be to the user's advantage to manipulate them, so as to be somewhat independent of one another.

Signal Gain = 1 + R2/R1	Signal Gain = – R2/R1	Signal Gain = –R2/R1
Noise Gain = 1 + R2/R1	Noise Gain = 1 + R2/R1	Noise Gain = $1 + \dfrac{R2}{R1\|R3}$

◆ **Voltage Noise and Offset Voltage of the op amp are reflected to the output by the Noise Gain.**

◆ **Noise Gain, not Signal Gain, is relevant in assessing stability.**

◆ **Circuit C has unchanged Signal Gain, but higher Noise Gain, thus better stability, worse noise, and higher output offset voltage.**

Figure 1-50: Manipulating op amp noise gain and signal gain

But, importantly, *it is the noise gain that is relevant in assessing stability*. It is sometimes possible to alter the noise gain, while leaving signal gain unaffected. When this is done, a marginally stable op amp stage can sometimes be made stable, with the same signal gain.

For example, consider the inverting amplifier of Fig. 1-50B. If we add a third resistor to Fig. 1-50B, it becomes Fig. 1-50C. This dummy resistor R3, from the inverting input to ground, increases the noise gain to $1 + R2/(R1\|R3)$. But, note the signal gain is unaffected; that is it is still $-R2/R1$.

This provides a means of stabilizing an unstable inverting amplifier— at a cost of worse signal-to-noise ratio, less loop gain, and increased sensitivity to input offset voltage. Nevertheless, it is still a sometimes useful trick.

Open-Loop Gain And Open-Loop Gain Nonlinearity

Open-loop voltage gain, usually called A_{VOL} (sometimes simply A_V), for most VFB op amps is quite high. Common values are 100,000 to 1,000,000, and 10 or 100 times these figures for high precision parts. Some fast op amps have appreciably lower open-loop gain, but gains of less than a few thousand are unsatisfactory for high accuracy use. Note also that open-loop gain isn't highly stable with temperature, and can vary quite widely from device to device of the same type, so it is important that it be reasonably high.

Since a voltage feedback op amp operates as voltage in/voltage out, its open-loop gain is a dimensionless ratio, so no unit is necessary. However, data sheets sometimes express gain in V/mV or V/μV instead of V/V, for the convenience of using smaller numbers. Or, voltage gain can also be expressed in dB terms, as gain in dB = $20 \times \log A_{VOL}$. Thus an open-loop gain of 1V/μV is equivalent to 120dB, and so on.

CFB op amps have a current input and a voltage output, so their open-loop *transimpedance gain* is expressed in volts per ampere or ohms (or kΩ or MΩ). Values usually lie between hundreds of kΩ and tens of MΩ.

From basic feedback theory, it is understood that in order to maintain accuracy, a precision amplifier's DC open-loop gain, A_{VOL}, should be high. This can be seen by examining the closed-loop gain equation, including errors due to finite gain. The expression for closed loop gain with a finite gain error is:

$$G_{CL} = \frac{1}{\beta} \bullet \left[\frac{1}{1 + \dfrac{1}{A_{VOL}\beta}} \right]$$

Eq. 1-15A

Since noise gain is equal to $1/\beta$, there are alternate forms of this expression. Combining the two right side terms and using the NG expression, an alternate one is:

$$G_{CL} = \frac{NG}{1 + \dfrac{NG}{A_{VOL}}}$$

Eq. 1-15B

Equations 1-15A and 1-15B are equivalent, and either can be used. As previously discussed, noise gain (NG) is simply the gain seen by a small voltage source in series with the op amp input, and is also the ideal amplifier signal gain in the non-inverting mode. If A_{VOL} in equations 1-15A and 1-15B is infinite, the closed-loop gain becomes exactly equal to the noise gain, $1/\beta$.

However, for NG << A_{VOL} and finite A_{VOL}, there is a closed-loop gain error estimation:

$$\text{Closed loop error(\%)} \approx \frac{NG}{A_{VOL}} \bullet 100$$

Eq. 1-16

Note that the expression of Eq. 1-16 is equivalent to the earlier mentioned Eq. 1-11, when $1/\beta$ is substituted for NG. Again, either form can be used, at the user's discretion.

Notice from Eq. 1-16 that the percent gain error is directly proportional to the noise gain, therefore the effects of finite A_{VOL} are less for low gain. Some examples illustrate key points about these gain relationships.

In Figure 1-51 below, the first example for a NG of 1000 shows that for an open-loop gain of 2 million, the closed-loop gain error is about 0.05%. Note that if the open-loop gain stays constant over temperature and for various output loads and voltages, the 0.05% gain error can easily be calibrated out of the measurement, and then there is then no overall system gain error. If, however, the open-loop gain *changes*, the resulting closed-loop gain will also change. This introduces a *gain uncertainty*. In the second example, A_{VOL} drops to 300,000, which produces a gain error of 0.33%. This situation introduces a *gain uncertainty* of 0.28% in the closed-loop gain. In most applications, when using a good amplifier, the gain resistors of the circuit will be the largest source of absolute gain error, but it should be noted that gain uncertainty cannot be removed by calibration.

◆ **"IDEAL" CLOSED LOOP GAIN = 1/β = NOISE GAIN (NG)**

◆ **ACTUAL CLOSED LOOP GAIN** $= \dfrac{1}{\beta} \cdot \left| \dfrac{1}{1 + \dfrac{1}{A_{VOL}\beta}} \right| = \dfrac{NG}{1 + \dfrac{NG}{A_{VOL}}}$

◆ **CLOSED LOOP GAIN ERROR (%)** $\approx \dfrac{NG}{A_{VOL}} \times 100$ $(NG \ll A_{VOL})$

    ◆ **Ex. 1: Assume A_{VOL} = 2,000,000, NG = 1,000**
        % GAIN ERROR ≈ 0.05%

    ◆ **Ex. 2: Assume A_{VOL} Drops to 300,000**
        % GAIN ERROR ≈ 0.33%

    ◆ **CLOSED LOOP GAIN UNCERTAINTY**
        = 0.33% − 0.05% = 0.28%

Figure 1-51: Changes in open-loop gain cause closed-loop gain uncertainty

Changes in the output voltage level and output loading are the most common causes of changes in the open-loop gain of op amps. A change in open-loop gain with signal level produces a *nonlinearity* in the closed-loop gain transfer function, which also cannot be removed during system calibration. Most op amps have fixed loads, so A_{VOL} changes with load are not generally important. However, the sensitivity of A_{VOL} to output signal level may increase for higher load currents.

The severity of this non-linearity varies widely from one device type to another, and generally isn't specified on the data sheet. The minimum A_{VOL} is always specified, and choosing an op amp with a high A_{VOL} will minimize the probability of gain nonlinearity errors. Gain nonlinearity can come from many sources, depending on the design of the op amp. One common source is thermal feedback (for example, from a hot output stage back to the input stage). If temperature shift is the sole cause of the nonlinearity error, it can be assumed that minimizing the output loading will help. To verify this, the nonlinearity is measured with no load, and then compared to the loaded condition.

An oscilloscope X-Y display test circuit for measuring DC open-loop gain nonlinearity is shown in Figure 1-52 below. The same precautions previously discussed relating to the offset voltage test circuit must also be observed in this circuit. The amplifier is configured for a signal gain of -1. The open-loop gain is defined as the change in output voltage divided by the change in the input offset voltage. However, for large values of A_{VOL}, the actual offset may change only a few microvolts over the entire output voltage swing. Therefore the divider consisting of the 10Ω resistor and R_G ($1M\Omega$) forces the node voltage V_Y to be :

$$V_Y = \left[1 + \frac{R_G}{10\Omega}\right] V_{OS} = 100,001 \bullet V_{OS}.$$

Eq. 1-17

The value of R_G is chosen to give measurable voltages at V_Y depending on the expected values of V_{OS}.
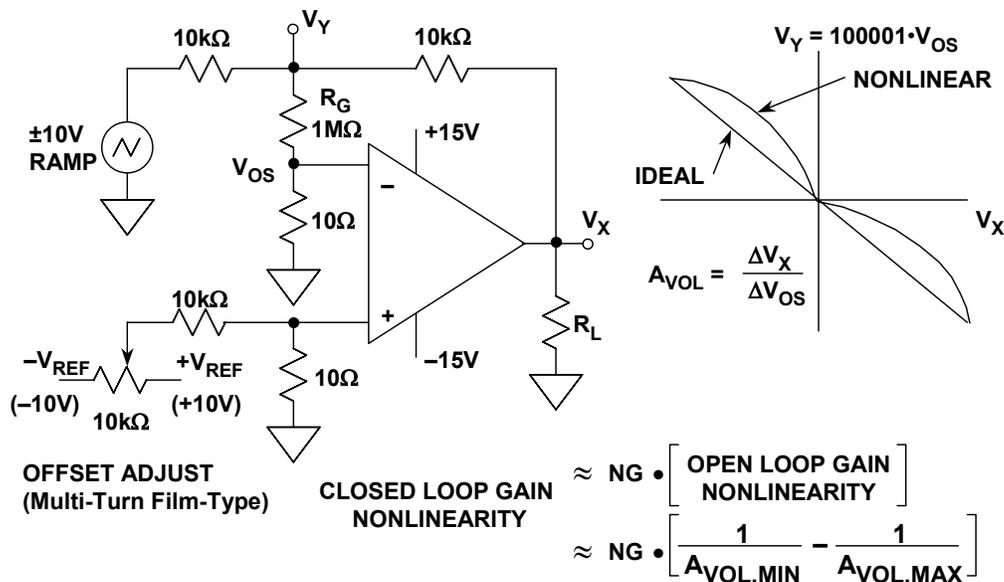
Figure 1-52: *Circuit measures open-loop gain nonlinearity*

The $\pm 10V$ ramp generator output is multiplied by the signal gain, -1, and forces the op amp output voltage V_X to swing from $+10V$ to $-10V$. Because of the gain factor applied to the offset voltage, the offset adjust potentiometer is added to allow the initial output offset to be set to zero. The resistor values chosen will null an input offset voltage of up to $\pm 10mV$. Stable 10V voltage references such as the AD688 should be used at each end of the potentiometer to prevent output drift. *Also, note that the ramp generator frequency must be quite low, probably no more than a fraction of 1Hz because of the low corner frequency of the open-loop gain (0.1Hz for the OP177).*

The plot on the right-hand side of Fig. 1-52 shows V_Y plotted against V_X. If there is no gain nonlinearity the graph will have a constant slope, and A_{VOL} is calculated as follows:

$$A_{VOL} = \frac{\Delta V_X}{\Delta V_{OS}} = \left[1 + \frac{R_G}{10\Omega}\right]\left[\frac{\Delta V_X}{\Delta V_Y}\right] = 100,001 \bullet \left[\frac{\Delta V_X}{\Delta V_Y}\right].$$

Eq. 1-18

If there is nonlinearity, A_{VOL} will vary dynamically as the output signal changes. The approximate open-loop gain nonlinearity is calculated based on the maximum and minimum values of A_{VOL} over the output voltage range:

$$\text{Open -Loop Gain Nonlinearity} = \frac{1}{A_{VOL,MIN}} - \frac{1}{A_{VOL,MAX}}. \qquad \text{Eq. 1-19}$$

The closed-loop gain nonlinearity is obtained by multiplying the open-loop gain nonlinearity by the noise gain, NG:

$$\text{Closed -Loop Gain Nonlinearity} \approx NG \bullet \left[\frac{1}{A_{VOL,MIN}} - \frac{1}{A_{VOL,MAX}} \right]. \qquad \text{Eq. 1-20}$$

In an ideal case, the plot of V_{OS} versus V_X would have a constant slope, and the reciprocal of the slope is the open-loop gain, A_{VOL}. A horizontal line with zero slope would indicate infinite open-loop gain. In an actual op amp, the slope may change across the output range because of nonlinearity, thermal feedback, etc. In fact, the slope can even change sign.
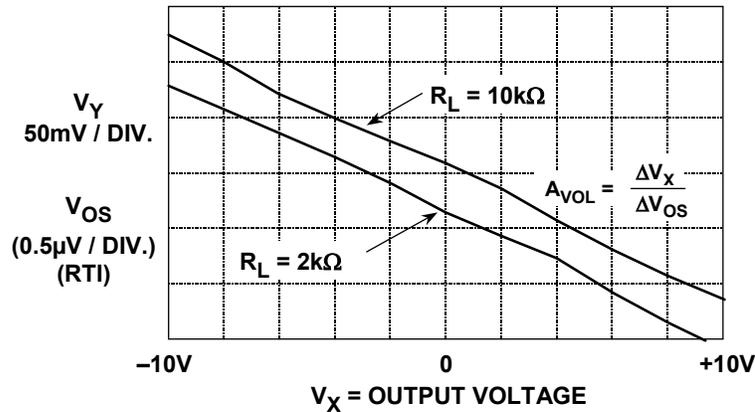
A_{VOL} (AVERAGE) $\approx$ 8 million

$A_{VOL,MAX} \approx$ 9.1 million, $A_{VOL,MIN} \approx$ 5.7 million

OPEN LOOP GAIN NONLINEARITY $\approx$ 0.07ppm

CLOSED LOOP GAIN NONLINEARITY $\approx$ NG×0.07ppm

Figure 1-53: OP177 gain nonlinearity

Figure 1-53 above shows the V_Y (and V_{OS}) versus V_X plot for an OP177 precision op amp. The plot is shown for two different loads, 2kΩ and 10kΩ. The reciprocal of the slope is calculated based on the end points, and the average A_{VOL} is about 8 million. The maximum and minimum values of A_{VOL} across the output voltage range are measured to be approximately 9.1 million, and 5.7 million, respectively. This corresponds to an open-loop gain nonlinearity of about 0.07ppm. Thus, for a noise gain of 100, the corresponding closed-loop gain nonlinearity is about 7ppm.

These nonlinearity measurements are, of course, most applicable to high precision DC circuits. But they are also applicable to wider bandwidth applications, such as audio. The X-Y display technique of Fig. 1-52 will easily show crossover distortion in a poorly designed op amp output stage, for example.

Op Amp Frequency Response

There are a number of issues to consider when discussing the frequency response of op amps. Some are relevant to both voltage and current feedback op amp types, some apply to one or the other, but not to both. Issues which vary with type are usually related to small-signal performance, while large-signal issues mostly apply to both.

A good working definition of "large-signal" is where the output voltage swing/frequency limit is set by the slew rate measured at the output stage, rather than the pole(s) of the small signal response. We shall therefore consider large signal parameters applying to both types of op amp before we consider those parameters where they differ.

Frequency Response— Slew Rate and Full-Power Bandwidth

The slew rate (SR) of an amplifier is the maximum rate of change of voltage at its output. It is expressed in V/s (or, more probably, V/μs). We have mentioned earlier why op amps might have different slew rates during positive and negative going transitions, but for this analysis we shall assume that good fast op amps have reasonably symmetrical slew rates.

If we consider a sine wave signal with a peak-to-peak amplitude of $2V_p$ and of a frequency f, the expression for the output voltage is:

$$V(t) = V_p \sin 2\pi ft. \hspace{3cm} \text{Eq. 1-21}$$

This sine wave signal has a maximum rate-of-change (slope) at the zero crossing. This maximum rate-of-change is:

$$\left.\frac{dv}{dt}\right|_{max} = 2\pi f V_p . \hspace{3cm} \text{Eq. 1-22}$$

To reproduce this signal without distortion, an amplifier must be able to respond in terms of its output voltage at this rate (or faster). When an amplifier reaches its maximum output rate-of-change, or *slew rate*, it is said to be *slew limiting* (sometimes also called rate limiting). So, we can see that the maximum signal frequency at which slew limiting *does not* occur is directly proportional to the signal slope, and inversely proportional to the amplitude of the signal. This allows us to define the *full-power bandwidth* (FPBW) of an op amp, which is the maximum frequency at which slew limiting doesn't occur for rated voltage output. It is calculated by letting $2V_p$ in Eq. 1-22 equal the maximum peak-to-peak swing of the amplifier, dV/dt equal the amplifier slew rate, and solving for f:

$$\text{FPBW} = \text{Slew Rate}/2\pi V_p \hspace{3cm} \text{Eq. 1-23}$$

It is important to realize that both slew rate and full-power bandwidth can also depend somewhat on the power supply voltage being used, and the load the amplifier is driving (particularly if it is capacitive).

The key issues regarding slew rate and full-power bandwidth are summarized in Figure 1-54 below. As a point of reference, an op amp with a 1V peak output swing reproducing a 1MHz sine wave must have a minimum SR of 6.28V/μs.

◆ **Slew Rate = Maximum rate at which the output voltage of an op amp can change**

◆ **Ranges: A few volts/μs to several thousand volts/μs**

◆ **For a sinewave, $V_{out} = V_p\sin 2\pi ft$**

$$dV/dt = 2\pi f V_p \cos 2\pi ft$$

$$(dV/dt)_{max} = 2\pi f V_p$$

◆ **If $2V_p$ = full output span of op amp, then**

$$\text{Slew Rate} = (dV/dt)_{max} = 2\pi \cdot FPBW \cdot V_p$$

$$FPBW = \text{Slew Rate} / 2\pi V_p$$

Figure 1-54: Slew rate and full-power bandwidth

Realistically, for a practical circuit the designer would choose an op amp with a SR in excess of this figure, since real op amps show increasing distortion prior to reaching the slew limit point.

Frequency Response— Settling Time

The *settling time* of an amplifier is defined as the time it takes the output to respond to a step change of input and *come into, and remain within a defined error band*, as measured relative to the 50% point of the input pulse, as shown in Figure 1-55 below.
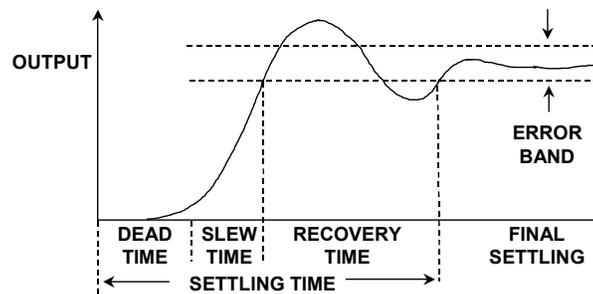
◆ **Error band is usually defined to be a percentage of the step 0.1%, 0.05%, 0.01%, etc.**

◆ **Settling time is non-linear; it may take 30 times as long to settle to 0.01% as to 0.1%.**

◆ **Manufacturers often choose an error band which makes the op amp look good.**
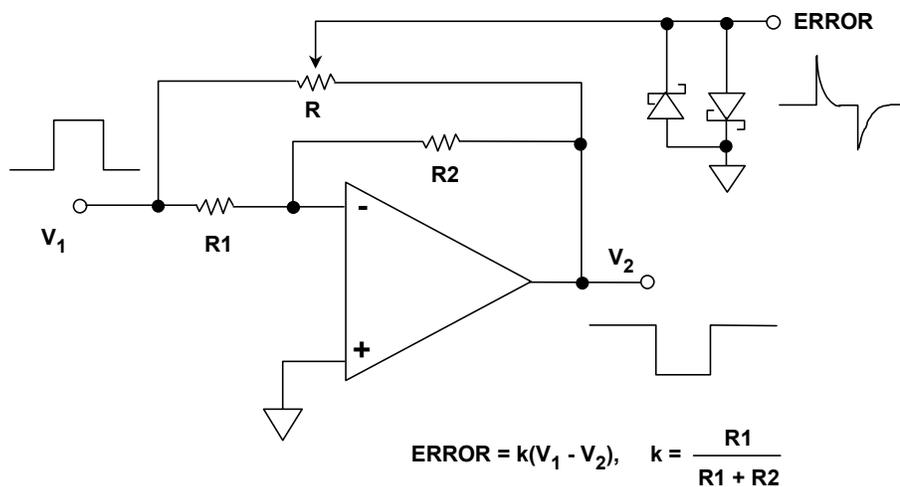
Figure 1-55: Settling time

Unlike a DAC device, there is no natural error band for an op amp (a DAC naturally has an error band of 1 LSB, or perhaps ±1LSB). So, one must be chosen and defined, along with other definitions, such as the step size (1V, 5V, 10V, etc.). What is chosen will

depend on the performance of the op amp, but since the value chosen will vary from device to device, comparisons are often difficult. This is true because settling is not linear, and many different time constants may be involved. Examples are early op amps using dielectrically isolated (DI) processes. These had very fast settling to 1% of full-scale, but they took almost forever to settle to 10-bits (0.1 %). Similarly, some very high precision op amps have thermal effects that cause settling to 0.001% or better to take tens of ms, although they will settle to 0.025% in a few μs.

It should also be noted that thermal effects can cause significant differences between short-term settling time (generally measured in nanoseconds) and long-term settling time (generally measured in microseconds or milliseconds). In many AC applications, long-term settling time is not important; but if it is, it must be measured on a much different time scale that short-term settling time.

$$ERROR = k(V_1 - V_2), \quad k = \frac{R1}{R1 + R2}$$

*Figure 1-56: Measuring settling time using a "false summing node"*

Measuring fast settling time to high accuracy is very difficult. Great care is required in order to generate fast, highly accurate, low noise, flat top pulses. Large amplitude step voltages will overdrive many oscilloscope front ends, when the input scaling is set for high sensitivity.

The example test setup shown in Figure 1-56 above is useful in making settling time measurements on op amps operating in the inverting mode. The signal at the "false summing node" represents the difference between the output and the input signal, multiplied by the constant k., i.e. the ERROR signal.

There are many subtleties involved towards making this setup work reliably. The resistances should low in value, to minimize parasitic time constants. The back-back Schottky diode clamps help prevent scope overdrive, and allow high sensitivity. If R1=R2, then k = 0.5. Thus the error band at the ERROR output will be 5mV for 0.1% settling with a 10V input step.

In some case, a second (very fast) amplifier stage may be used after the false summing node, to increase the signal level. In any case, testing of settling time must be done with a test setup identical to that used by the op amp manufacturer, to ensure validity.

1.70

Many modern digitizing oscilloscopes are insensitive to input overdrive and can be used to measure the ERROR waveform directly— this must be verified for each oscilloscope by examining the operating manual carefully. Note that a direct measurement allows measurements of settling time in both the inverting and non-inverting modes. An example of the output step response to a flat pulse input for the AD8039 op amp is shown in Figure 1-57 below. Notice that the settling time to 0.1% is approximately 18ns.
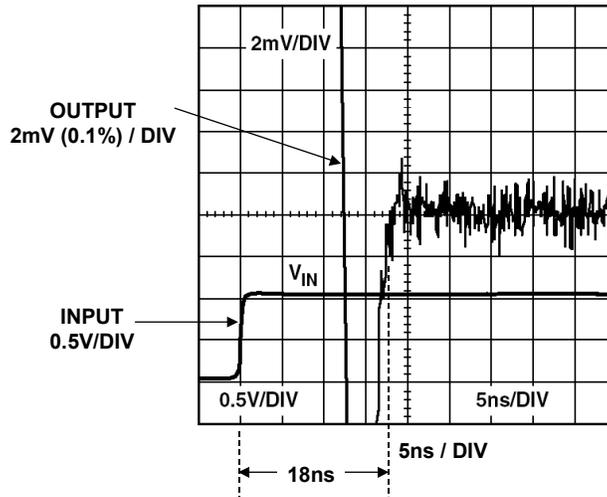
Figure 1-57: AD8039 G = +2 settling time measured directly

In making settling time measurements of this type, it is also imperative to use a pulse generator source capable of generating a pulse of sufficient flatness. In other words, if the op amp under test has a settling time of 20ns to 0.1%, the applied pulse should settle to better than 0.05% in less than 5ns.
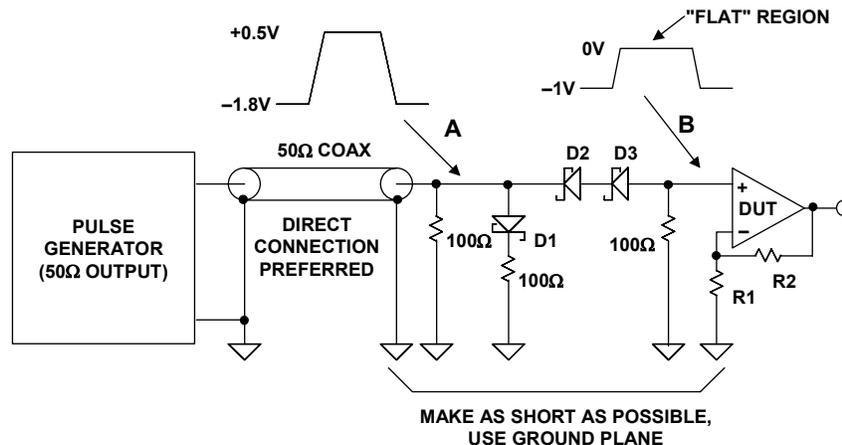
Figure 1-58: A simple flat pulse generator

This type of generator can be expensive, but a simple circuit as shown in Figure 1-58 can be used with a reasonably flat generator to ensure a flat pulse output.

The circuit of Fig. 1-58 works best if low capacitance Schottky diodes are used for D1-D2-D3, and the lead lengths on all the connections are minimized. A short length of 50Ω coax can be used to connect the pulse generator to the circuit, however best results are obtained if the test fixture is connected directly to the output of the generator. The pulse generator is adjusted to output a positive-going pulse at "A" which rises from

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approximately –1.8V to +0.5V in less than 5ns (assuming the settling time of the DUT is in the order of 20ns). Shorter rise times may generate ringing, and longer rise times can degrade the DUT settling time; therefore some optimization is required in the actual circuit to get best performance. When the pulse generator output "A" goes above 0V, D1 begins to conduct, and D2/D3 are reversed biased. The "0V" region of the signal "B" at the input of the DUT is flat "by definition"— neglecting the leakage current and stray capacitance of the D2-D3 series combination. The D1 diode and its 100Ω resistor help maintain an approximate 50Ω termination during the time the pulse at "A" is positive.

Frequency Response— Voltage Feedback Op amps, Gain-Bandwidth Product

The open-loop frequency response of a voltage feedback op amp is shown in Figure 1-59 below. There are two possibilities: Fig. 1-59A shows the most common, where a high DC gain drops at 6dB/octave from quite a low frequency down to unity gain. This is a classic single pole response. By contrast, the amplifier in Fig. 1-59B has two poles in its response—gain drops at 6dB/octave for a while, and then drops at 12dB/octave. The amplifier in Fig. 1-59A is known as an *unconditionally stable* or *fully compensated* type and may be used with a noise gain of unity. This type of amplifier is stable with 100% feedback (including capacitance) from output to inverting input.
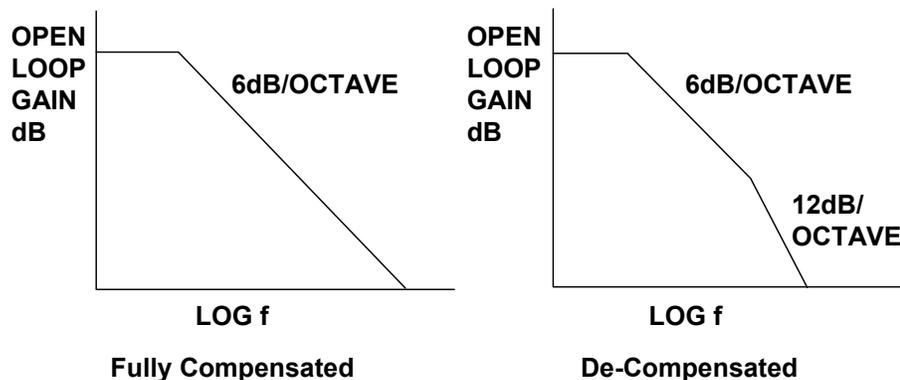

Figure 1-59: *Frequency response of voltage feedback op amps*

Compare this to the amplifier in Fig 1-59B. If this op amp is used with a noise gain that is lower than the gain at which the slope of the response increases from 6 to 12dB/octave, the phase shift in the feedback will be too great, and it will oscillate. Amplifiers of this type are characterized as "stable at gains ≥ X" where X is the gain at the frequency where the 6dB/12dB transition occurs. Note that here it is, of course, the *noise gain* that is being referenced. The gain level for stability might be between 2 and 25, typically quoted behavior might be "gain-of-five-stable**,"** etc. These *decompensated* op amps do have higher gain-bandwidth products than fully compensated amplifiers, all other things being equal. So, they are useful, despite the slightly greater complication of designing with them. But, unlike their fully compensated op amp relatives, a decompensated op amp can never be used with direct capacitive feedback from output to inverting input.

The 6dB/octave slope of the response of both types means that over the range of frequencies where this slope occurs, *the product of the closed-loop gain and the 3dB closed-loop bandwidth at that gain is a constant* —this is known as the *gain-bandwidth product* (GBW) and is a figure of merit for an amplifier.

For example, if an op amp has a GBW product of X MHz, then its closed-loop bandwidth at a noise gain of 1 will be X MHz, at a noise gain of 2 it will be X/2 MHz, and at a noise gain of Y it will be X/Y MHz (see Figure 1-60 below). Notice that the *closed-loop* bandwidth is the frequency at which the noise gain plateau intersects the open-loop gain.
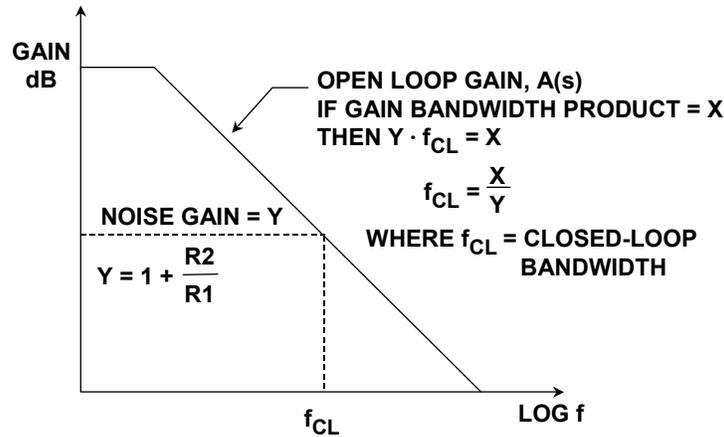
Figure 1-60: *Gain-bandwidth product for voltage feedback op amps*

In the above example, it was assumed that the feedback elements were resistive. This is not usually the case, especially when the op amp requires a feedback capacitor for stability.

Figure 1-61 below shows a typical example where there is capacitance, C1, on the inverting input of the op amp. This capacitance is the sum of the op amp internal capacitance, plus any external capacitance that may exist. This always-present capacitance introduces a pole in the noise gain transfer function.
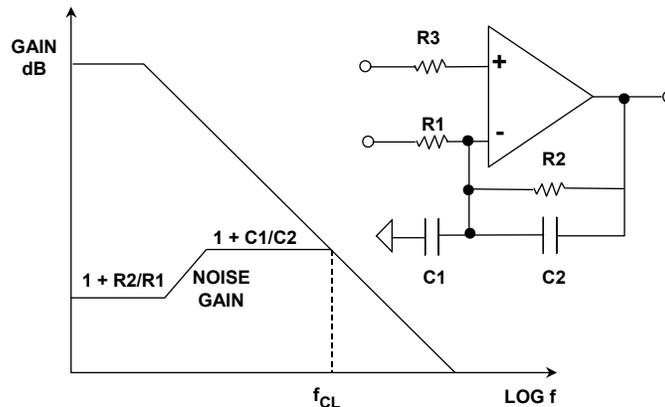
Figure 1-61: *Bode plot showing noise gain for voltage feedback op amp with reactive and resistive feedback elements*

The net slope of the noise gain curve and the open-loop gain curve, *at the point of intersection*, determines system stability. For unconditional stability, the noise gain must intersect the open-loop gain with a net slope of less than 12dB/octave (20dB per decade). Adding the feedback capacitor, C2, introduces a zero in the noise gain transfer function, which stabilizes the circuit. Notice that in Fig. 1-61 the closed-loop bandwidth, f_{cl}, is the frequency at which the noise gain intersects the open-loop gain.

■ **OP AMP APPLICATIONS**

The Bode plot of the noise gain is a very useful tool in analyzing op amp stability. Constructing the Bode plot is a relatively simple matter. Although it is outside the scope of this section to carry the discussion of noise gain and stability further, the reader is referred to Reference 1 for an excellent treatment of constructing and analyzing Bode plots. Second-order systems related to noise analysis are discussed later in this section.

Frequency Response— Current Feedback Op amps

Current feedback op amps do not behave in the same way as voltage feedback types. They are not stable with capacitive feedback, nor are they so with a short circuit from output to inverting input. With a CFB op amp, *there is generally an optimum feedback resistance for maximum bandwidth.* Note that the value of this resistance may vary with supply voltage— consult the device data sheet. If the feedback resistance is increased, the bandwidth is reduced. Conversely, if it is reduced, bandwidth increases, and the amplifier may become unstable.

GAIN dB

G1

$G1 \cdot f_1 \ne G2 \cdot f_2$

G2

f_1 f_2 LOG f
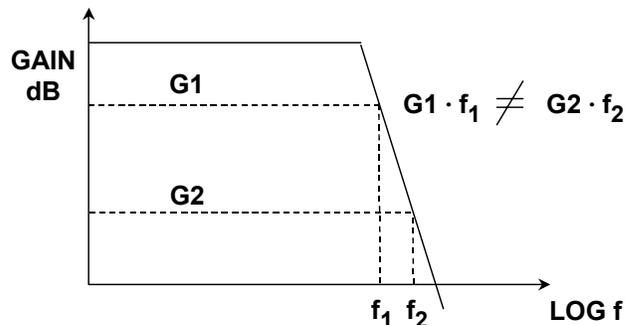
◆ **Feedback resistor fixed for optimum performance. Larger values reduce bandwidth, smaller values may cause instability.**

◆ **For fixed feedback resistor, changing gain has little effect on bandwidth.**

◆ **Current feedback op amps do not have a fixed gain-bandwidth product.**

**Figure 1-62:** *Frequency response for current feedback op amps*

In a CFB op amp, for a given value of feedback resistance (R2), *the closed-loop bandwidth is largely unaffected by the noise gain*, as shown in Figure 1-62 above. Thus it is not correct to refer to gain-bandwidth product, for a CFB amplifier, because of the fact that it is not constant. Gain is manipulated in a CFB op amp application by choosing the correct feedback resistor for the device (R2), and then selecting the bottom resistor (R1) to yield the desired closed loop gain. The gain relationship of R2 and R1 is identical to the case of a VFB op amp (Fig. 1-14, again).

Typically, CFB op amp data sheets will provide a table of recommended resistor values, which provide maximum bandwidth for the device, over a range of both gain and supply voltage. It simplifies the design process considerably to use these tables.

Bandwidth Flatness

In demanding applications such as professional video, it is desirable to maintain a relatively flat bandwidth and linear phase up to some maximum specified frequency, and simply specifying the 3dB bandwidth isn't enough. In particular, it is customary to specify the *0.1dB bandwidth*, or *0.1dB bandwidth flatness*. This means there is no more than 0.1dB ripple up to a specified 0.1dB bandwidth frequency.

Video buffer amplifiers generally have both the 3dB and the 0.1dB bandwidth specified. Figure 1-63 below shows the frequency response of the AD8075 triple video buffer.
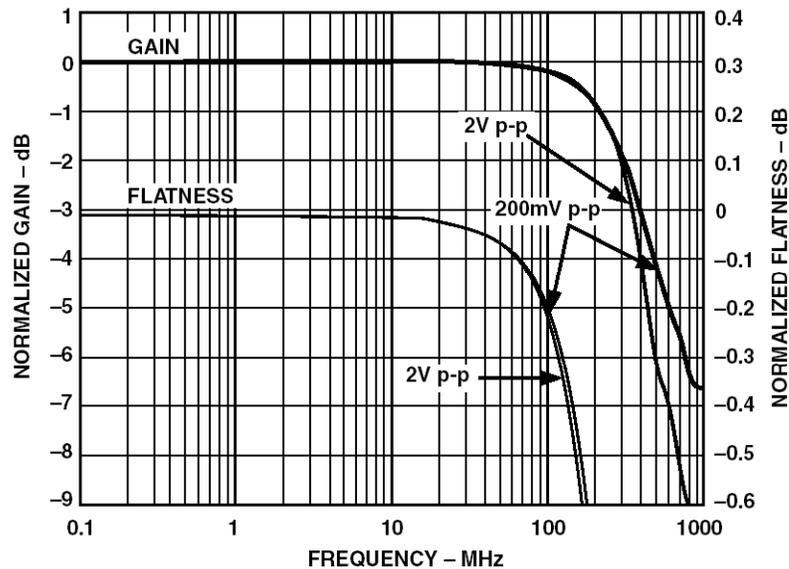
3dB BANDWIDTH ≈ 400MHz, 0.1dB BANDWIDTH ≈ 65MHz

Figure 1-63: 3dB and 0.1dB bandwidth for the AD8075, G = 2,
triple video buffer, R_L = 150Ω

Note that the 3dB bandwidth is approximately 400MHz. This can be determined from the response labeled "GAIN" in the graph, and the corresponding gain scale is shown on the left-hand vertical axis (at a scaling of 1dB/division).

The response scale for "FLATNESS" is on the right-hand vertical axis, at a scaling of 0.1dB/division in this case. This allows the 0.1dB bandwidth to be determined, which is about 65MHz in this case. There is the general point to be noted here, and that is the major difference in the applicable bandwidth between the 3dB and 0.1dB criteria. It requires a 400MHz bandwidth amplifier (as conventionally measured) to provide the 65MHz 0.1dB flatness rating.

It should be noted that these specifications hold true when driving a 75Ω source and load terminated cable, which represents a resistive load of 150Ω. Any capacitive loading at the amplifier output will cause peaking in the frequency response, and must be avoided.

Operational Amplifier Noise

This section discusses the noise generated within op amps, not the external noise which they may pick up. External noise is also important, and is discussed in detail in Chapter 7, but in this section we are concerned solely with internal noise.

There are three noise sources in an op amp: a voltage noise which appears differentially across the two inputs, and two current noise sources, one in each input. The simple voltage noise op amp model is shown in Figure 1-64 below. The three noise sources are effectively uncorrelated (independent of each other). There is a slight correlation between the two noise currents, but it is too small to need consideration in practical noise analyses. In addition to these three internal noise sources, it is necessary to consider the Johnson noise of the external gain setting resistors that are used with the op amp.
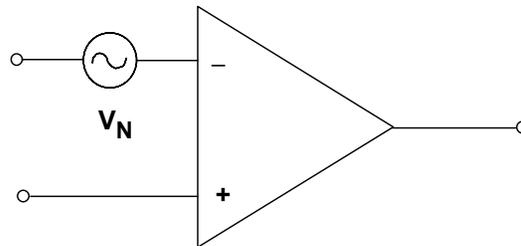
◆ **Input Voltage Noise is bandwidth dependent and measured in nV/√Hz (noise spectral density)**

◆ **Normal Ranges are 1nV/√ Hz to 20nV/√Hz**

Figure 1-64: Input voltage noise

All resistors have a Johnson noise of $\sqrt{(4kTBR)}$, where k is Boltzmann's Constant $(1.38 \times 10^{-23} \text{J/K})$, T is the absolute temperature, B is the bandwidth, and R is the resistance. Note that this is an intrinsic property— it is not possible to obtain resistors that do not have Johnson noise. The simple model is shown in Figure 1-65 below.

◆ **ALL resistors have a voltage noise of $V_{NR} = \sqrt{(4kTBR)}$**

◆ **T = Absolute Temperature = T(°C) + 273.15**

◆ **B = Bandwidth (Hz)**

◆ **k = Boltzmann's Constant $(1.38 \times 10^{-23} \text{J/K})$**

◆ **A 1000Ω resistor generates 4nV / √Hz @ 25°C**

Figure 1-65: Johnson noise of resistors

Uncorrelated noise voltages add in a "root-sum-of-squares" manner; i.e., noise voltages V_1, V_2, V_3 give a summed result of $\sqrt{(V_1^2 + V_2^2 + V_3^2)}$. Noise powers, of course, add

normally. Thus, any noise voltage that is more than 3 to 5 times any of the others is dominant, and the others may generally be ignored. This simplifies noise assessment.

The voltage noise of different op amps may vary from under 1nV/√Hz to 20nV√Hz, or even more. Bipolar op amps tend to have lower voltage noise than JFET ones, although it is possible to make JFET op amps with low voltage noise (such as the AD743/AD745), at the cost of large input devices, and hence large input capacitance. Voltage noise is specified on the data sheet, and it isn't possible to predict it from other parameters.

Current noise can vary much more widely, dependent upon the input structure. It ranges from around 0.1fA/√Hz (in JFET electrometer op amps) to several pA/√Hz (in high speed bipolar op amps). It isn't always specified on data sheets, but may be calculated in cases like simple BJT or JFETs, where all the bias current flows in the input junction, because in these cases it is simply the Schottky (or shot) noise of the bias current.
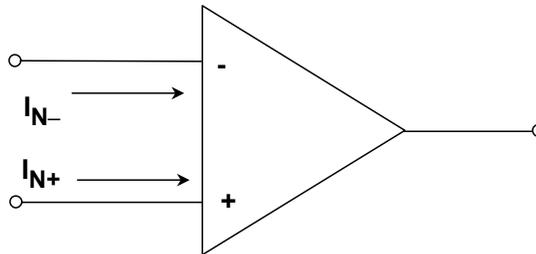
- ◆ **Normal Ranges: 0.1fA/√ Hz to 10pA/√Hz**
- ◆ **In Voltage Feedback op amps the current noise in the inverting and non-inverting inputs is uncorrelated (effectively) but roughly equal in magnitude.**
- ◆ **In simple BJT and JFET input stages, the current noise is the shot noise of the bias current and may be calculated from the bias current.**
- ◆ **In bias-compensated input stages and in current feedback op amps, the current noise cannot be calculated.**
- ◆ **The current noise in the two inputs of a current feedback op amp may be quite different. They may not even have the same 1/f corner.**
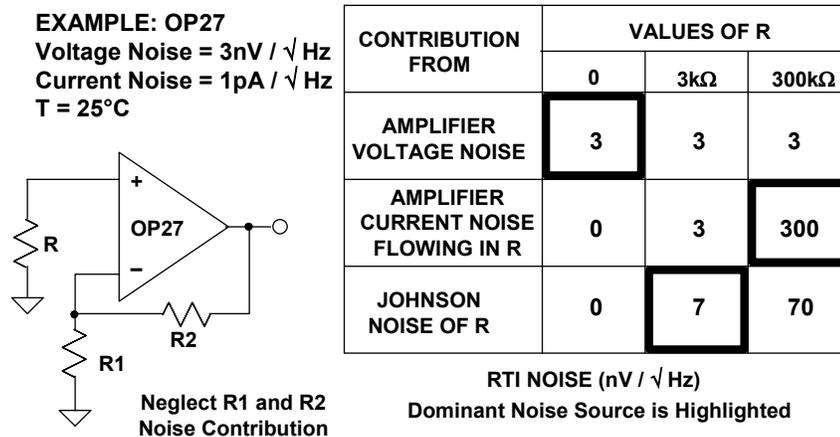
Figure 1-66: *Input current noise*

Shot noise spectral density is simply $\sqrt{(2I_B q)}$/√Hz, where I_B is the bias current (in amps) and q is the charge on an electron (1.6×10^{-19} C). It can't be calculated for bias-compensated or current feedback op amps, where the external bias current is the *difference* of two internal currents. A simple current noise model is shown in Figure 1-66.

Current noise is only important when it flows in an impedance, and thus generates a noise voltage. Maintaining relatively low impedances at the input of an op amp circuit contributes markedly to minimizing the effects of current noise (just as doing the same thing also aids in minimizing offset voltage)

It is logical therefore, that the optimum choice of a low noise op amp depends on the impedances around it. This will be illustrated with the aid of some impedance examples, immediately below.

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Consider for example an OP27, an op amp with low voltage noise (3nV/√Hz), but quite high current noise (1pA/√Hz). With zero source impedance, the voltage noise will dominate as shown in Figure 1-67 below (left column). With a source resistance of 3kΩ (center column), the current noise of 1pA/√Hz flowing in 3kΩ will equal the voltage noise, but the Johnson noise of the 3kΩ resistor is 7nV/√Hz and is dominant. With a source resistance of 300kΩ (right column), the current noise portion increases 100× to 300nV/√Hz, voltage noise continues unchanged, and the Johnson noise (which is proportional to the resistance *square root*) increases tenfold. Current noise dominates.

EXAMPLE: OP27
Voltage Noise = 3nV / √ Hz
Current Noise = 1pA / √ Hz
T = 25°C

OP27

R

R2

R1

Neglect R1 and R2
Noise Contribution

CONTRIBUTION FROM	VALUES OF R		
	0	3kΩ	300kΩ
AMPLIFIER VOLTAGE NOISE	**3**	3	3
AMPLIFIER CURRENT NOISE FLOWING IN R	0	3	**300**
JOHNSON NOISE OF R	0	**7**	70

RTI NOISE (nV / √ Hz)
Dominant Noise Source is Highlighted

Figure 1-67: Different noise sources dominate at different source impedances

The above example shows that the choice of a low noise op amp depends on the source impedance of the signal, and at high impedances, current noise always dominates.
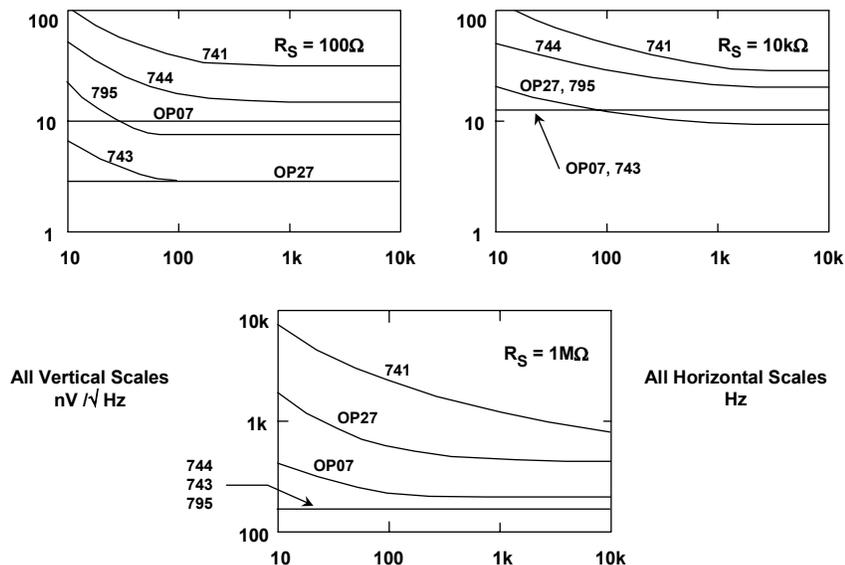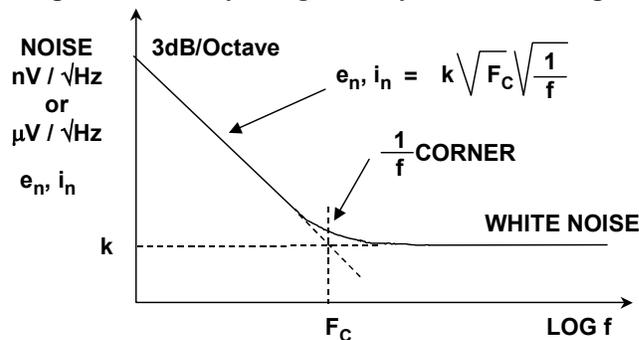

Figure 1-68: Different amplifiers are best at different source impedances

From Figure 1-68 above, it should be apparent that different amplifiers are best at different source impedances. For low impedance circuits, low voltage noise amplifiers such as the OP27 will be the obvious choice, since they are inexpensive, and their comparatively large current noise will not affect the application. At medium resistances, the Johnson noise of resistors is dominant, while at very high source resistance, we must choose an op amp with the smallest possible current noise, such as the AD549 or AD795.

Until recently, BiFET amplifiers tended to have comparatively high voltage noise (though very low current noise), and were thus more suitable for low noise applications in high rather than low impedance circuitry. The AD795, AD743, and AD745 have very low values of both voltage and current noise. The AD795 specifications at 10kHz are 10nV/√Hz and 0.6fA/√Hz, and the AD743/AD745 specifications at 10kHz are 2.9nV/√Hz and 6.9fA/√Hz. These make possible the design of low-noise amplifier circuits that have low noise over a wide range of source impedances.

The *noise figure* of an amplifier is the amount (in dB) by which the noise of the amplifier exceeds the noise of a perfect noise-free amplifier in the same environment. The concept is useful in RF and TV applications, where 50Ω and 75Ω transmission lines and terminations are ubiquitous, but is useless for an op amp that is used in a wide range of electronic environments. Noise figure related to communications applications is discussed in more detail in Chapter 6 (Section 6-4). Voltage noise spectral density and current noise spectral density are generally more useful specifications in most cases.

NOISE
nV / √Hz
or
μV / √Hz

e_n, i_n

3dB/Octave

$$e_n, i_n \ = \ k\sqrt{F_C}\sqrt{\frac{1}{f}}$$

$\frac{1}{f}$ CORNER

WHITE NOISE

k

F_C LOG f

◆ **1/f Corner Frequency is a figure of merit for op amp noise performance (the lower the better)**

◆ **Typical Ranges: 2Hz to 2kHz**

◆ **Voltage Noise and Current Noise do not necessarily have the same 1/f corner frequency**

Figure 1-69: Frequency characteristic of op amp noise

So far, we have assumed that noise is *white* (i.e., its spectral density does not vary with frequency). This is true over most of an op amp's frequency range, but at low frequencies the noise spectral density rises at 3dB/octave, as shown in Figure 1-69 above. The power spectral density in this region is inversely proportional to frequency, and therefore the voltage noise spectral density is inversely proportional to the square root of the frequency. For this reason, this noise is commonly referred to as *1/f noise*. Note however, that some textbooks still use the older term *flicker noise*.

The frequency at which this noise starts to rise is known as the *1/f corner frequency* (F_C) and is a figure of merit— the lower it is, the better. The 1/f corner frequencies are not necessarily the same for the voltage noise and the current noise of a particular amplifier, and a current feedback op amp may have three 1/f corners: for its voltage noise, its inverting input current noise, and its non-inverting input current noise.

The general equation which describes the voltage or current noise spectral density in the 1/f region is

$$e_n, i_n, = k\sqrt{F_C}\sqrt{\frac{1}{f}},$$

<div align="right">Eq. 1-24</div>

where k is the level of the "white" current or voltage noise level, and F_C is the 1/f corner frequency.

The best low frequency low noise amplifiers have corner frequencies in the range 1-10Hz, while JFET devices and more general purpose op amps have values in the range to 100Hz. Very fast amplifiers, however, may make compromises in processing to achieve high speed which result in quite poor 1/f corners of several hundred Hz or even 1-2kHz. This is generally unimportant in the wideband applications for which they were intended, but may affect their use at audio frequencies, particularly for equalized circuits.

Popcorn Noise

Popcorn noise is so-called because when played through an audio system, it sounds like cooking popcorn. It consists of random step changes of offset voltage that take place at random intervals in the 10+ millisecond timeframe. Such noise results from high levels of contamination and crystal lattice dislocation at the surface of the silicon chip, which in turn results from inappropriate processing techniques or poor quality raw materials.

When monolithic op amps were first introduced in the 1960s, popcorn noise was a dominant noise source. Today, however, the causes of popcorn noise are well understood, raw material purity is high, contamination is low, and production tests for it are reliable so that no op amp manufacturer should have any difficulty in shipping products that are substantially free of popcorn noise. For this reason, it is not even mentioned in most modern op amp textbooks.

RMS Noise Considerations

As was discussed above, noise spectral density is a function of frequency. In order to obtain the RMS noise, the noise spectral density curve must be integrated over the bandwidth of interest.

In the 1/f region, the RMS noise in the bandwidth F_L to F_C is given by

$$v_{n,rms}(F_L, F_C) = v_{nw}\sqrt{F_C}\sqrt{\int_{F_L}^{F_C}\frac{1}{f}\,df} = v_{nw}\sqrt{F_C \ln\left[\frac{F_C}{F_L}\right]}$$

<div align="right">Eq. 1-25</div>

where v_{nw} is the voltage noise spectral density in the "white" region, F_L is the lowest frequency of interest in the 1/f region, and F_C is the 1/f corner frequency.

The next region of interest is the "white" noise area which extends from F_C to F_H.

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The RMS noise in this bandwidth is given by

$$v_{n,rms}(F_C, F_H) = v_{nw}\sqrt{F_H - F_C}$$ Eq. 1-26

Eq. 1-25 and 1-26 can be combined to yield the total RMS noise from F_L to F_H:

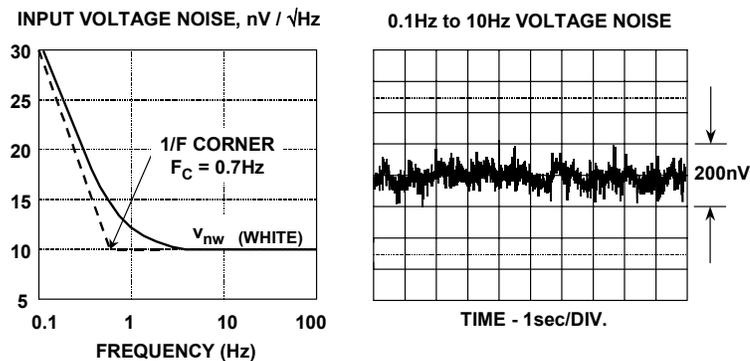$$v_{n,rms}(F_L, F_H) = v_{nw}\sqrt{F_C \ln\left[\frac{F_C}{F_L}\right] + (F_H - F_C)}$$ Eq. 1-27

In many cases, the low frequency p-p noise is specified in a 0.1 to 10Hz bandwidth, measured with a 0.1 to 10Hz bandpass filter between op amp and measuring device.
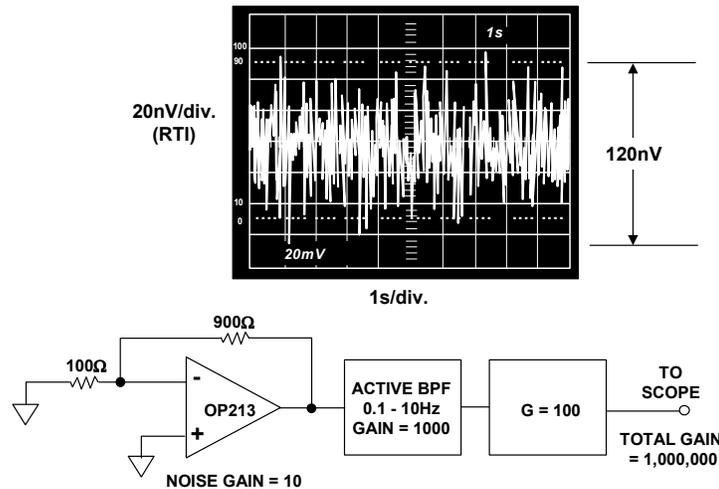
Figure 1-70: *The peak-to-peak noise in the 0.1Hz to 10Hz bandwidth for the OP213 is less than 120nV*

The measurement is often presented as a scope photo with a time scale of 1s/div, as is shown in Figure 1-70 above for the OP213.

♦ $V_{n,rms}(F_L, F_H) = v_{nw}\sqrt{F_C \ln\left[\frac{F_C}{F_L}\right] + (F_H - F_C)}$

♦ For $F_L = 0.1Hz$, $F_H = 10Hz$, $v_{nw} = 10nV/\sqrt{Hz}$, $F_C = 0.7Hz$:
  ♦ $V_{n,rms} = 33nV$
  ♦ $V_{n,pp} = 6.6 \times 33nV = 218nV$

Figure 1-71: *Input voltage noise for the OP177*

It is possible to relate the 1/f noise measured in the 0.1 to 10Hz bandwidth to the voltage noise spectral density. Figure 1-71 above shows the OP177 input voltage noise spectral

density on the left-hand side of the diagram, and the 0.1 to 10Hz peak-to-peak noise scope photo on the right-hand side. Equation 1-26 can be used to calculate the total RMS noise in the bandwidth 0.1 to 10Hz by letting $F_L = 0.1Hz$, $F_H = 10Hz$, $F_C = 0.7Hz$, $v_{nw} = 10nV/\sqrt{Hz}$. The value works out to be about 33nV RMS, or 218nV peak-to-peak (obtained by multiplying the RMS value by 6.6— see the following discussion). This compares well to the value of 200nV as measured from the scope photo.

It should be noted that at higher frequencies, the term in the equation containing the natural logarithm becomes insignificant, and the expression for the RMS noise becomes:

$$V_{n,rms}(F_H, F_L) \approx v_{nw} \sqrt{F_H - F_L} \ .$$ Eq. 1-28

And, if $F_H \gg F_L$,

$$V_{n,rms}(F_H) \approx v_{nw} \sqrt{F_H} \ .$$ Eq. 1-29

However, some op amps (such as the OP07 and OP27) have voltage noise characteristics that increase slightly at high frequencies. The voltage noise versus frequency curve for op amps should therefore be examined carefully for flatness when calculating high frequency noise using this approximation.

At very low frequencies when operating exclusively in the 1/f region, $F_C \gg (F_H - F_L)$, and the expression for the RMS noise reduces to:

$$V_{n,rms}(F_H, F_L) \approx v_{nw} \sqrt{F_C \ln \left[\frac{F_H}{F_L} \right]} \ .$$ Eq. 1-30

Note that there is no way of reducing this 1/f noise by filtering if operation extends to DC. Making $F_H = 0.1Hz$ and $F_L = 0.001$ still yields an RMS 1/f noise of about 18nV RMS, or 119nV peak-to-peak.

EQUIVALENT NOISE BANDWIDTH = $1.57 \times f_C$
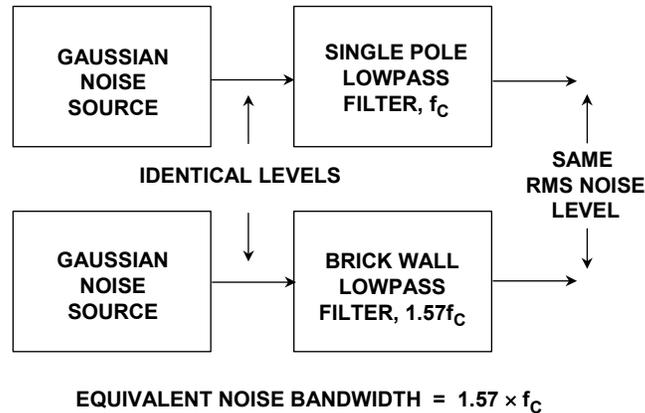
Figure 1-72: Equivalent noise bandwidth

The point is that averaging results of a large number of measurements over a long period of time has practically no effect on the RMS value of the 1/f noise. A method of reducing it further is to use a chopper stabilized op amp, to remove the low frequency noise.

In practice, it is virtually impossible to measure noise within specific frequency limits with no contribution from outside those limits, since practical filters have finite rolloff

1.82

characteristics. Fortunately, measurement error introduced by a single pole lowpass filter is readily computed. The noise in the spectrum above the single pole filter cutoff frequency, f_c, extends the corner frequency to $1.57f_c$. Similarly, a two pole filter has an apparent corner frequency of approximately $1.2f_c$. The error correction factor is usually negligible for filters having more than two poles. The net bandwidth after the correction is referred to as the filter *equivalent noise bandwidth* (see Figure 1-72 opposite).

It is often desirable to convert RMS noise measurements into peak-to-peak. In order to do this, one must have some understanding of the statistical nature of noise. For Gaussian noise and a given value of RMS noise, statistics tell us that the chance of a particular peak-to-peak value being exceeded decreases sharply as that value increases— but this probability never becomes zero.

Thus, for a given RMS noise, it is possible to predict the percentage of time that a given peak-to-peak value will be exceeded, but it is not possible to give a peak-to-peak value which will never be exceeded as shown in Figure 1-73 below.

Nominal Peak-to-Peak	% of the Time Noise will Exceed Nominal Peak-to-Peak Value
2 × rms	32%
3 × rms	13%
4 × rms	4.6%
5 × rms	1.2%
6 × rms	0.27%
6.6 × rms**	0.10%
7 × rms	0.046%
8 × rms	0.006%

Most often used conversion factor is 6.6

Figure 1-73: RMS to peak-to-peak ratios

Peak-to-peak noise specifications, therefore, must always be written with a time limit. A suitable one is 6.6 times the RMS value, which is exceeded only 0.1% of the time.
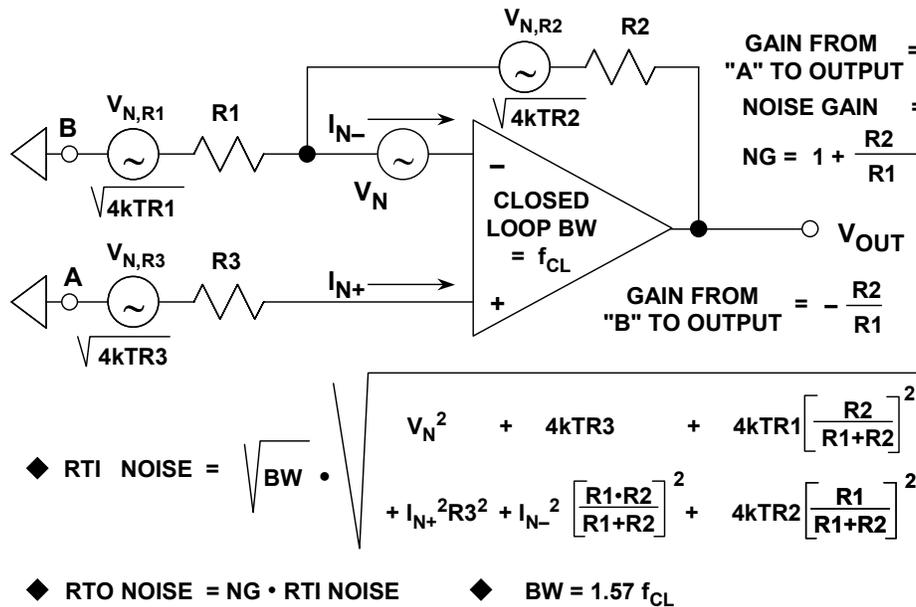
Total Output Noise Calculations

We have already pointed out that any noise source which produces less than one third to one fifth of the noise of some greater source can be ignored, with little error. When so doing, both noise voltages must be measured at the same point in the circuit. To analyze the noise performance of an op amp circuit, we must assess the noise contributions of each part of the circuit, and determine which are significant. To simplify the following calculations, we shall work with noise spectral densities, rather than actual voltages, to

leave bandwidth out of the expressions (the noise spectral density, which is generally expressed in nV/√Hz, is equivalent to the noise in a 1Hz bandwidth).

If we consider the circuit in Figure 1-74 below, which is an amplifier consisting of an op amp and three resistors (R3 represents the source resistance at node A), we can find six separate noise sources: the Johnson noise of the three resistors, the op amp voltage noise, and the current noise in each input of the op amp. Each source has its own contribution to the noise at the amplifier output. Noise is generally specified RTI, or *referred to the input*, but it is often simpler to calculate the noise referred to the output (RTO) and then divide it by the *noise* gain (not the *signal* gain) of the amplifier to obtain the RTI noise.

GAIN FROM "A" TO OUTPUT =

NOISE GAIN =

$$NG = 1 + \frac{R2}{R1}$$

$$\text{GAIN FROM "B" TO OUTPUT} = -\frac{R2}{R1}$$

$$\blacklozenge \text{ RTI NOISE} = \sqrt{BW} \cdot \sqrt{V_N{}^2 + 4kTR3 + 4kTR1\left[\frac{R2}{R1+R2}\right]^2 + I_{N+}{}^2 R3^2 + I_{N-}{}^2\left[\frac{R1 \cdot R2}{R1+R2}\right]^2 + 4kTR2\left[\frac{R1}{R1+R2}\right]^2}$$

$\blacklozenge$ **RTO NOISE = NG • RTI NOISE** $\blacklozenge$ **BW = 1.57 f$_{CL}$**

Figure 1-74: Op amp noise model for single pole system

Figure 1-75 (opposite) is a detailed analysis of how each of the noise sources in Fig. 1-74 is reflected to the output of the op amp. Some further discussion regarding the effect of the current noise at the inverting input is warranted. This current, I_{N-}, does not flow in R1, as might be expected— the negative feedback around the amplifier works to keep the potential at the inverting input unchanged, so that a current flowing from that pin is forced, by negative feedback, to flow in R2 only, resulting in a voltage at the output of I_{N-} R2. We could equally well consider the voltage caused by I_{N-} flowing in the parallel combination of R1 and R2 and then amplified by the noise gain of the amplifier, but the results are identical— only the calculations are more involved.

Notice that the Johnson noise voltage associated with the three resistors has been included in the expressions of Fig. 1-75. All resistors have a Johnson noise of √(4kTBR), where k is Boltzmann's Constant (1.38×10^{-23} J/K), T is the absolute temperature, B is the bandwidth in Hz, and R is the resistance in Ω. A simple relationship which is easy to remember is that a 1000Ω resistor generates a Johnson noise of 4nV/√Hz at 25°C.

The analysis so far assumes that the feedback network is purely resistive and that the noise gain versus frequency is flat. This applies to most applications, but if the feedback network contains reactive elements (usually capacitors) the noise gain is not constant

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over the bandwidth of interest, and more complex techniques must be used to calculate the total noise (see in particular, Reference 2 and Chapter 4, Section 4-4 of this book).

NOISE SOURCE EXPRESSED AS A VOLTAGE	MULTIPLY BY THIS FACTOR TO REFER TO THE OP AMP OUTPUT
Johnson noise in R3: $\sqrt{(4kTR3)}$	Noise Gain = 1 + R2/R1
Non-inverting input current noise flowing in R3: $I_{N+}R3$	Noise Gain = 1 + R2/R1
Input voltage noise: V_N	Noise Gain = 1 + R2/R1
Johnson noise in R1: $\sqrt{(4kTR1)}$	–R2/R1 (Gain from input of R1 to output)
Johnson noise in R2: $\sqrt{(4kTR2)}$	1
Inverting input current noise flowing in R2: $I_{N-}R2$	1

Figure 1-75: Noise sources referred to the output (RTO)

The circuit shown in Figure 1-76 below represents a second-order system, where capacitor C1 represents the source capacitance, stray capacitance on the inverting input, the input capacitance of the op amp, or any combination of these. C1 causes a breakpoint in the noise gain, and C2 is the capacitor that must be added to obtain stability.
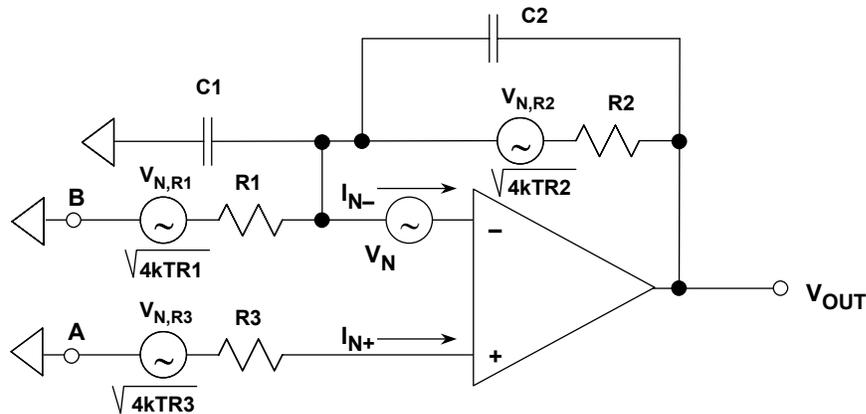
Figure 1-76: Op amp noise model with reactive elements (second-order system)

Because of C1 and C2, the noise gain is a function of frequency, and has peaking at the higher frequencies (assuming C2 is selected to make the second-order system critically damped). Textbooks state that a flat noise gain can be achieved if one simply makes R1C1 = R2C2.

But in the case of current-to-voltage converters, however, R1 is typically a high impedance, and the method doesn't work. Maximizing the signal bandwidth in these situations is somewhat complex and is treated in detail in Section 1-6 of this chapter and in Chapter 4, Section 4-4 of this book.

A DC signal applied to input A (B being grounded) sees a gain of $1 + R2/R1$, the low frequency noise gain. At higher frequencies, the gain from input A to the output becomes $1 + C1/C2$ (the high frequency noise gain).

The closed-loop bandwidth f_{cl} is the point at which the noise gain intersects the open-loop gain. A DC signal applied to B (A being grounded) sees a gain of $-R2/R1$, with a high frequency cutoff determined by R2-C2. Bandwidth from B to the output is $1/2\pi R2C2$.

The current noise of the non-inverting input, I_{N+}, flows in R3 and gives rise to a noise voltage of $I_{N+}R3$, which is amplified by the frequency-dependent noise gain, as are the op amp noise voltage, V_N, and the Johnson noise of R3, which is $\sqrt{(4kTR3)}$. The Johnson noise of R1 is amplified by $-R2/R1$ over a bandwidth of $1/2\pi R2C2$, and the Johnson noise of R2 is not amplified at all but is connected directly to the output over a bandwidth of $1/2\pi R2C2$. The current noise of the inverting input, I_{N-}, flows in R2 only, resulting in a voltage at the amplifier output of $I_{N-}R2$ over a bandwidth of $1/2\pi R2C2$.

If we consider these six noise contributions, we see that if R1, R2, and R3 are low, then the effect of current noise and Johnson noise will be minimized, and the dominant noise will be the op amp's voltage noise. As we increase resistance, both Johnson noise and the voltage noise produced by noise currents will rise.

If noise currents are low, then Johnson noise will take over from voltage noise as the dominant contributor. Johnson noise, however, rises with the square root of the resistance, while the current noise voltage rises linearly with resistance, so ultimately, as the resistance continues to rise, the voltage due to noise currents will become dominant.

These noise contributions we have analyzed are not affected by whether the input is connected to node A or node B (the other being grounded or connected to some other low-impedance voltage source), which is why the non-inverting gain ($1 + Z2/Z1$), which is seen by the voltage noise of the op amp, V_N, is known as the "noise gain".

Calculating the total output RMS noise of the second-order op amp system requires multiplying each of the six noise voltages by the appropriate gain and integrating over the appropriate frequency as shown in Figure 1-77 (opposite).

The root-sum-square of all the output contributions then represents the total RMS output noise. Fortunately, this cumbersome exercise may be greatly simplified in most cases by making the appropriate assumptions and identifying the chief contributors.

NOISE SOURCE EXPRESSED AS A VOLTAGE	MULTIPLY BY THIS FACTOR TO REFER TO OUTPUT	INTEGRATION BANDWIDTH
Johnson noise in R3: $\sqrt{(4kTR3)}$	Noise Gain as a function of frequency	Closed-Loop BW
Non-inverting input current noise flowing in R3: $I_{N+}R3$	Noise Gain as a function of frequency	Closed-Loop BW
Input voltage noise: V_N	Noise Gain as a function of frequency	Closed-Loop BW
Johnson noise in R1: $\sqrt{(4kTR1)}$	–R2/R1 (Gain from B to output)	$1/2\pi R2C2$
Johnson noise in R2: $\sqrt{(4kTR2)}$	1	$1/2\pi R2C2$
Inverting input current noise flowing in R2: $I_{N-}R2$	1	$1/2\pi R2C2$

Figure 1-77: Noise sources referred to the output for a second-order system

Although shown before, the noise gain for a typical second-order system is repeated in Figure 1-78 below. It is quite easy to perform the voltage noise integration in two steps, but notice that because of peaking, the majority of the output noise due to the input voltage noise will be determined by the high frequency portion where the noise gain is 1 + C1/C2. This type of response is typical of second-order systems.
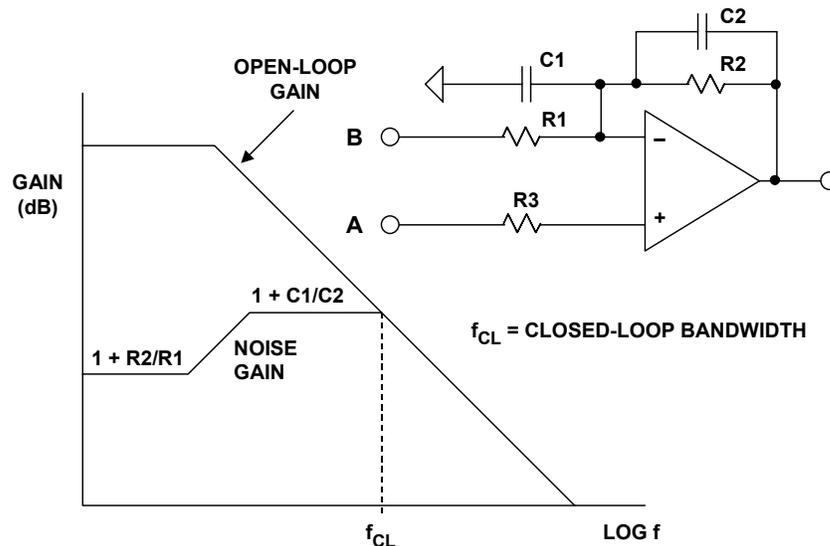
Figure 1-78: Noise gain of a typical second-order system

The noise due to the inverting input current noise, R1, and R2 is only integrated over the bandwidth $1/2\pi R2C2$.

Op Amp Distortion

Dynamic range of an op amp may be defined in several ways. The most common ways are to specify *harmonic distortion*, *total harmonic distortion* (THD), or *total harmonic distortion plus noise* (THD + N).

Other specifications related specifically to communications systems such as *intermodulation distortion* (IMD), *intercept points* (IP), *spurious free dynamic range* (SFDR), *multitone power ratio* (MTPR) and others are covered thoroughly in Chapter 6, Section 6-4. In this section, only harmonic distortion, THD, and THD + N will be covered.

The distortion components which makes up total harmonic distortion is usually calculated by taking the root sum of the squares of the first five or six harmonics of the fundamental. In many practical situations, however, there is negligible error if only the second and third harmonics are included. The definition of THD and THD + N is shown in Figure 1-79 below.

◆ V_s = Signal Amplitude (RMS Volts)

◆ V_2 = Second Harmonic Amplitude (RMS Volts)

◆ V_n = nth Harmonic Amplitude (RMS Volts)

◆ V_{noise} = RMS value of noise over measurement bandwidth

◆ $$THD + N = \frac{\sqrt{V_2{}^2 + V_3{}^2 + V_4{}^2 + \ldots + V_n{}^2 + V_{noise}{}^2}}{V_s}$$

◆ $$THD = \frac{\sqrt{V_2{}^2 + V_3{}^2 + V_4{}^2 + \ldots + V_n{}^2}}{V_s}$$

Figure 1-79: Definitions of THD and THD + N

It is important to note that the THD measurement does not include noise terms, while THD + N does. The noise in the THD + N measurement must be integrated over the measurement bandwidth. In audio applications, the bandwidth is normally chosen to be around 100kHz. In narrow-band applications, the level of the noise may be reduced by filtering.

On the other hand, harmonics and intermodulation products which fall within the measurement bandwidth cannot be filtered, and therefore may limit the system dynamic range.
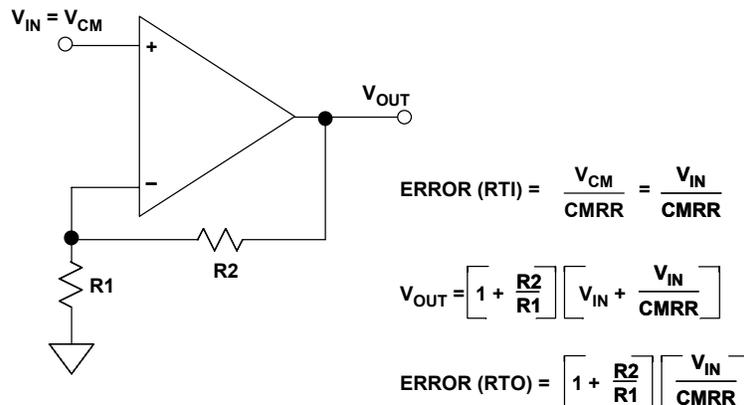
Common-Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio (PSRR)

If a signal is applied equally to both inputs of an op amp, so that the differential input voltage is unaffected, the output should not be affected. In practice, changes in common-mode voltage will produce changes in output. The op amp *common-mode rejection ratio* (CMRR) is the ratio of the common-mode gain to differential-mode gain. For example, if a differential input change of Y volts produces a change of 1V at the output, and a common-mode change of X volts produces a similar change of 1V, then the CMRR is X/Y. When the common-mode rejection ratio is expressed in dB, it is generally referred to as common-mode rejection (CMR). Typical LF CMR values are between 70 and 120dB, but at higher frequencies, CMR deteriorates. Many op amp data sheets show a plot of CMR versus frequency, as shown in Figure 1-80 for an OP177 op amp.

$$CMR = 20 \log_{10} CMRR$$
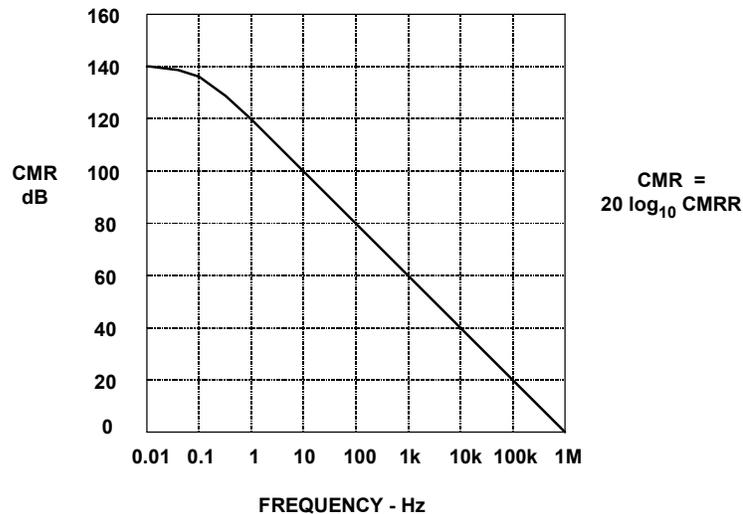
Figure 1-80: OP177 common-mode rejection (CMR)

CMRR produces a corresponding output offset voltage error in op amps configured in the non-inverting mode as shown in Figure 1-81 below.
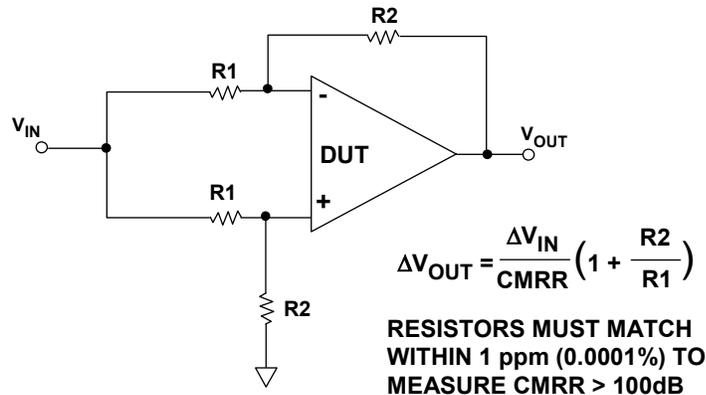

$$ERROR\ (RTI) = \frac{V_{CM}}{CMRR} = \frac{V_{IN}}{CMRR}$$

$$V_{OUT} = \left[1 + \frac{R2}{R1}\right]\left[V_{IN} + \frac{V_{IN}}{CMRR}\right]$$

$$ERROR\ (RTO) = \left[1 + \frac{R2}{R1}\right]\left[\frac{V_{IN}}{CMRR}\right]$$

Figure 1-81: Calculating offset error due to common-mode rejection ratio (CMRR)

Note inverting mode operating op amps will have negligible CMRR error, as both inputs are held at a ground (or virtual ground), i.e., there is no CM dynamic voltage.

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Common-mode rejection ratio can be measured in several ways. The method shown in Figure 1-82 below uses four precision resistors to configure the op amp as a differential amplifier, a signal is applied to both inputs, and the change in output is measured— an amplifier with infinite CMRR would have no change in output. The disadvantage inherent in this circuit is that the ratio match of the resistors is as important as the CMRR of the op amp. A mismatch of 0.1% between resistor pairs will result in a CMR of only 66dB— no matter how good the op amp! Since most op amps have a LF CMR of between 80 and 120dB, it is clear that this circuit is only marginally useful for measuring CMRR (although it does an excellent job in measuring the matching of the resistors!).

$$\Delta V_{OUT} = \frac{\Delta V_{IN}}{CMRR}\left(1 + \frac{R2}{R1}\right)$$

RESISTORS MUST MATCH WITHIN 1 ppm (0.0001%) TO MEASURE CMRR > 100dB

*Figure 1-82: Simple common-mode rejection ratio (CMRR) test circuit*

The slightly more complex circuit shown in Figure 1-83 below measures CMRR without requiring accurately matched resistors. In this circuit, the common-mode voltage is changed by switching the power supply voltages. (This is easy to implement in a test facility, and the same circuit with different supply voltage connections can be used to measure power supply rejection ratio).

$$CMRR = 101\left|\frac{20V}{\Delta V_{OUT}}\right|$$

A1: HIGH GAIN, LOW V_{OS}, LOW I_B
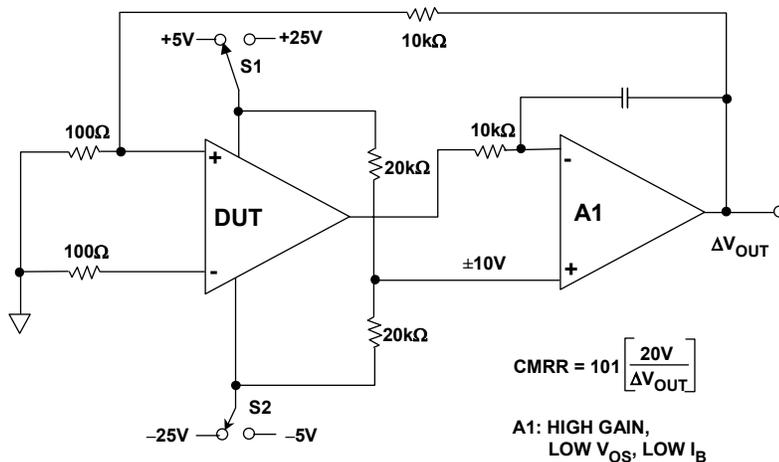
Figure 1-83: CMRR test circuit does not require precision resistors

The power supply values shown in the circuit are for a ±15V DUT op amp, with a common-mode voltage range of ±10V. Other supplies and common-mode ranges can also be accommodated by changing voltages, as appropriate. The integrating amplifier A1 should have high gain, low V_{OS} and low I_B, such as an OP97 family device.

If the supply of an op amp changes, its output should not, but it does. The specification of *power supply rejection ratio* or PSRR is defined similarly to the definition of CMRR. If a change of X volts in the supply produces the same output change as a differential input change of Y volts, then the PSRR on that supply is X/Y. The definition of PSRR assumes that both supplies are altered equally in opposite directions—otherwise the change will introduce a common-mode change as well as a supply change, and the analysis becomes considerably more complex. It is this effect which causes apparent differences in PSRR between the positive and negative supplies.
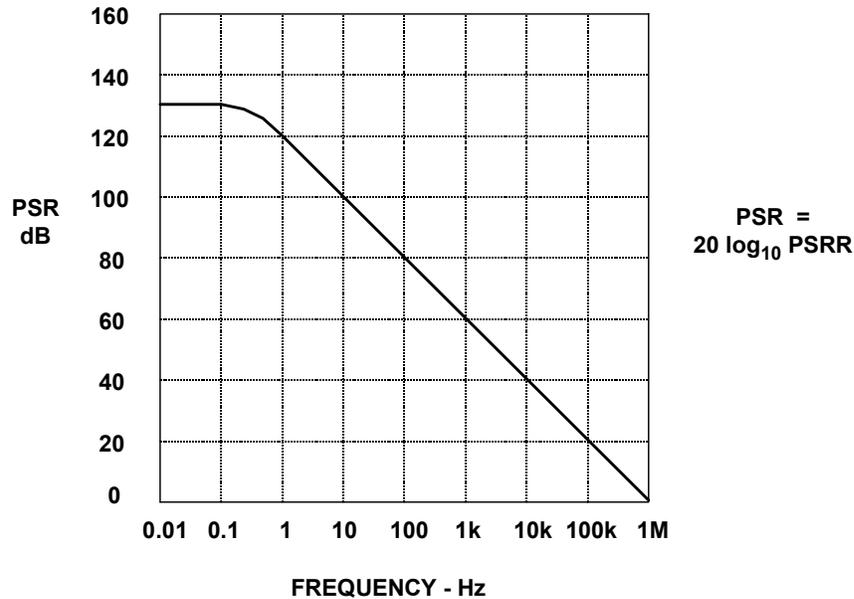
Figure 1-84: *OP177 power supply rejection*

Typical PSR for the OP177 is shown in Figure 1-84 above.

The test setup used to measure CMRR may be modified to measure PSRR as shown in Figure 1-85 below.


$$PSRR = 101 \left| \frac{1V}{\Delta V_{OUT}} \right|$$

A1: HIGH GAIN, LOW V_{OS}, LOW I_B
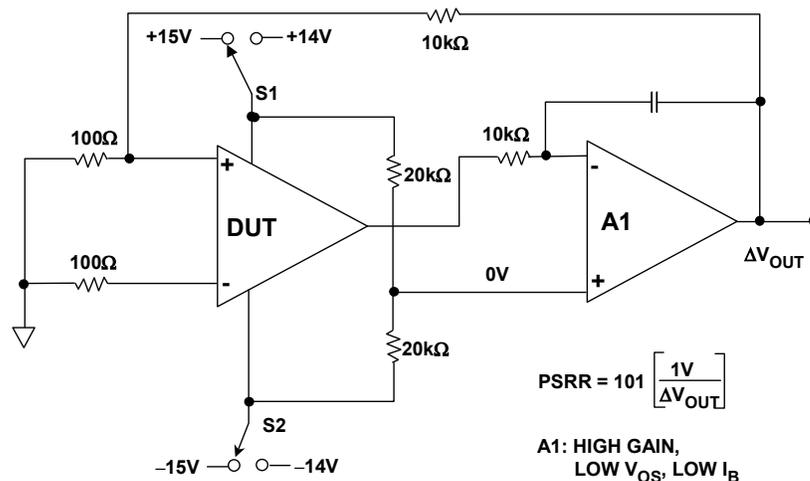
Figure 1-85: *Test setup for measuring power supply rejection ratio (PSRR)*
The voltages are chosen for a symmetrical power supply change of 1V. Other values may be used where appropriate.

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Power Supplies and Decoupling

Because op amp PSRR is frequency dependent, op amp power supplies must be well decoupled. At low frequencies, several devices may share a 10-50µF capacitor on each supply, provided it is no more than 10cm (PC track distance) from any of them.
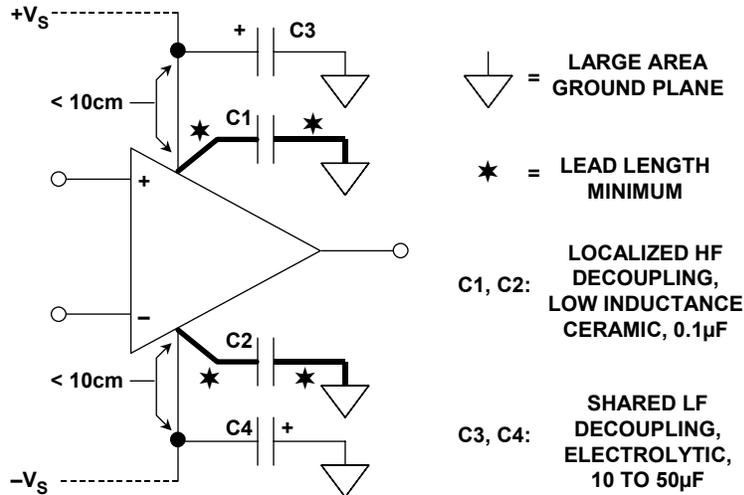
Figure 1-86: Proper low and high-frequency decoupling techniques for op amps

At high frequencies, each IC should have the supply leads decoupled by a low inductance 0.1µF (or so) capacitor with short leads/PC tracks. These capacitors must also provide a return path for HF currents in the op amp load. Typical decoupling circuits are shown in Figure 1-86 above. Further bypassing and decoupling information is found Chapter 7.

Power Supplies and Power Dissipation

Op amps have no ground terminal. Specifications of power supply are quite often in the form ±X Volts, but in fact it might equally be expressed as 2X Volts. What is important is where the CM and output ranges lie relative to the supplies. This information may be provided in tabular form or as a graph.

Often data sheets will advise that an op amp will work over a range of supplies (from +3 to ±16.5V for example), and will then give parameters at several values of supply, so that users may extrapolate. If the minimum supply is quite high, it is usually because the device uses a structure requiring a threshold voltage to function (zener diode).

Data sheets also give current consumption. Any current flowing into one supply pin will flow out of the other or out of the output terminal. When the output is open circuit, the dissipation is easily calculated from the supply voltage and current. When current flows in a load, it is easiest to calculate the total dissipation (remember that if the load is grounded to the center rail the load current flows from a supply to ground, not between supplies), and then subtract the load dissipation to obtain the device dissipation. Data sheets normally give details of thermal resistances and maximum junction temperature ratings, from which dissipation limits may be calculated knowing conditions. Details of further considerations relating to power dissipation, heatsinking, etc., can be found in Chapter 7, Section 7-5.

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NOTES:

SECTION 1-5: PRECISION OP AMPS
Walt Kester, Walt Jung

This section examines in more detail some of the issues relating to amplifiers for use in precision signal conditioning applications. Although the OP177 op amp is used for the "gold standard" for precision in these discussions, more recent product introductions such as the rail-to-rail output OP777, OP727, and OP747, along with the OP1177, OP2177, and OP4177 offer nearly as good performance in smaller packages.

Precision op amp open-loop gains greater than 1 million are available, along with common-mode and power supply rejection ratios of the same magnitude. Offset voltages of less than 25µV and offset drift less than 0.1µV/°C are available in dual supply op amps such as the OP177, however, the performance in single-supply precision bipolar op amps may sometimes fall short of this performance. This is the tradeoff that must sometimes be made in low power, low voltage applications. On the other hand, however, modern chopper stabilized op amps provide offsets and offset voltage drifts which cannot be distinguished from noise, and these devices operate on single supplies and provide rail-to-rail inputs and outputs. They too come with their own set of problems that are discussed later within this section.

It is important to understand that DC open-loop gain, offset voltage, power supply rejection (PSR), and common-mode rejection (CMR) alone shouldn't be the only considerations in selecting precision amplifiers. The AC performance of the amplifier is also important, even at "low" frequencies. Open-loop gain, PSR, and CMR all have relatively low corner frequencies, and therefore what may be considered "low" frequency may actually fall above these corner frequencies, increasing errors above the value predicted solely by the DC parameters. For example, an amplifier having a DC open-loop gain of 10 million and a unity-gain crossover frequency of 1MHz has a corresponding corner frequency of 0.1Hz! One must therefore consider the open-loop gain at the actual *signal* frequency. The relationship between the single-pole unity-gain crossover frequency, f_u, the signal frequency, f_{sig}, and the open-loop gain $A_{VOL(fsig)}$ (measured at the signal frequency is given by:

$$A_{VOL(f_{sig})} = \frac{f_u}{f_{sig}}.$$
<div align="right">Eq. 1-31</div>

It the example above, the open-loop gain is 10 at 100kHz, and 100,000 at 10Hz. Note that the constant gain-bandwidth product concept only holds true for VFB op amps. It doesn't apply to CFB op amps, but then they are rarely used in precision applications.

Loss of open-loop gain at the frequency of interest can introduce distortion, especially at audio frequencies. Loss of CMR or PSR at the line frequency or harmonics thereof can also introduce errors.

The challenge of selecting the right amplifier for a particular signal conditioning application has been complicated by the sheer proliferation of various types of amplifiers in various processes (Bipolar, Complementary Bipolar, BiFET, CMOS, BiCMOS, etc.) and architectures (traditional op amps, instrumentation amplifiers, chopper amplifiers, isolation amplifiers, etc.)

In addition, a wide selection of precision amplifiers are now available which operate on single-supply voltages which complicates the design process even further because of the reduced signal swings and voltage input and output restrictions. Offset voltage and noise are now a more significant portion of the input signal.

◆ **Input Offset Voltage**   **<100µV**

◆ **Input Offset Voltage Drift**   **<1µV/°C**

◆ **Input Bias Current**   **<2nA**

◆ **Input Offset Current**   **<2nA**

◆ **DC Open Loop Gain**   **>1,000,000**

◆ **Unity Gain Bandwidth Product, f_u**   **500kHz - 5MHz**

◆ **Always Check Open Loop Gain at Signal Frequency!**

◆ **1/f (0.1Hz to 10Hz) Noise**   **<1µV p-p**

◆ **Wideband Noise**   **<10nV/√Hz**

◆ **CMR, PSR**   **>100dB**

◆ **Tradeoffs:**

    ● **Single supply operation**

    ● **Low supply currents**
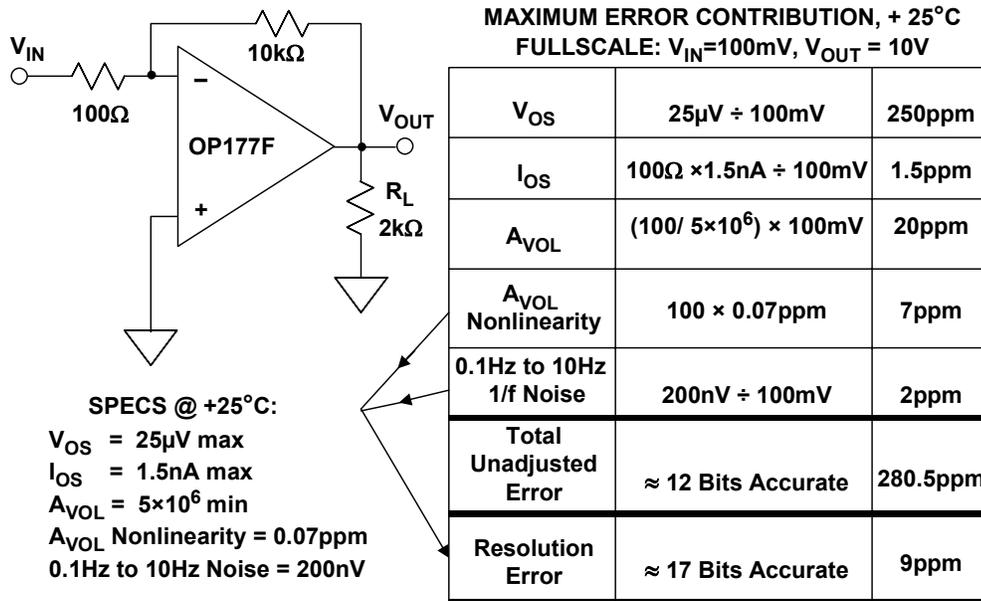
Figure 1-87: Precision op amp characteristics

Selection guides and parametric search engines, which can simplify this process somewhat, are available on the world-wide-web (http://www.analog.com) as well as on CDROM. Some general attributes of precision op amps are summarized in Figure 1-87.

Precision Op Amp Amplifier DC Error Budget Analysis

In order to develop a concept for the magnitudes of the various errors in a high precision op amp circuit, a simple room temperature analysis for the OP177F is shown on the opposite page, in Figure 1-88. The amplifier is connected in the inverting mode with a signal gain of 100. The key data sheet specifications are also shown in the diagram. We assume an input signal of 100mV fullscale which corresponds to an output signal of 10V. The various error sources are normalized to fullscale and expressed in parts per million (ppm). Note: parts per million (ppm) error = fractional error $\times 10^6$ = % error $\times 10^4$.

Note that the offset errors due to V_{OS} and I_{OS} and the gain error due to finite A_{VOL} can be removed with a system calibration. However, the error due to open-loop gain nonlinearity cannot be removed with calibration and produces a relative accuracy error, often called *resolution error*.

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A second contributor to resolution error is the 1/f noise. This noise is always present and adds to the uncertainty of the measurement. The overall relative accuracy of the circuit at room temperature is 9ppm, equivalent to ~17 bits of resolution.

MAXIMUM ERROR CONTRIBUTION, + 25°C FULLSCALE: V_{IN}=100mV, V_{OUT} = 10V		
V_{OS}	25µV ÷ 100mV	250ppm
I_{OS}	100Ω ×1.5nA ÷ 100mV	1.5ppm
A_{VOL}	(100/ 5×10⁶) × 100mV	20ppm
A_{VOL} Nonlinearity	100 × 0.07ppm	7ppm
0.1Hz to 10Hz 1/f Noise	200nV ÷ 100mV	2ppm
Total Unadjusted Error	≈ 12 Bits Accurate	280.5ppm
Resolution Error	≈ 17 Bits Accurate	9ppm

SPECS @ +25°C:

V_{OS} = 25µV max
I_{OS} = 1.5nA max
A_{VOL} = 5×10⁶ min
A_{VOL} Nonlinearity = 0.07ppm
0.1Hz to 10Hz Noise = 200nV

Figure 1-88: Precision op amp (OP177F) DC error budget analysis

It is also useful to compare the performance of a number of single-supply op amps to that of the "gold standard" OP177, and this is done in Figure 1-89 below for some representative devices.

LISTED IN ORDER OF INCREASING SUPPLY CURRENT

PART NO.	V_{OS} max	V_{OS} TC	A_{VOL}min	NOISE (1kHz)	INPUT	OUTPUT	I_{SY}/AMP MAX
OP293	250µV	2µV/°C	200k	5nV/√Hz	0, 4V	5mV, 4V	20µA
OP196/296/496	300µV	2µV/°C	150k	26nV/√Hz	R/R	"R/R"	60µA
OP777	100µV	1.3µV/°C	300k	15nV√Hz	0, 4V	"R/R"	270µA
OP191/291/491	700µV	5µV/°C	25k	35nV/√Hz	R/R	"R/R"	350µA
*AD820/822/824	1000µV	20µV/°C	500k	16nV/√Hz	0, 4V	"R/R"	800µA
**AD8601/2/4	600µV	2µV/°C	20k	33nV/√Hz	R/R	"R/R"	1000µA
OP184/284/484	150µV	2µV/°C	50k	3.9nV/√Hz	R/R	"R/R"	1350µA
OP113/213/413	175µV	4µV/°C	2M	4.7nV/√Hz	0, 4V	5mV, 4V	3000µA
OP177F (±15V)	25µV	0.1µV/°C	5M	10nV/√Hz	N/A	N/A	2000µA

*JFET INPUT   **CMOS

NOTE: Unless Otherwise Stated
Specifications are Typical @ +25°C
V_S = +5V

Figure 1-89: Precision single-supply op amp performance characteristics

Note that the Fig. 1-89 amplifier list does *not* include the category of chopper op amps, which excel in many of the categories. These are covered separately, immediately below.

Chopper Stabilized Amplifiers

For the lowest offset and drift performance, chopper-stabilized amplifiers may be the only solution. The best bipolar amplifiers offer offset voltages of 25µV and 0.1µV/°C drift. Offset voltages less than 5µV with practically no measurable offset drift are obtainable with choppers, albeit with some penalties.

A basic chopper amplifier circuit is shown in Figure 1-90 below. When the switches are in the "Z" (auto-zero) position, capacitors C2 and C3 are charged to the amplifier input and output offset voltage, respectively. When the switches are in the "S" (sample) position, V_{IN} is connected to V_{OUT} through the path comprised of R1, R2, C2, the amplifier, C3, and R3. The chopping frequency is usually between a few hundred Hz and several kHz, and it should be noted that because this is a sampling system, the input frequency must be much less than one-half the chopping frequency in order to prevent errors due to aliasing. The R1-C1 combination serves as an antialiasing filter. It is also assumed that after a steady state condition is reached, there is only a minimal amount of charge transferred during the switching cycles. The output capacitor, C4, and the load, R_L, must be chosen such that there is minimal V_{OUT} droop during the auto-zero cycle.
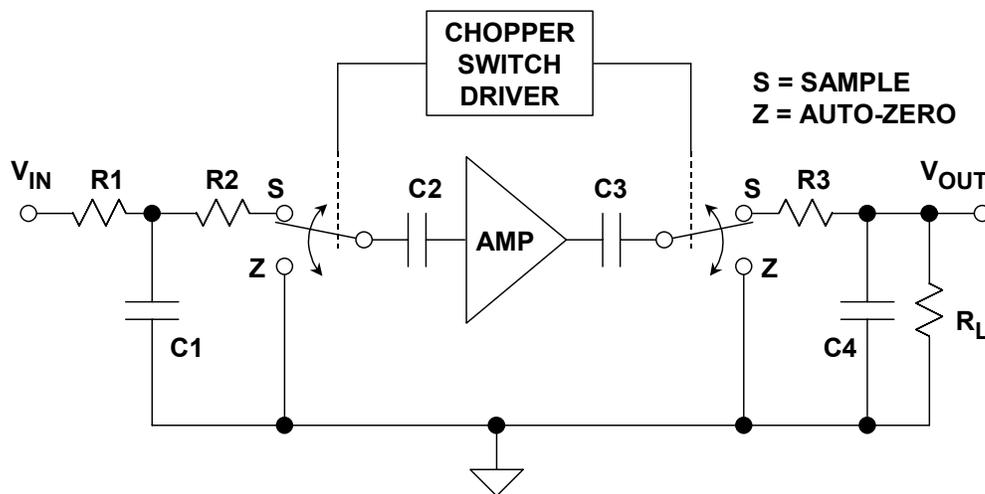

Figure 1-90: *Classic chopper amplifier*

The basic chopper amplifier of Fig. 1-90 can pass only very low frequencies because of the input filtering required to prevent aliasing. In contrast to this, the *chopper-stabilized* architecture shown in Figure 1-91 (opposite) is most often used in chopper amplifier implementations. In this circuit, A1 is the *main* amplifier, and A2 is the *nulling* amplifier. In the sample mode (switches in "S" position), the nulling amplifier, A2, monitors the input offset voltage of A1 and drives its output to zero by applying a suitable correcting voltage at A1's null pin. Note, however, that A2 also has an input offset voltage, so it must correct its own error before attempting to null A1's offset. This is achieved in the auto-zero mode (switches in "Z" position) by momentarily disconnecting A2 from A1, shorting its inputs together, and coupling its output to its own null pin. During the auto-zero mode, the correction voltage for A1 is momentarily held by C1. Similarly, C2 holds the correction voltage for A2 during the sample mode. In modern IC chopper-stabilized op amps, the storage capacitors C1 and C2 are on-chip.

Note in this architecture that *the input signal is always connected to the output, through A1*. The bandwidth of A1 thus determines the overall signal bandwidth, and the input signal is not limited to less than one-half the chopping frequency as in the case of the traditional chopper amplifier architecture. However, the switching action does produce small transients at the chopping frequency, that can mix with the input signal frequency and produce intermodulation distortion.
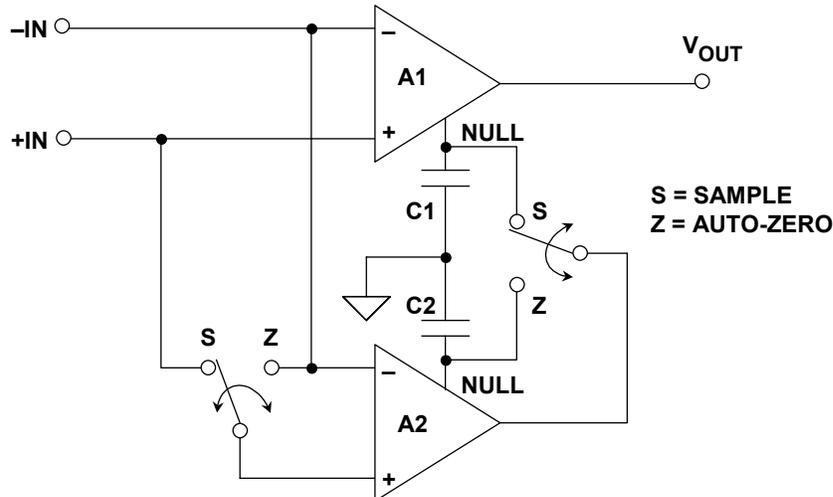
Figure 1-91: *Modern chopper stabilized op amp*

A patented spread-spectrum technique is used in the AD8571/72/74 series of single-supply chopper-stabilized op amps, to virtually eliminate intermodulation effects.
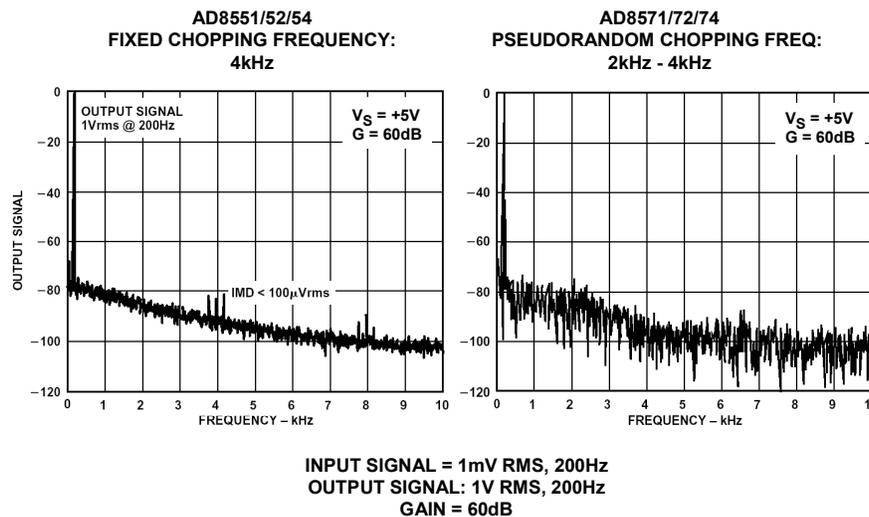

Figure 1-92: *Intermodulation product: fixed versus pseudorandom chopping frequency*

These devices use a pseudorandom chopping frequency swept between 2kHz and 4kHz. Figure 1-92 above compares the intermodulation distortion of a traditional chopper stabilized op amp (AD8551/52/54, left) that uses a fixed 4kHz chopping frequency to that of the AD8571/72/74 (right) that uses the pseudorandom chopping frequency.

1.99

A comparison between fixed and pseudorandom chopping on the voltage noise is shown in Figure 1-93 below. Notice for the fixed chopping frequency, there are distinct peaks in the noise spectrum at the odd harmonics of 4kHz, whereas with pseudorandom chopping, the spectrum is much more uniform, although the average noise level is higher.
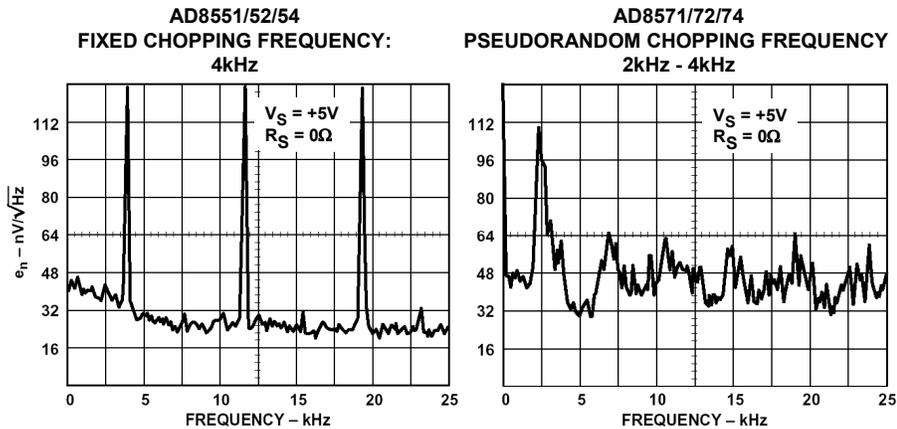
Figure 1-93: *Voltage noise spectral density comparison: fixed versus pseudorandom chopping frequency*

The AD8571/8572/8574 family of chopper-stabilized op amps offers rail-to-rail input and output single-supply operation, low offset voltage, and low offset drift. As discussed above, the pseudorandom chopping frequency minimizes intermodulation distortion with the input signal. The storage capacitors are internal to the IC, and no external capacitors other than standard decoupling capacitors are required. Key specifications for the devices are given in Figure 1-94 below.

◆ **Single Supply: +2.7V to +5V**

◆ **1µV Typical Input Offset Voltage**

◆ **0.005µV/°C Typical Input Offset Voltage Drift**

◆ **130dB CMR, PSR**

◆ **750µA Supply Current / Op Amp**

◆ **50µs Overload Recovery Time**

◆ **50nV/√Hz Input Voltage Noise**

◆ **Pseudorandom Chopping Frequency**

◆ **1.5MHz Gain-Bandwidth Product**

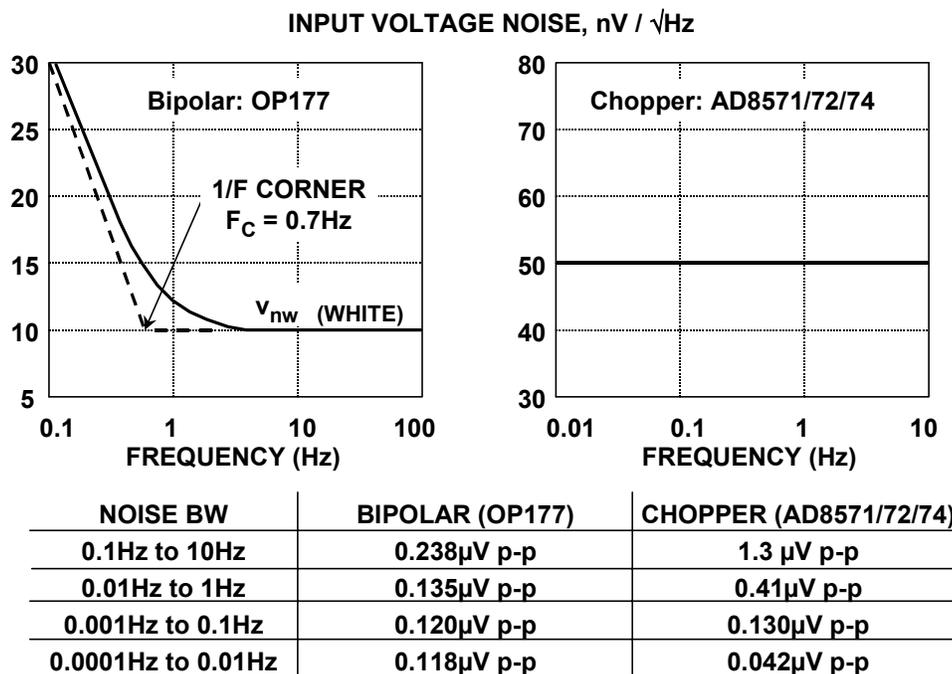◆ **Single (AD8571), Dual (AD8572) and Quad (AD8574)**

Figure 1-94: *AD8571/72/74 chopper stabilized rail-to-rail input/output amplifiers*

It should be noted that extreme care must be taken when applying all of the chopper stabilized devices. This is because in order to fully realize the full offset and drift performance inherent to the parts, parasitic thermocouple effects in external circuitry must be avoided. See Chapter 4, Section 4-5 for a general discussion of thermocouples, and Chapter 7, Section 7-1 related to passive components.

Noise Considerations for Chopper-Stabilized Op Amps

It is interesting to consider the effects of a chopper amplifier on low frequency 1/f noise. If the chopping frequency is considerably higher than the 1/f corner frequency of the input noise, the chopper-stabilized amplifier continuously nulls out the 1/f noise on a sample-by-sample basis. Theoretically, a chopper op amp therefore has no 1/f noise. However, the chopping action produces wideband noise which is generally much worse than that of a precision bipolar op amp.

Figure 1-95 below shows the noise of a precision bipolar amplifier (OP177) versus that of the AD8571/72/74 chopper-stabilized op amp. The peak-to-peak noise in various bandwidths is calculated for each in the table below the graphs.

INPUT VOLTAGE NOISE, nV / √Hz

NOISE BW	BIPOLAR (OP177)	CHOPPER (AD8571/72/74)
0.1Hz to 10Hz	0.238µV p-p	1.3 µV p-p
0.01Hz to 1Hz	0.135µV p-p	0.41µV p-p
0.001Hz to 0.1Hz	0.120µV p-p	0.130µV p-p
0.0001Hz to 0.01Hz	0.118µV p-p	0.042µV p-p

Figure 1-95: Noise: bipolar versus chopper stabilized op amp

Note from the data that as the frequency is lowered, the chopper amplifier noise continues to drop, while the bipolar amplifier noise approaches a limit determined by the 1/f corner frequency and its white noise. Notice that only at very low frequencies (<0.01Hz) is the chopper noise performance superior to that of the bipolar op amp.

In order to take advantage of the chopper op amp's lack of 1/f noise, much filtering is required— otherwise the total noise of a chopper will always be worse than a good bipolar op amp. Choppers should therefore be selected on the basis of their low offset and drift— not because of their lack of 1/f noise.

REFERENCES: PRECISION OP AMPS

1.   Walt Kester, Editor, **1992 Amplifier Applications Guide**, Analog Devices, 1992, ISBN: 0-916550-10-9.

2.   Walt Kester, Editor, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, 1999, ISBN: 0-916550-20-6.

3.   Data Sheet for **AD8551/AD8552/AD8554 Zero-Drift, Single-Supply, Rail-to-Rail Input/Output Operational Amplifiers,** http://www.analog.com

4.   Data Sheet for **AD8571/AD8572/AD8574 Zero-Drift, Single-Supply, Rail-to-Rail Input/Output Operational Amplifiers**, http://www.analog.com

5.   Data Sheet for **OP777/OP727/OP747 Precision Micropower Single-Supply Operational Amplifiers,** http://www.analog.com

6.   Data Sheet for **OP1177/OP2177/OP4177 Precision Low Noise, Low Input Bias Current Operational Amplifiers,** http://www.analog.com

SECTION 1-6: HIGH SPEED OP AMPS
Walt Kester

Introduction

High speed analog signal processing applications, such as video and communications, require op amps which have wide bandwidth, fast settling time, low distortion and noise, high output current, good DC performance, and operate at low supply voltages. These devices are widely used as gain blocks, cable drivers, ADC pre-amps, current-to-voltage converters, etc. Achieving higher bandwidths for less power is extremely critical in today's portable and battery-operated communications equipment. The rapid progress made over the last few years in high speed linear circuits has hinged not only on the development of IC processes but also on innovative circuit topologies.
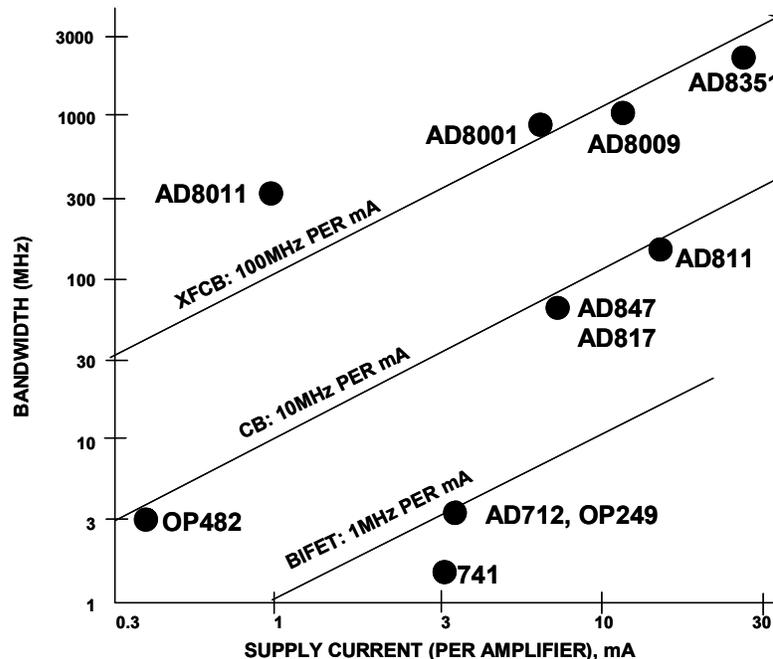
Figure 1-96: *Amplifier bandwidth versus supply current for Analog Devices' processes*

The evolution of high speed processes using amplifier bandwidth as a function of supply current as a figure of merit is shown in Figure 1-96 above. (In the case of duals, triples, and quads, the current per amplifier is used). Analog Devices BiFET process, which produced the AD712 (3MHz bandwidth, 3mA current, yields about 1MHz per mA.

The CB (Complementary Bipolar) process (AD817, AD847, AD811, etc.) yields about 10MHz/mA of supply current. The f_ts of the CB process PNP transistors are about 700MHz, and the NPN's about 900MHz. The CB process at Analog Devices was introduced in 1985.

The next complementary bipolar process from Analog Devices is a high speed dielectrically isolated process called "XFCB" (eXtra Fast Complementary Bipolar) which was introduced in 1992 .This process yields 3GHZ PNPs and 5GHZ matching NPNs, and coupled with innovative circuit topologies allows op amps to achieve new levels of cost-effective performance at astonishing low quiescent currents. The approximate figure of merit for this process is typically 100MHz/mA, although the AD8011 op amp is capable of 300MHz bandwidth on 1mA of supply current due to its unique two-stage current-feedback architecture described later in this section.

Even faster CB processes have been developed at Analog Devices for low voltage supply products such as "XFCB 1.5" (5GHz PNP, 9GHz NPN), and "XFCB 2" (9GHZ PNP, 16GHz NPN). The AD8351 differential low distortion RF amplifier (shown on Fig. 1-96) is fabricated on "XFCB 1.5" and has a bandwidth of 2GHz for a gain of 12dB. It is expected that newer complementary bipolar processes will be optimized for higher f_ts.

In order to select intelligently the correct high speed op amp for a given application, an understanding of the various op amp topologies as well as the tradeoffs between them is required. The two most widely used topologies are voltage feedback (VFB) and current feedback (CFB). An overview of these topologies has been presented in a previous section, but the following discussion treats the frequency-related aspects of the two topologies in considerably more detail.

Voltage Feedback (VFB) Op Amps

A voltage feedback (VFB) op amp is distinguished from a current feedback (CFB) op amp by circuit topology. The VFB op amp is certainly the most popular in low frequency applications, but the CFB op amp has some advantages at high frequencies. We will discuss CFB in detail later, but first the more traditional VFB architecture.

Early IC voltage feedback op amps were made on "all NPN" processes. These processes were optimized for NPN transistors— the "lateral" PNP transistors had relatively poor performance. Some examples of these early VFB op amps which used these poor quality PNPs include the 709, the LM101 and the 741 (see Chapter H: "Op Amp History").

Lateral PNPs were generally only used as current sources, level shifters, or for other non-critical functions. A simplified diagram of a typical VFB op amp manufactured on such a process is shown in Figure 1-97 (opposite).

The input stage is a differential pair (sometimes called a *long-tailed pair*) consisting of either a bipolar pair (Q1, Q2) or a FET pair. This "g_m" (transconductance) stage converts the small-signal differential input voltage, v, into a current, i, and its transfer function is measured in units of conductance, $1/\Omega$, (or mhos). The small-signal emitter resistance, r_e, is approximately equal to the reciprocal of the small-signal g_m.

The formula for the small-signal g_m of a single bipolar transistor is given by the following equation:

$$g_m = \frac{1}{r_e} = \frac{q}{kT}(I_C) = \frac{q}{kT}\left(\frac{I_T}{2}\right), \text{ or} \qquad \text{Eq. 1-32}$$

$$g_m \approx \left(\frac{1}{26mV}\right)\left(\frac{I_T}{2}\right). \qquad \text{Eq. 1-33}$$

where I_T is the differential pair tail current, I_C is the collector quiescent bias current ($I_C = I_T/2$), q is the electron charge, k is Boltzmann's constant, and T is absolute temperature. At +25°C, $V_T = kT/q = 26mV$ (often called the *thermal voltage*, V_T).
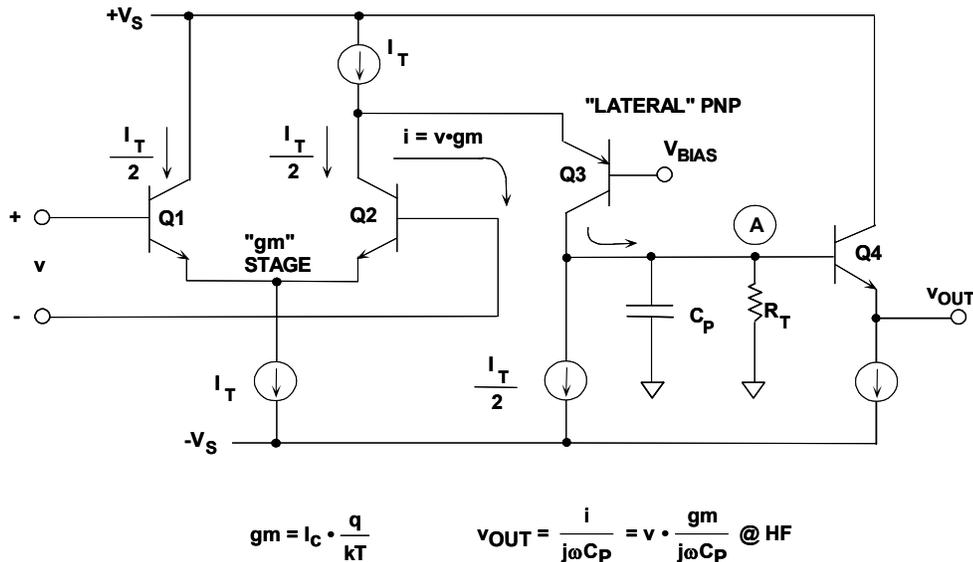
**Figure 1-97:** *Voltage feedback (VFB) op amp designed on an "all NPN" IC process*

As we will see shortly, the amplifier unity gain-bandwidth product, f_u, is equal to $g_m/2\pi C_P$, where the capacitance C_P is used to set the dominant pole frequency. For this reason, the tail current, I_T, is made proportional to absolute temperature (PTAT). This current tracks the variation in r_e with temperature thereby making g_m independent of temperature. It is relatively easy to make C_P reasonably constant over temperature.

The Q2 collector output of the g_m stage drives the emitter of a lateral PNP transistor (Q3). It is important to note that Q3 is not used to amplify the signal, only to level shift, i.e., the signal current variation in the collector of Q2 appears at the collector of Q3. The collector current of Q3 develops a voltage across high impedance node A, and C_P sets the dominant pole of the amplifier. Emitter follower Q4 provides a low impedance output.

The effective load at the high impedance node A can be represented by a resistance, R_T, in parallel with the dominant pole capacitance, C_P. The small-signal output voltage, v_{out}, is equal to the small-signal current, i, multiplied by the impedance of the parallel combination of R_T and C_P.

Figure 1-98 below shows a simple model for the single-stage amplifier and the corresponding Bode plot. The Bode plot is conveniently constructed on a log-log scale.
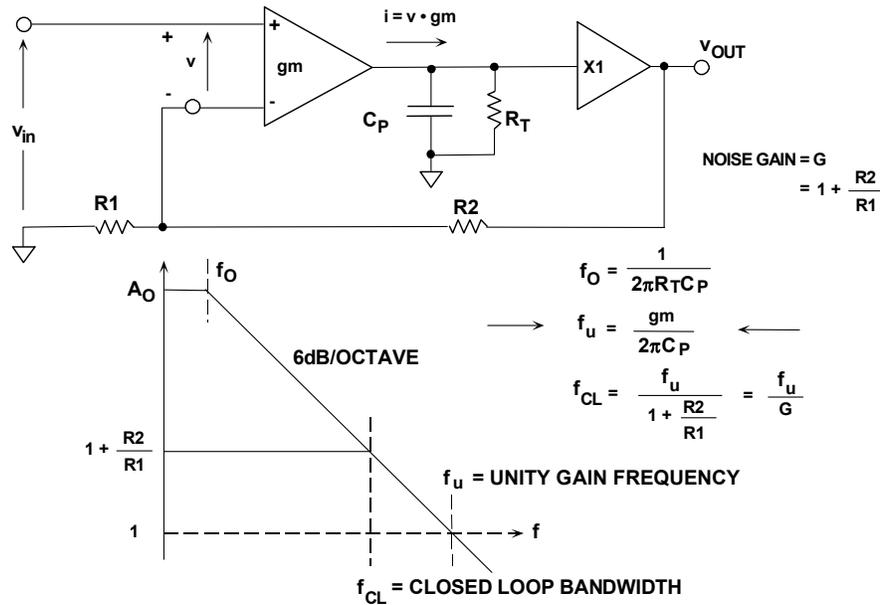
Figure 1-98: Model and Bode plot for a VFB op amp

The low frequency breakpoint, f_O, is given by:

$$f_o = \frac{1}{2\pi R_T C_P} \, .$$

Eq. 1-34

Note that the high frequency response is determined solely by g_m and C_P:

$$v_{out} = v \cdot \frac{g_m}{j\omega C_P} \, .$$

Eq. 1-35

The unity gain-bandwidth frequency, f_u, occurs where $|v_{out}| = |v|$. Letting $\omega = 2\pi f_u$ and $|v_{out}| = |v|$, Eq. 1-35 can be solved for f_u,

$$f_u = \frac{g_m}{2\pi C_P} \, .$$

Eq. 1-36

We can use feedback theory to derive the closed-loop relationship between the circuit's signal input voltage, v_{in}, and its output voltage, v_{out}:

$$\frac{v_{out}}{v_{in}} = \frac{1 + \dfrac{R2}{R1}}{1 + \dfrac{j\omega C_P}{g_m}\left(1 + \dfrac{R2}{R1}\right)} \, .$$

Eq. 1-37

At the op amp 3dB closed-loop bandwidth frequency, f_{cl}, the following is true:

$$\frac{2\pi f_{cl} C_P}{g_m}\left(1 + \frac{R2}{R1}\right) = 1 \text{ , and hence}$$

Eq. 1-38

$$f_{cl} = \frac{g_m}{2\pi C_P}\left(\frac{1}{1 + \dfrac{R2}{R1}}\right), \text{ or}$$

Eq. 1-39

$$f_{cl} = \frac{f_u}{1 + \dfrac{R2}{R1}}.$$

Eq. 1-40

This demonstrates the fundamental property of VFB op amps: *The closed-loop bandwidth multiplied by the closed-loop gain is a constant*, i.e., the VFB op amp exhibits a constant gain-bandwidth product over most of the usable frequency range.

As noted previously, some VFB op amps (called *de-compensated*) are not stable at unity gain, but designed to be operated at some minimum (higher) amount of closed-loop gain. However, even for these op amps, the gain-bandwidth product is still relatively constant over the region of stability.

Now, consider the following typical example: $I_T = 100\mu A$, $C_P = 2pF$. We find that:

$$g_m = \frac{I_T/2}{V_T} = \frac{50\mu A}{26mV} = \frac{1}{520\Omega}$$

Eq. 1-41

$$f_u = \frac{g_m}{2\pi C_P} = \frac{1}{2\pi(520)(2\cdot 10^{-12})} = 153MHz.$$

Eq. 1-42

Now, we must consider the large-signal response of the circuit. The slew-rate, SR, is simply the total available charging current, $I_T/2$, divided by the dominant pole capacitance, C_P. For the example under consideration,

$$I = C\frac{dv}{dt}, \ \frac{dv}{dt} = SR, \ SR = \frac{I}{C}$$

Eqs. 1-43

$$SR = \frac{I_T/2}{C_P} = \frac{50\mu A}{2pF} = 25V/\mu s.$$

Eq. 1-44

The full-power bandwidth (FPBW) of the op amp can now be calculated from the formula:

$$FPBW = \frac{SR}{2\pi A} = \frac{25V/\mu s}{2\pi \cdot 1V} = 4MHz,$$

Eq. 1-45

where A is the peak amplitude of the output signal. If we assume a 2V peak-to-peak output sinewave (certainly a reasonable assumption for high speed applications), then we obtain a FPBW of only 4MHz, even though the small-signal unity gain-bandwidth product is 153MHz! For a 2V p-p output sinewave, distortion will begin to occur much lower than the actual FPBW frequency. We must increase the SR by a factor of about 40 in order for the FPBW to equal 153MHz. The only way to do this is to increase the tail current, I_T, of the input differential pair by the same factor. This implies a bias current of 4mA in order to achieve a FPBW of 160MHz. We are assuming that C_P is a fixed value of 2pF and cannot be lowered by design. These calculations are summarized below in Figure 1-99.

◆ Assume that I_T = 100µA, Cp = 2pF

$$g_m = \frac{I_C}{V_T} = \frac{50\mu A}{26mV} = \frac{1}{520\Omega}$$

$$f_u = \frac{g_m}{2\pi\ Cp} = 153MHz$$

◆ Slew Rate = SR =

BUT FOR 2V PEAK-PEAK OUTPUT (A = 1V)

$$FPBW = \frac{SR}{2\pi\ A} = 4MHz$$

◆ Must increase I_T to 4mA to get FPBW = 160MHz!!

◆ Reduce g_m by adding emitter degeneration resistors

Figure 1-99: VFB op amp bandwidth and slew rate calculations

In practice, the FPBW of the op amp should be approximately 5 to 10 times the maximum output frequency in order to achieve acceptable distortion performance (typically 55-80dBc @ 5 to 20MHz, but actual system requirements vary widely).

Notice, however, that increasing the tail current causes a proportional increase in g_m and hence f_u. In order to prevent possible instability due to the large increase in f_u, g_m can be reduced by inserting resistors in series with the emitters of Q1 and Q2 (this technique, called *emitter degeneration*, also serves to linearize the g_m transfer function and thus also lowers distortion).

This analysis points out that a major inefficiency of conventional bipolar voltage feedback op amps is their inability to achieve high slew rates without proportional increases in quiescent current (assuming that C_P is fixed, and has a reasonable minimum value of 2 or 3pF).

This of course is not meant to say that high speed op amps designed using this architecture are deficient, just that there are circuit design techniques available which allow equivalent performance at much lower quiescent currents. This is extremely important in portable battery operated equipment where every milliwatt of power dissipation is critical.
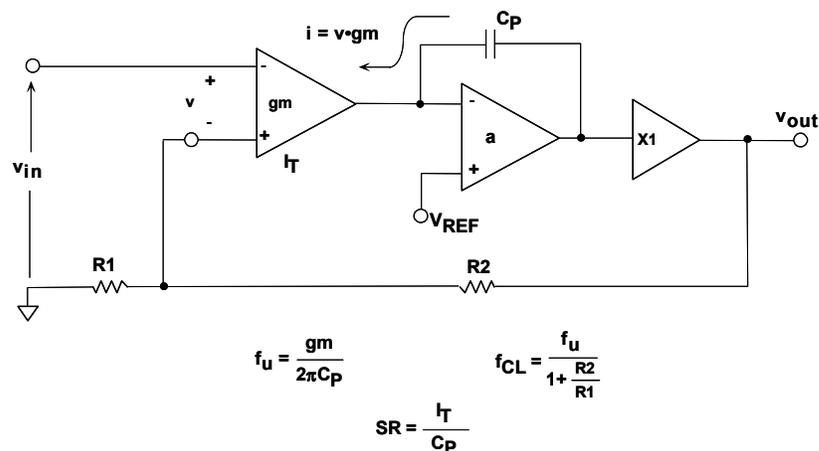
VFB Op Amps Designed on Complementary Bipolar Processes

With the advent of complementary bipolar (CB) processes having high quality PNP transistors as well as NPNs, VFB op amp configurations such as the one shown in the simplified diagram in Figure 1-100 below became popular.
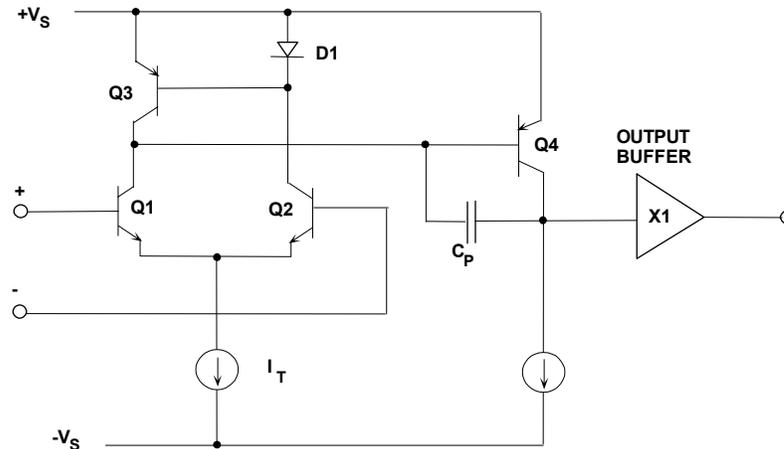
Figure 1-100: VFB op amp using two gain stages

Notice that the input differential pair (Q1, Q2) is loaded by a current mirror (Q3 and D1). We show D1 as a diode for simplicity, but it is actually a diode-connected PNP transistor (matched to Q3) with the base and collector connected to each other. This simplification will be used in many of the circuit diagrams to follow in this section. The common emitter transistor, Q4, provides a *second* voltage gain stage.

$$f_u = \frac{gm}{2\pi C_P} \qquad f_{CL} = \frac{f_u}{1 + \frac{R2}{R1}}$$

$$SR = \frac{I_T}{C_P}$$

Figure 1-101: Model for two stage VFB op amp

Since the PNP transistors are fabricated on a complementary bipolar process, they are high quality and matched to the NPNs, and therefore suitable for voltage gain. The dominant pole of the Fig. 1-100 amplifier is set by C_P, and the combination of the gain stage, Q4 and local feedback capacitor C_P is often referred to as a *Miller Integrator*. The unity-gain output buffer is usually a complementary emitter follower.

A model for this two-stage VFB op amp is shown in Figure 1-101 above. Notice that the unity gain-bandwidth frequency, f_u, is still determined by the input stage g_m and the

dominant pole capacitance, C_P. The second gain stage increases the DC open-loop gain, but maximum slew rate is still limited by the input stage tail current as: $SR = I_T/C_P$.

A two-stage amplifier topology such as this is widely used throughout the IC industry in VFB op amps, both precision and high speed. It can be recalled that a similar topology with a dual FET input stage was used in the early high speed, fast settling FET modular op amps (see Chapter H: "Op Amp History").

Another popular VFB op amp architecture is the *folded cascode* as shown in Figure 1-102 below. An industry-standard video amplifier family (the AD847) is based on this architecture. This circuit also takes advantage of the fast PNPs available on a CB process. The differential signal currents in the collectors of Q1 and Q2 are fed to the emitters of a PNP cascode transistor pair (hence the term *folded cascode*). The collectors of Q3 and Q4 are loaded with the current mirror, D1 and Q5, and voltage gain is developed at the Q4-Q5 node. This single-stage architecture uses the junction capacitance at the high-impedance node for compensation (C_{STRAY}). Some variations of the design bring this node to an external pin so that additional external capacitance can be added if desired.
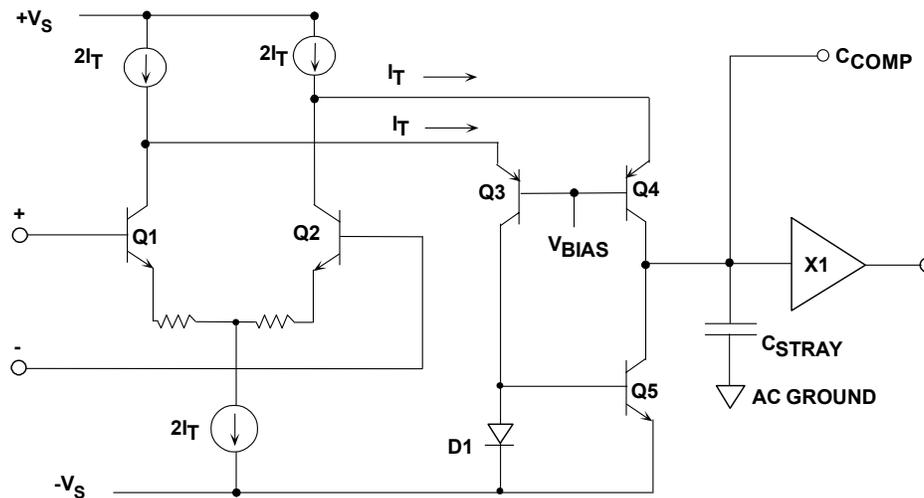

Figure 1-102: *AD847-family folded cascode simplified circuit*

With no emitter degeneration resistors in Q1 and Q2, and no additional external compensating capacitance, this circuit is only stable for high closed-loop gains. However, unity-gain compensated versions of this family are available which have the appropriate amount of emitter degeneration.

The availability of JFETs on a CB process allows not only low input bias current but also improvements in the slew rate tradeoff, which must be made between g_m and I_T found in bipolar input stages. Figure 1-103 (opposite) shows a simplified diagram of the AD845 16MHz op amp. JFETs have a much lower g_m per mA of tail current than a bipolar transistor. This lower g_m of the FET allows the input tail current (hence the slew rate) to be increased, without having to increase C_P to maintain stability.

The unusual thing about this seemingly poor performance of the JFET is that it is exactly what is needed for a fast, high SR input stage. For a typical JFET, the value of g_m is approximately $I_s/1V$ (I_s is the source current), rather than $I_c/26mV$ for a bipolar transistor,

i.e., the FET g_m is about 40 times lower. This allows much higher tail currents (and higher slew rates) for a given g_m when JFETs are used as the input stage.
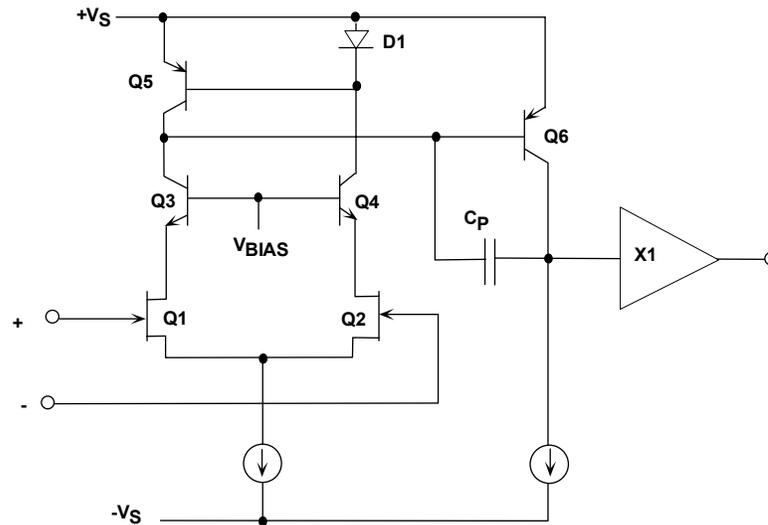
Figure 1-103: *AD845 BiFET 16MHz op amp simplified circuit*

A New VFB Op Amp Architecture for "Current-on-Demand" Performance, Lower Power, and Improved Slew Rate

Until recently, op amp designers had to make the above tradeoffs between the input g_m stage quiescent current and the slew-rate and distortion performance. ADI has patented a circuit core which supplies *current-on-demand,* to charge and discharge the dominant pole capacitor, C_P, while allowing the quiescent current to be small. The additional current is proportional to the fast slewing input signal and adds to the quiescent current.
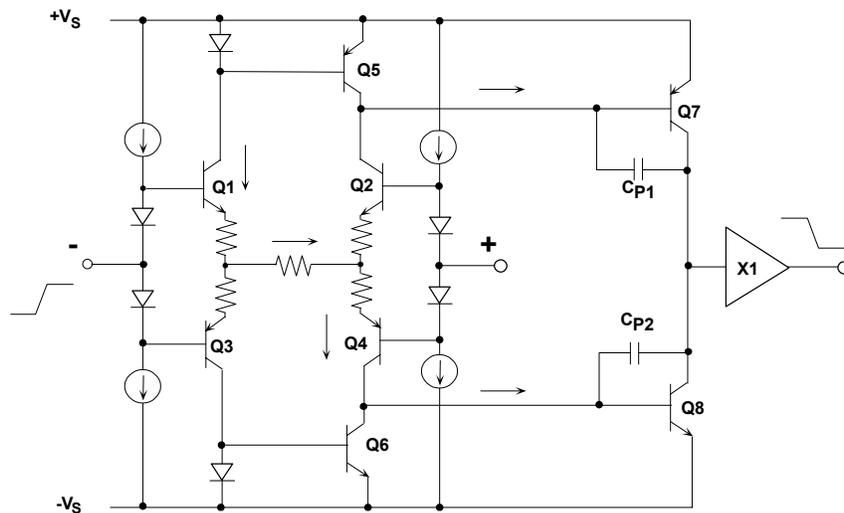
Figure 1-104: *"Quad-Core" VFB g_m stage for current-on-demand*

A simplified diagram of the basic core cell is shown in Figure 1-104 above. The *quad-core* (g_m stage) consists of transistors Q1, Q2, Q3, and Q4 with their emitters connected together as shown. Consider a positive step voltage on the inverting input. This voltage produces a proportional current in Q1 that is mirrored into C_{P1} by Q5. The current through Q1 also flows through Q4 and C_{P2}.

1.111

At the dynamic range limit, Q2 and Q3 are correspondingly turned off. Notice that the charging and discharging current for C_{P1} and C_{P2} is not limited by the quad core bias current. In practice, however, small current-limiting resistors are required forming an "H" resistor network as shown. Q7 and Q8 form the second gain stage (driven differentially from the collectors of Q5 and Q6), and the output is buffered by a unity-gain complementary emitter follower (X1).

The quad core configuration is patented (see Reference 1), as well as the circuits that establish the quiescent bias currents (not shown in Fig. 1-104). A number of new VFB op amps using this proprietary configuration have been released and have unsurpassed high frequency low distortion performance, bandwidth, and slew rate at the indicated quiescent current levels as shown in Figure 1-105 below.

LISTED IN ORDER OF DECREASING SUPPLY CURRENT

PART #	I_{SY} / AMP	BANDWIDTH	SLEWRATE	DISTORTION
AD9631/32 (1)	17mA	320MHz	1300V/μs	–72dBc@20MHz
AD8074/75 (3)	8mA	600MHz	1600V/μs	–62dBc@20MHz
AD8047/48 (1)	5.8mA	250MHz	750V/μs	–66dBc@5MHz
AD8041 (1)	5.2mA	160MHz	160V/μs	–69dBc@10MHz
AD8042 (2)	5.2mA	160MHz	200V/μs	–64dBc@10MHz
AD8044 (3)	2.8mA	150MHz	150V/μs	–75dBc@5MHz
AD8039 (2)	1.5mA	300MHz	425V/μs	–65dBc@5MHz
AD8031 (1)	0.75mA	80MHz	30V/μs	–62dBc@1MHz
AD8032 (2)	0.75mA	80MHz	30V/μs	–72dBc@1MHz

Number in ( ) indicates single, dual, triple, or quad

Figure 1-105: High speed VFB op amps

The AD9631, AD8074, and AD8047 are optimized for a gain of +1, while the AD9632, AD8075, and AD8048 for a gain of +2.

The same quad-core architecture is used as the *second* stage of the AD8041 rail-to-rail output, zero-volt input single-supply op amp. The input stage is a differential PNP pair which allows the input common-mode signal to go about 200mV below the negative supply rail. The AD8042 and AD8044 are dual and quad versions of the AD8041.

Current Feedback (CFB) Op Amps

We will now examine in more detail the current feedback (CFB) op amp topology which is very popular in high speed op amps. As mentioned previously, the circuit concepts were introduced decades ago, however modern high speed complementary bipolar processes are required to take full advantage of the architecture.

It has long been known that in bipolar transistor circuits, currents can be switched faster than voltages, other things being equal. This forms the basis of non-saturating emitter-coupled logic (ECL) and devices such as current-output DACs. Maintaining low impedances at the current switching nodes helps to minimize the effects of stray capacitance, one of the largest detriments to high speed operation. The current mirror is a good example of how currents can be switched with a minimum amount of delay.
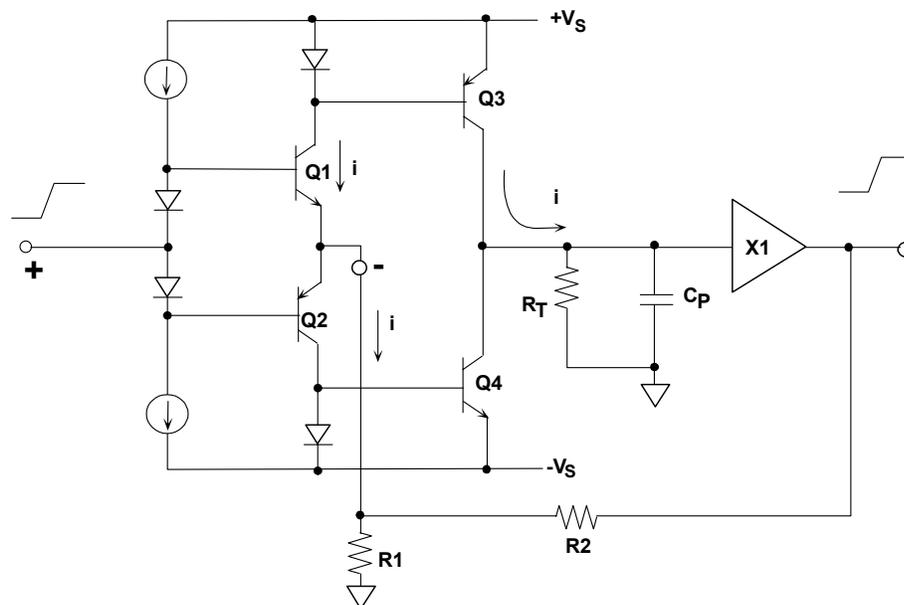
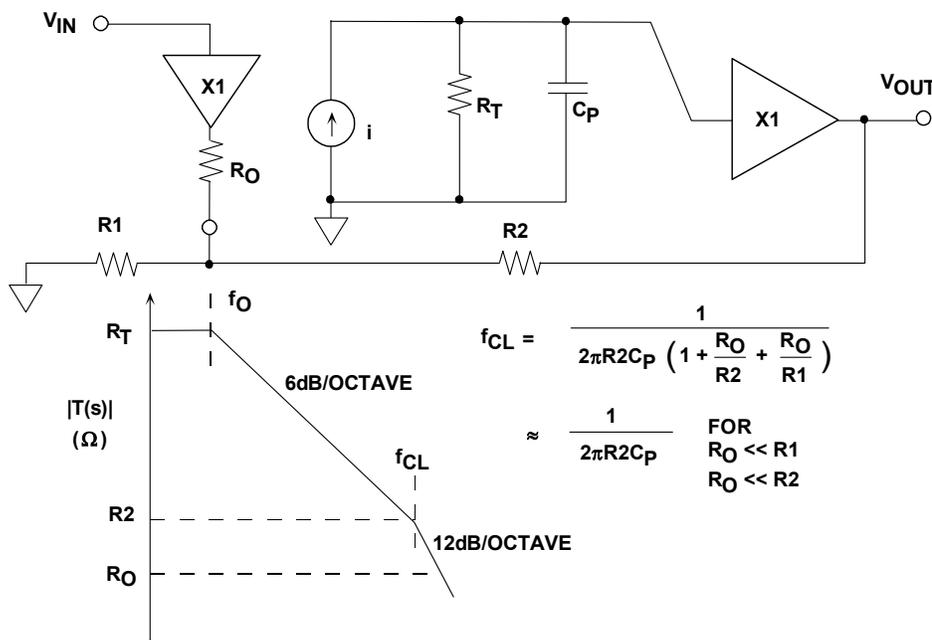*Figure 1-106:* Simplified current feedback (CFB) op amp

The current feedback op amp topology is simply an application of these fundamental principles of current steering. A simplified CFB op amp is shown in Figure 1-106 above. The non-inverting input is high impedance and is buffered directly to the inverting input through the complementary emitter follower buffers Q1 and Q2. Note that the inverting input impedance is very low (typically 10 to 100Ω), because of the low emitter resistance (ideally, would be zero). This is a fundamental difference between a CFB and a VFB op amp, and also a feature that gives the CFB op amp some unique advantages.

The collector outputs of Q1 and Q2 drive current mirrors, which mirror the inverting input current to the high impedance node, modeled by R_T and C_P. The high impedance node is buffered by a complementary unity gain emitter follower. Feedback from the output to the inverting input acts to force the inverting input *current* to zero, hence the term *Current Feedback*. Note that in a ideal case, for zero inverting input impedance, no small signal voltage can exist at this node, only small-signal current.

Now, consider a positive step voltage applied to the non-inverting input of the CFB op amp. Q1 immediately sources a proportional current into the external feedback resistors creating an *error* current, which is mirrored to the high impedance node by Q3. The voltage developed at the high impedance node is equal to this current multiplied by the equivalent impedance. This is where the term *transimpedance op amp* originated, since the transfer function is an impedance, rather than a unitless voltage ratio as in a traditional VFB op amp.

Note also that the error current delivered to the high impedance node is not limited by the input stage tail current. In other words, unlike a conventional VFB op amp, *there is no slew-rate limitation in an ideal CFB op amp*. The current mirrors supply *current-on-demand* from the power supplies. The negative feedback loop then forces the output voltage to a value that reduces the inverting input error current to zero.

$$f_{CL} = \frac{1}{2\pi R2 C_P \left(1 + \dfrac{R_O}{R2} + \dfrac{R_O}{R1}\right)}$$

$$\approx \frac{1}{2\pi R2 C_P} \quad \begin{array}{l} \text{FOR} \\ R_O \ll R1 \\ R_O \ll R2 \end{array}$$

Figure 1-107: CFB op amp model and Bode plot

The model for a CFB op amp is shown in Figure 1-107 above, along with the corresponding Bode plot. The Bode plot is plotted on a log-log scale, and the open-loop gain is expressed as a transimpedance, T(s), with units of ohms.

The finite output impedance of the input buffer is modeled by R_O. The input error current is *i*. By applying the principles of negative feedback, we can derive the expression for the op amp transfer function:

$$\frac{v_{out}}{v_{in}} = \frac{1 + \dfrac{R2}{R1}}{1 + j\omega C_P R2 \left(1 + \dfrac{Ro}{R2} + \dfrac{Ro}{R1}\right)}. \qquad \text{Eq. 1-46}$$

At the op amp 3dB closed-loop bandwidth frequency, f_{cl}, the following is true:

$$2\pi f_{cl} C_P R2 \left(1 + \frac{Ro}{R2} + \frac{Ro}{R1} \right) = 1 .$$

<div align="right">Eq. 1-47</div>

Solving for f_{cl}:

$$f_{cl} = \frac{1}{2\pi C_P R2 \left(1 + \dfrac{Ro}{R2} + \dfrac{Ro}{R1} \right)} .$$

<div align="right">Eq. 1-48</div>

For the condition $R_O \ll R2$ and R1, the equation simply reduces to:

$$f_{cl} = \frac{1}{2\pi C_P R2} .$$

<div align="right">Eq. 1-49</div>

Examination of this equation quickly reveals that *the closed-loop bandwidth of a CFB op amp is determined by the internal dominant pole capacitor, C_P, and the external feedback resistor R2, and is independent of the gain-setting resistor, R1*. This ability to maintain constant bandwidth independent of gain makes CFB op amps ideally suited for wideband programmable gain amplifiers.
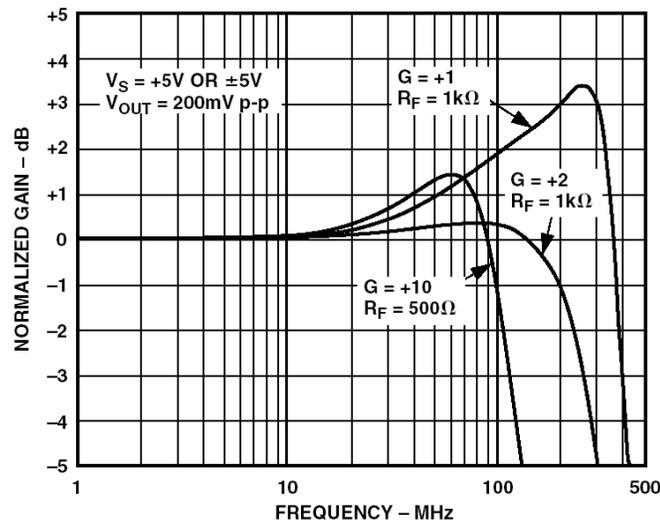
Figure 1-108: *AD8011 frequency response, G = +1, +2, +10*

Because the closed-loop bandwidth is inversely proportional to the external feedback resistor, R2, a CFB op amp is usually optimized for a specific R2. Increasing R2 from its optimum value lowers the bandwidth, and decreasing it may lead to oscillation and instability because of high frequency parasitic poles.

The frequency response of the AD8011 CFB op amp is shown in Figure 1-108 above for various closed-loop values of gain (+1, +2, and +10). Note that even at a gain of +10, the closed-loop bandwidth is still greater than 100MHz. The peaking which occurs at a gain of +1 is typical of wideband CFB op amps used in the non-inverting mode, and is due primarily to stray capacitance at the inverting input. This peaking can be reduced by sacrificing bandwidth, by using a slightly larger feedback resistor.

<div align="right">**1.115**</div>

The AD8011 CFB op amp (introduced in 1995) still represents state-of-the-art performance, and key specifications are shown in Figure 1-109 below.

- ◆ **1mA Power Supply Current (+5V or ±5V)**
- ◆ **300MHz Bandwidth (G = +1)**
- ◆ **2000 V/µs Slew Rate**
- ◆ **29ns Settling Time to 0.1%**
- ◆ **Video Specifications (G = +2)**
    - **Differential Gain Error 0.02%**
    - **Differential Phase Error 0.06°**
    - **25MHz 0.1dB Bandwidth**
- ◆ **Distortion**
    - **–70dBc @ 5MHz**
    - **–62dBc @ 20MHz**
- ◆ **Fully Specified for ±5V or +5V Operation**

Figure 1-109: AD8011 key specifications

Traditional current feedback op amps have been limited to a single gain stage, using current-mirrors. The AD8011 (and also others in this family) unlike traditional CFB op amps, use a *two-stage gain configuration*, as shown in Figure 1-110 below.
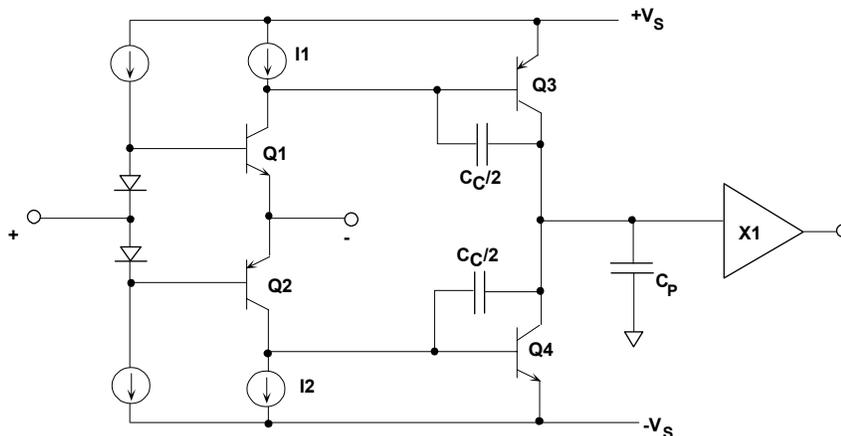
Figure 1-110: Simplified two-stage current feedback op amp

Until the advent of the AD8011, fully complementary two-gain stage CFB op amps had been impractical because of their high power dissipation. The AD8011 employs a patented (see Reference 2) second gain stage consisting of a pair of complementary amplifiers (Q3 and Q4). Note that they are not connected as current mirrors but as grounded-emitter gain stages. The detailed design of current sources (I1 and I2), and their respective bias circuits are the key to the success of the two-stage CFB circuit; they keep the amplifier's quiescent power low, yet are capable of supplying *current-on-demand* for wide current excursions required during fast slewing.

A further advantage of the two-stage amplifier is the higher overall bandwidth (for the same power), which means lower signal distortion and the ability to drive heavier external loads.

Thus far, we have learned several key features of CFB op amps. The most important is that for a given complementary bipolar IC process, *CFB generally yields higher FPBW (hence lower distortion) than VFB for the same amount of quiescent supply current.* This is because there is practically no slew-rate limiting in CFB. Because of this, the full power bandwidth and the small signal bandwidth are approximately the same.

LISTED IN ORDER OF DECREASING SUPPLY CURRENT

PART #	I_{SY} / AMP	BANDWIDTH	SLEWRATE	DISTORTION
AD8009 (1)	14mA	1000MHz	5500V/µs	−80dBc@5MHz
AD8023 (3)	10mA	250MHz	1200V/µs	ΔG=0.06%, Δφ=0.02°
AD8001 (1)	5.0mA	600MHz	1200V/µs	−65dBc@5MHz
AD8002 (2)	5.0mA	600MHz	1200V/µs	−65dBc@5MHz
AD8004 (4)	3.5mA	250MHz	3000V/µs	−78dBc@5MHz
AD8013 (3)	4.0mA	140MHz	1000V/µs	ΔG=0.02%, Δφ=0.06°
AD8072 (2)	3.5mA	100MHz	500V/µs	ΔG=0.05%, Δφ=0.1°
AD8073 (3)	3.5mA	100MHz	500V/µs	ΔG=0.05%, Δφ=0.1°
AD8012 (2)	1.7mA	350MHz	2250V/µs	−66dBc@5MHz
AD8014 (1)	1.2mA	400MHz	4000V/µs	−70dBc@5MHz
AD8011 (1)	1.0mA	300MHz	5500V/µs	−70dBc@5MHz
AD8005 (1)	0.4mA	270MHz	1500/µs	−53dBc@5MHz

Number in ( ) Indicates Single, Dual, Triple, or Quad

Figure 1-111: *Performance of selected CFB op amps*

The second important feature is that the *inverting input impedance of a CFB op amp is very low.* This is advantageous when using the op amp in the inverting mode as an I/V converter, because there is less sensitivity to inverting input capacitance than with VFB.

The third feature is that *the closed-loop bandwidth of a CFB op amp is determined by the value of the internal Cp capacitor and the external feedback resistor R2 and is relatively independent of the gain-setting resistor R1.*

The performance for a selected group of current feedback op amps is shown in Figure 1-111 above. Note that the op amps are listed in order of decreasing power supply current.

◆ **CFB yields higher FPBW and lower distortion than VFB for the same process and power dissipation**

◆ **Inverting input impedance of a CFB op amp is low, non-inverting input impedance is high**

◆ **Closed-loop bandwidth of a CFB op amp is determined by the internal dominant-pole capacitance and the external feedback resistor, independent of the gain-setting resistor**

Figure 1-112: *Summary: CFB op amps*

Figure 1-112 above summarizes the general characteristics of CFB op amps.

Effects of Feedback Capacitance in Op Amps

It is quite common to use a capacitor in the feedback loop of a VFB op amp, to shape the frequency response as in a simple single-pole lowpass filter shown in Figure 1-113A below. The resulting noise gain is plotted on a Bode plot to analyze stability and phase margin. Stability of the system is determined by the net slope of the noise gain and the open-loop gain where they intersect.
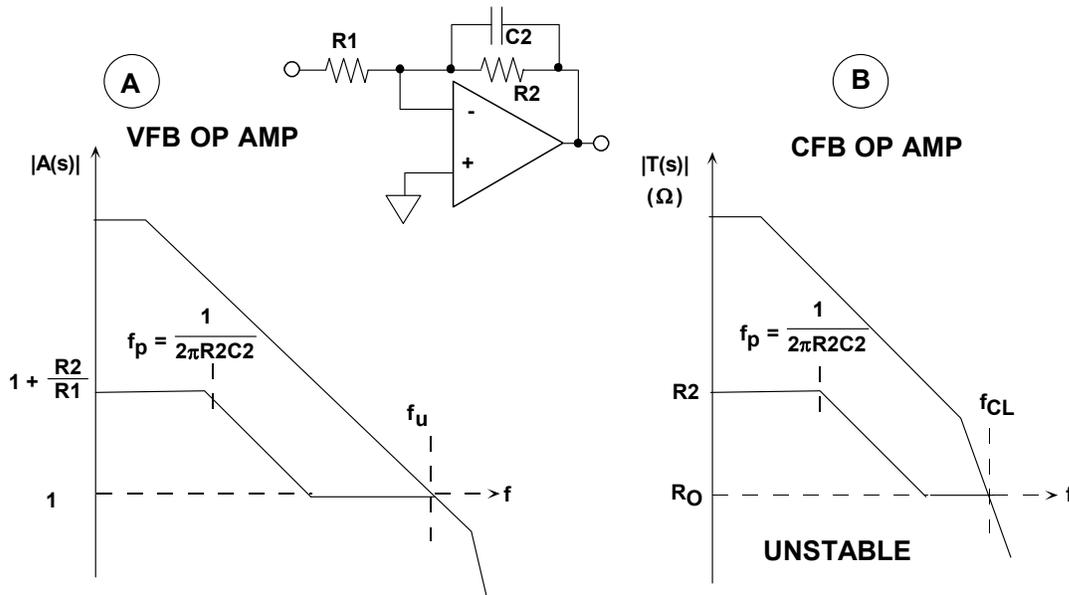
Figure 1-113: *Noise gain stability analysis for VFB and CFB op amps with feedback capacitor*

For unconditional stability, the noise gain plot must intersect the open-loop response with a net slope of less than 12dB/octave. In this case, the net slope where they intersect is 6dB/octave, indicating a stable condition. Notice for the case drawn in Fig. 1-113A, the second pole in the frequency response occurs at a considerably higher frequency than f_u.

In the case of the CFB op amp (Fig. 1-113B), the same analysis is used, except that the open-loop transimpedance gain, T(s), is used to construct the Bode plot.

The definition of *noise gain* (for the purposes of stability analysis) for a CFB op amp, however, must be redefined in terms of a *current* noise source attached to the inverting input as shown in Figure 1-114 on the following page. This current is reflected to the output by an impedance, which we define to be the "current noise gain" of a CFB op amp:

$$\text{"CURRENT NOISE GAIN"} \equiv R_O + Z2\left(1 + \frac{R_O}{Z1}\right). \qquad \text{Eq. 1-50}$$

Now, return to Fig. 1-113B, and observe the CFB *current noise gain* plot. At low frequencies, the CFB current noise gain is simply R2 (making the assumption that Ro is much less than Z1 or Z2. The first pole is determined by R2 and C2. As the frequency continues to increase, C2 becomes a short circuit, and all the inverting input current flows through R_O (again refer to Fig. 1-114).

$$\text{CURRENT "NOISE GAIN"} = \frac{V_{OUT}}{i}$$

$$= R_O + Z2\left(1 + \frac{R_O}{Z1}\right)$$
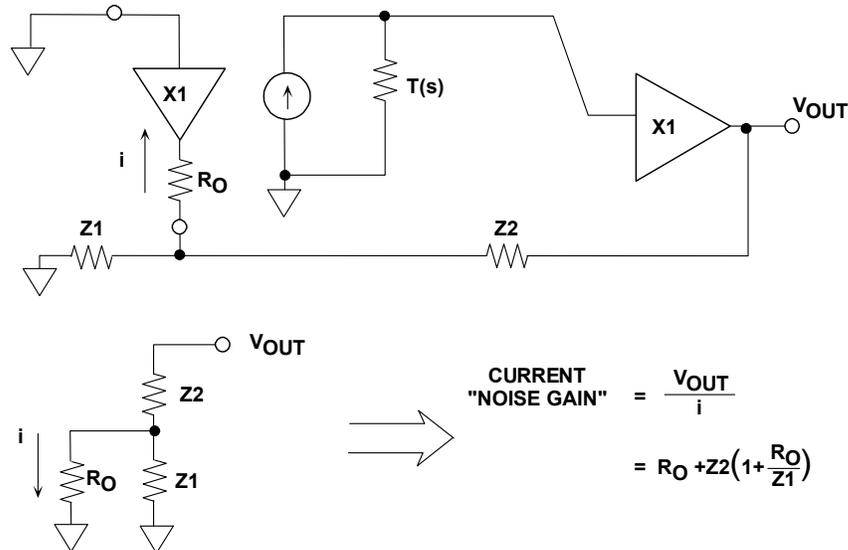
Figure 1-114: Current "noise gain" definition for CFB op amp for use in stability analysis

A CFB op amp is normally optimized for best performance for a fixed feedback resistor, R2. Additional poles in the transimpedance gain, T(s), occur at frequencies above the closed-loop bandwidth, f_{cl}, (set by R2). Note that the intersection of the CFB current noise gain with the open-loop T(s) occurs where the slope of the T(s) function is 12dB/octave. This indicates instability and possible oscillation.

It is for this reason that *CFB op amps are not suitable in configurations which require capacitance in the feedback loop*, such as simple active integrators or lowpass filters.


R2 FIXED FOR CFB OP AMP
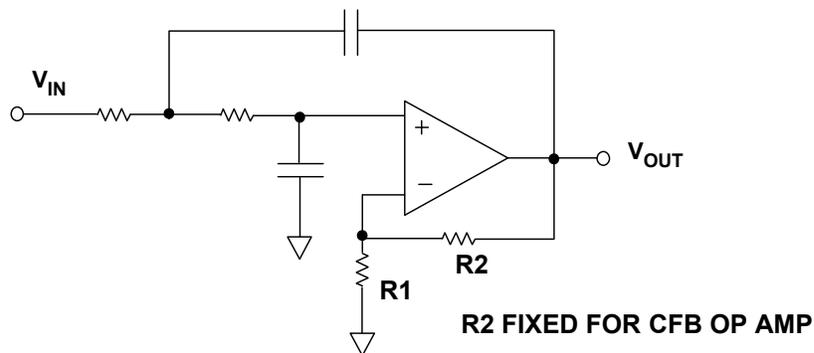
Figure 1-115: The Sallen-Key filter configuration

They can, however, be used in certain active filters such as the Sallen-Key configuration shown in Figure 1-115 above, which do not require capacitance in the feedback network.

On the other hand, VFB op amps, do make very flexible active filters. A multiple feedback 20MHz lowpass filter example using an AD8048 op amp is shown below in Figure 1-116.

In general, an active filter amplifier should have a bandwidth that is at least ten times the bandwidth of the filter, if problems due to phase shift of the amplifier are to be avoided. (The AD8048 has a bandwidth of over 200MHz in this configuration).
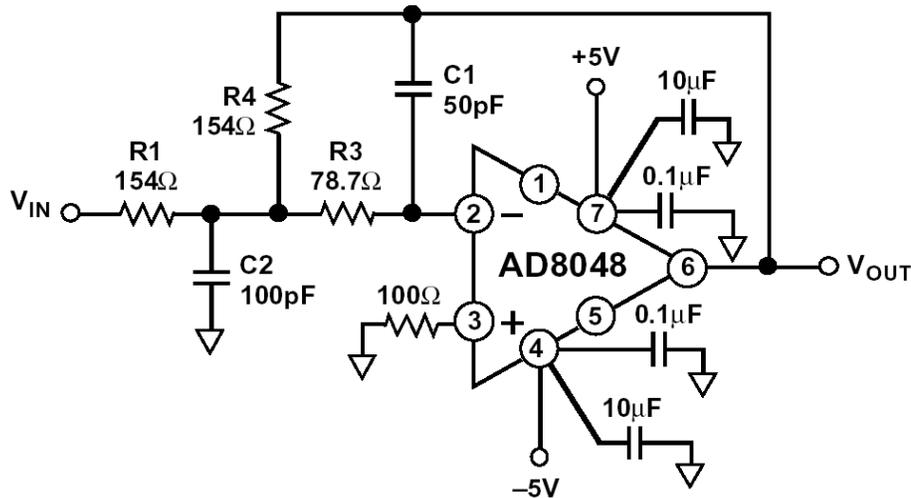
Figure 1-116: *Multiple feedback 20MHz lowpass filter using the AD8048 VFB op amp*

Design details of the filter design can be found on the AD8048 data sheet. Further discussions on active filter design are included in Chapter 5 of this book.

High Speed Current-to-Voltage Converters, and the Effects of Inverting Input Capacitance

Fast op amps are useful as current-to-voltage converters in such applications as high speed photodiode preamplifiers and current-output DAC buffers. A typical application using a VFB op amp as an I/V converter is shown in Figure 1-117 on the following page.
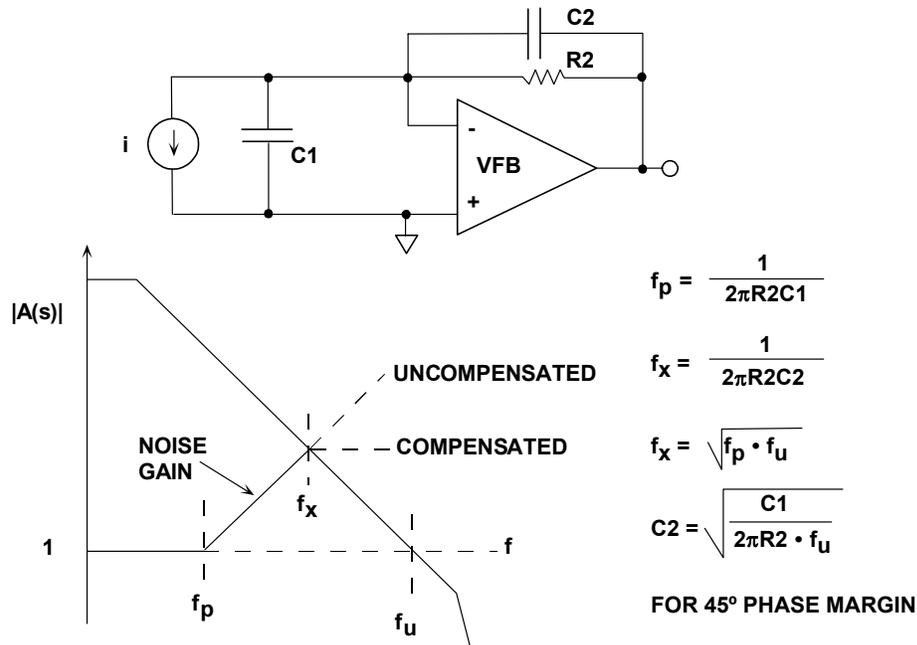
The net input capacitance, C1, forms a pole at a frequency f_P in the noise gain transfer function as shown in the Bode plot, and is given by:

$$f_P = \frac{1}{2\pi R2C1}.$$

Eq. 1-51

If left uncompensated, the phase shift at the frequency of intersection, f_x, will cause instability and oscillation. Introducing a zero at f_x by adding feedback capacitor C2 stabilizes the circuit and yields a phase margin of about 45°.

The location of the zero is given by:

$$f_X = \frac{1}{2\pi R2 C2} .$$

$$f_p = \frac{1}{2\pi R2 C1}$$

$$f_x = \frac{1}{2\pi R2 C2}$$

$$f_x = \sqrt{f_p \cdot f_u}$$

$$C2 = \sqrt{\frac{C1}{2\pi R2 \cdot f_u}}$$

FOR 45° PHASE MARGIN

Figure 1-117: Compensating for input capacitance in a current-to-voltage converter using VFB op amp

Although the addition of C2 actually decreases the pole frequency slightly, this effect is negligible if C2 << C1. The frequency f_x is the geometric mean of f_p and the unity-gain bandwidth frequency of the op amp, f_u,

$$f_X = \sqrt{f_P \cdot f_u} .$$

Combining Eq. 1-52 and Eq. 1-53 and solving for C2 yields:

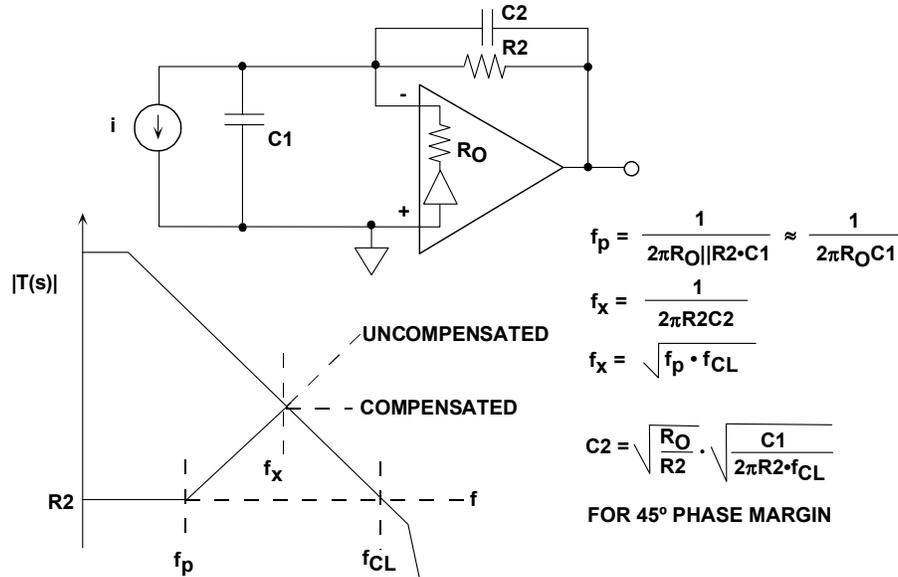$$C2 = \sqrt{\frac{C1}{2\pi R2 \cdot f_u}} .$$

This value of C2 will yield a phase margin of about 45°. Increasing the capacitor by a factor of 2 increases the phase margin to about 65° (see Reference 3).

In practice, the optimum value of C2 may be optimized experimentally by varying it slightly, to optimize the output pulse response.

A similar analysis can be applied to a CFB op amp as shown in Figure 1-118 below. In this case, however, the low inverting input impedance, R_O, greatly reduces the sensitivity to input capacitance. In fact, an ideal CFB with zero input impedance would be totally insensitive to any amount of input capacitance!

$$f_p = \frac{1}{2\pi R_O || R2 \cdot C1} \approx \frac{1}{2\pi R_O C1}$$

$$f_x = \frac{1}{2\pi R2 C2}$$

$$f_x = \sqrt{f_p \cdot f_{CL}}$$

$$C2 = \sqrt{\frac{R_O}{R2}} \cdot \sqrt{\frac{C1}{2\pi R2 \cdot f_{CL}}}$$

FOR 45° PHASE MARGIN

Figure 1-118: *Current-to-voltage converter using a CFB op amp*

The pole caused by C1 occurs at a frequency f_P:

$$f_P = \frac{1}{2\pi (R_O || R2)C1} \approx \frac{1}{2\pi R_O C1} . \qquad \text{Eq. 1-55}$$

This pole frequency will generally be much higher than the case for a VFB op amp, and the pole can be ignored completely if it occurs at a frequency greater than the closed-loop bandwidth of the op amp.

We next introduce a compensating zero at the frequency f_x by inserting the capacitor C2:

$$f_x = \frac{1}{2\pi R2 C2} . \qquad \text{Eq. 1-56}$$

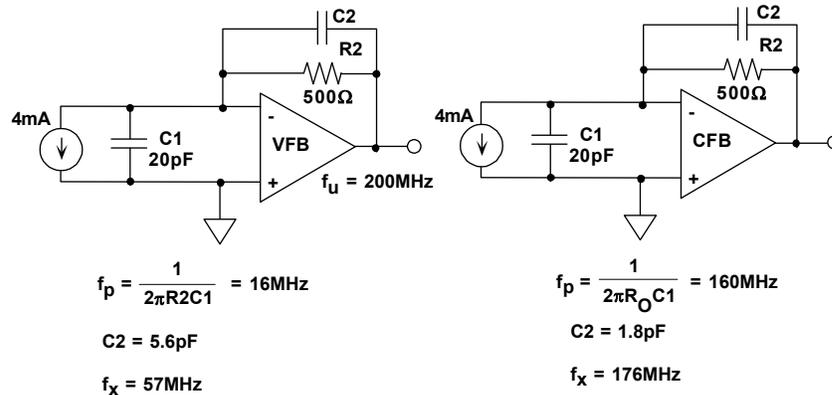As in the case for VFB, f_x is the geometric mean of f_p and f_{cl}:

$$f_x = \sqrt{f_P \cdot f_u} . \qquad \text{Eq. 1-57}$$

Combining Eq. 1-56 and Eq. 1-57 and solving for C2 yields:

$$C2 = \sqrt{\frac{R_O}{R2}} \cdot \sqrt{\frac{C1}{2\pi R2 \cdot f_{cl}}} . \qquad \text{Eq. 1-58}$$

There is a significant advantage in using a CFB op amp in this configuration as can be seen by comparing Eq. 1-58 with the similar equation for C2 required for a VFB op amp, Eq. 1-54. If the unity-gain bandwidth product of the VFB is equal to the closed-loop bandwidth of the CFB (at the optimum R2), then the size of the CFB compensation capacitor, C2, is reduced by a factor of $\sqrt{(R2/R_O)}$.

A comparison in an actual application is shown in Figure 1-119 below. The full scale output current of the DAC is 4mA, the net capacitance at the inverting input of the op amp is 20pF, and the feedback resistor is 500Ω. In the case of the VFB op amp, the pole due to C1 occurs at 16MHz. A compensating capacitor of 5.6pF is required for 45° of phase margin, and the signal bandwidth is 57MHz.

$$f_p = \frac{1}{2\pi R2 C1} = 16MHz$$

C2 = 5.6pF

f_X = 57MHz

$$f_p = \frac{1}{2\pi R_O C1} = 160MHz$$

C2 = 1.8pF

f_X = 176MHz

Figure 1-119: *CFB op amp is relatively insensitive to input capacitance when used as an I/V converter*

For the CFB op amp, however, because of the low inverting input impedance ($R_O = 50Ω$), the pole occurs at 160Mhz, the required compensation capacitor is about 1.8pF, and the corresponding signal bandwidth is 176MHz. In practice, the pole frequency is so close to the closed-loop bandwidth of the op amp that it could probably be left uncompensated.

It should be noted that a CFB op amp's relative insensitivity to inverting input capacitance is when it is used in the inverting mode. In the non-inverting mode, however, even a few picofarads of stray capacitance on the inverting input can cause significant gain-peaking and potential instability.
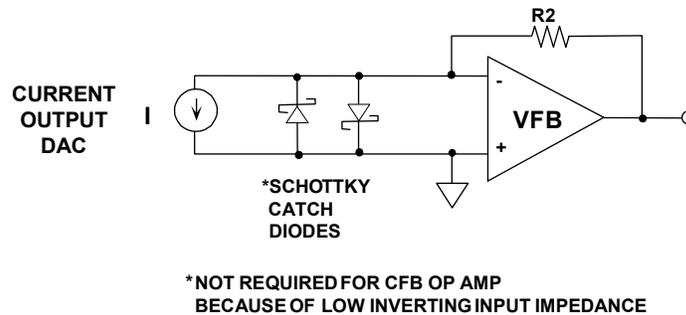
Figure 1-120: *Low inverting input impedance of CFB op amp helps reduce effects of fast DAC transients*

Another advantage of the low inverting input impedance of the CFB op amp is when it is used as an I/V converter to buffer the output of a high speed current output DAC. When a step function current (or DAC switching glitch) is applied to the inverting input of a VFB op amp, it can produce a large voltage transient until the signal can propagate through the op amp to its output and negative feedback is regained. Back-to-back Schottky diodes are often used to limit this voltage swing as shown in Figure 1-120 above. These diodes must be low capacitance, small geometry devices because their capacitance adds to the total input capacitance.

1.123

A CFB op amp, on the other hand, presents a low impedance (R_O) to fast switching currents even before the feedback loop is closed, thereby limiting the voltage excursion without the requirement of the external diodes. This greatly improves the settling time of the I/V converter.

Noise Comparisons between VFB and CFB Op Amps

In most applications of high speed op amps, it is the total output RMS noise that is generally of interest. Because of the high bandwidths involved, the chief contributor to the output RMS noise is therefore the white noise, and the 1/f noise is negligible.

Typical high speed op amps with bandwidths greater than 150MHz or so, and bipolar VFB input stages have input voltage noises ranging from about 2 to 20nV/√Hz.

For a VFB op amp, the inverting and non-inverting input current noise are typically equal, and almost always uncorrelated. Typical values for wideband VFB op amps range from 0.5pA/√Hz to 5pA/√Hz. The input current noise of a bipolar input stage is increased when input bias-current compensation generators are added, because their current noise is not correlated, and therefore adds (in an RSS manner) to the intrinsic current noise of the bipolar stage. However, bias current compensation is rarely used in high speed op amps.

The input voltage noise in CFB op amps tends to be lower than for VFB op amps having the same approximate bandwidth. This is because the input stage in a CFB op amp is usually operated at a higher current, thereby reducing the emitter resistance and hence the voltage noise. Typical values for CFB op amps range from about 1 to 5nV/√Hz.

The input current noise of CFB op amps tends to be larger than for VFB op amps because of the generally higher bias current levels. The inverting and non-inverting current noise of a CFB op amp is usually different because of the unique input architecture, and are specified separately. In most cases, the inverting input current noise is the larger of the two. Typical input current noise for CFB op amps ranges from 5 to 40pA/√Hz. This can often be dominant, except in cases of very high gain, when R1 is small.

The noise sources which dominate the output noise are highly dependent on the closed-loop gain of the op amp and the values of the feedback and feedforward resistors. For high values of closed-loop gain, the op amp voltage noise will tend be the chief contributor to the output noise. At low gains, the effects of the input current noise must also be considered, and may dominate, especially in the case of a CFB op amp.

Feedforward/feedback resistors in high speed op amp circuits may range from less than 100Ω to more than 1kΩ, so it is difficult to generalize about their contribution to the total output noise without knowing the specific values and the closed-loop gain.

The best way to make the noise calculations is to write a simple computer program that performs the calculations automatically, and include all the noise sources. The equation previously discussed can be used for this purpose (see Fig. 1-74, again). In most high speed op amp applications, the source impedance noise can often be neglected for source impedances of 100Ω or less.

◆ **Voltage Feedback Op Amps:**

● **Voltage Noise: 2 to 20nV/√Hz**

● **Current Noise: 0.5 to 5pA/√Hz**

◆ **Current Feedback Op Amps:**

● **Voltage Noise: 1 to 5nV/√Hz**

● **Current Noise: 5 to 40pA/√Hz**

◆ **Noise Contribution from Source Negligible if < 100Ω**

◆ **Voltage Noise Usually Dominates at High Gains**

◆ **Reflect Noise Sources to Output and Combine (RSS)**

◆ **Errors Will Result if there is Significant High Frequency Peaking**

Figure 1-121: High speed op amp noise summary

Figure 1-121 above summarizes the noise characteristics of high speed op amps

DC Characteristics of High Speed Op Amps

High speed op amps are optimized for bandwidth and settling time, not for precision DC characteristics as found in lower frequency precision op amps. In spite of this, however, high speed op amps do have reasonably good DC performance.

Input offset voltages of high speed bipolar input op amps are rarely trimmed, since offset voltage matching of the input stage is excellent, typically ranging from 1 to 3mV, with offset temperature coefficients of 5 to 15µV/°C.

Input bias currents on VFB op amps (with no input bias current compensation circuits) are approximately equal for (+) and (–) inputs, and can range from 1 to 5µA. The output offset voltage due to the input bias currents can be nulled by making the effective source resistance, R3, equal to the parallel combination of R1 and R2.

As previously discussed, this scheme will not work with bias-current compensated VFB op amps which have additional current generators on their inputs. In this case, the net input bias currents are not necessarily equal or of the same polarity.

CFB op amps generally have unequal and uncorrelated input bias currents because the (+) and (−) inputs have completely different architectures. For this reason, external bias current cancellation schemes are also ineffective. CFB input bias currents range from 5 to 15μA, being generally higher at the inverting input.

◆ **High Speed Bipolar Op Amp Input Offset Voltage:**

    ● **Ranges from 1 to 3mV for VFB and CFB**

    ● **Offset TC Ranges from 5 to 15μV/°C**

◆ **High Speed Bipolar Op Amp Input Bias Current:**

    ● **For VFB Ranges from 1 to 5μA**

    ● **For CFB Ranges from 5 to 15μA**

◆ **Bias Current Cancellation Doesn't Work for:**

    ● **Bias Current Compensated Op Amps**

    ● **Current Feedback Op Amps**

Figure 1-122: *High speed op amp offset voltage summary*

Figure 1-122 above summarizes the offset considerations for high speed op amps.

REFERENCES: HIGH SPEED OP AMPS

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