FAIRCHILD SEMICONDUCTOR®

July 2006

FSQ0365RN

Green Mode Fairchild Power Switch (FPS™) for Quasi-Resonant Operation - *Low EMI and High Efficiency*

Features

- Optimized for Quasi-Resonant Converter (QRC)
- Low EMI through Variable Frequency Control and Inherent Frequency Modulation
- High Efficiency through Minimum Voltage Switching
- Narrow frequency variation range over Wide Load and Input Voltage Variation
- Advanced Burst-Mode Operation for Low Standby Power Consumption
- Pulse-by-Pulse Current Limit
- Various Protection functions: Over Load Protection (OLP), Over Voltage Protection (OVP), Abnormal Over Current Protection (AOCP), Internal Thermal Shutdown (TSD)
- Under Voltage Lock Out (UVLO) with Hysteresis
- Internal startup circuit
- Internal High Voltage Sense FET (650V)
- Built-in Soft Start (15ms)

Applications

- Power Supply for DVP player
- Auxiliary Power Supply for PC, LCD TV and PDP TV

Description

In general, a Quasi-Resonant Converter (QRC) shows lower EMI and higher power conversion efficiency compared to a conventional hard-switched converter with a fixed switching frequency. The FSQ0365RN is an integrated Pulse Width Modulation (PWM) controller and Sense FET specifically designed for quasi-resonant operation with minimal external components. The PWM controller includes an integrated fixed frequency oscillator, under voltage lockout, leading edge blanking (LEB), optimized gate driver, internal soft start, temperature-compensated precise current sources for a loop compensation and self protection circuitry. Compared with discrete MOSFET and PWM controller solution, the FSQ0365RN can reduce total cost, component count, size and weight, while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform that is well suited for cost-effective designs of quasi-resonant switching flyback converters.

FSQ-series Product Lineup

Part Number	Package	current limit	R_{dson} (max)	Maximum Output Power[4]				Corresponding Old Devices
				230Vac±15%[3]		85-265Vac		
				Adapter[1]	Open frame[2]	Adapter[1]	Open Frame[2]	
FSQ321	8-Dip	0.7 A	19 Ω	12W	18W	7W	11W	FSDL321 FSDH321
FSQ0165RN	8-Dip	0.9 A	10 Ω	15W	21W	9W	13W	FSDL0165RN
FSQ0265RN	8-Dip	1.2 A	6 Ω	20W	26W	11W	16W	FSDM0265RN FSDM0265RNB
FSQ0365RN	8-Dip	1.5 A	4.5 Ω	24W	30W	13W	19W	FSDM0365RN FSDM0365RNB

Notes:

1. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient.
2. Maximum practical continuous power in an open frame design at 50°C ambient.
3. 230 VAC or 100/115 VAC with doubler.
4. The junction temperature can limit the maximum output power.

Application Diagram and Block Diagram

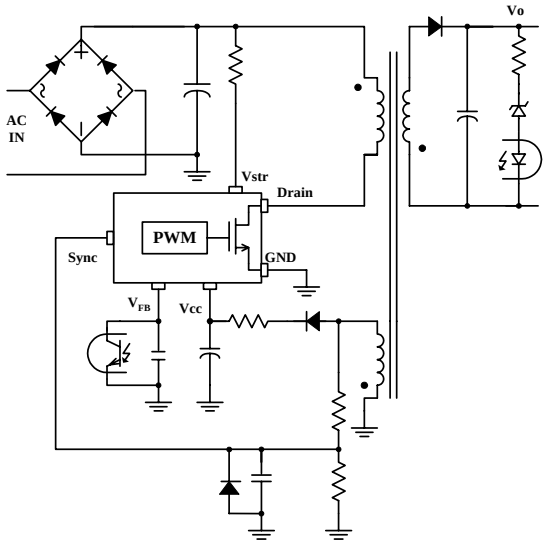

Figure 1. Typical Application Circuit

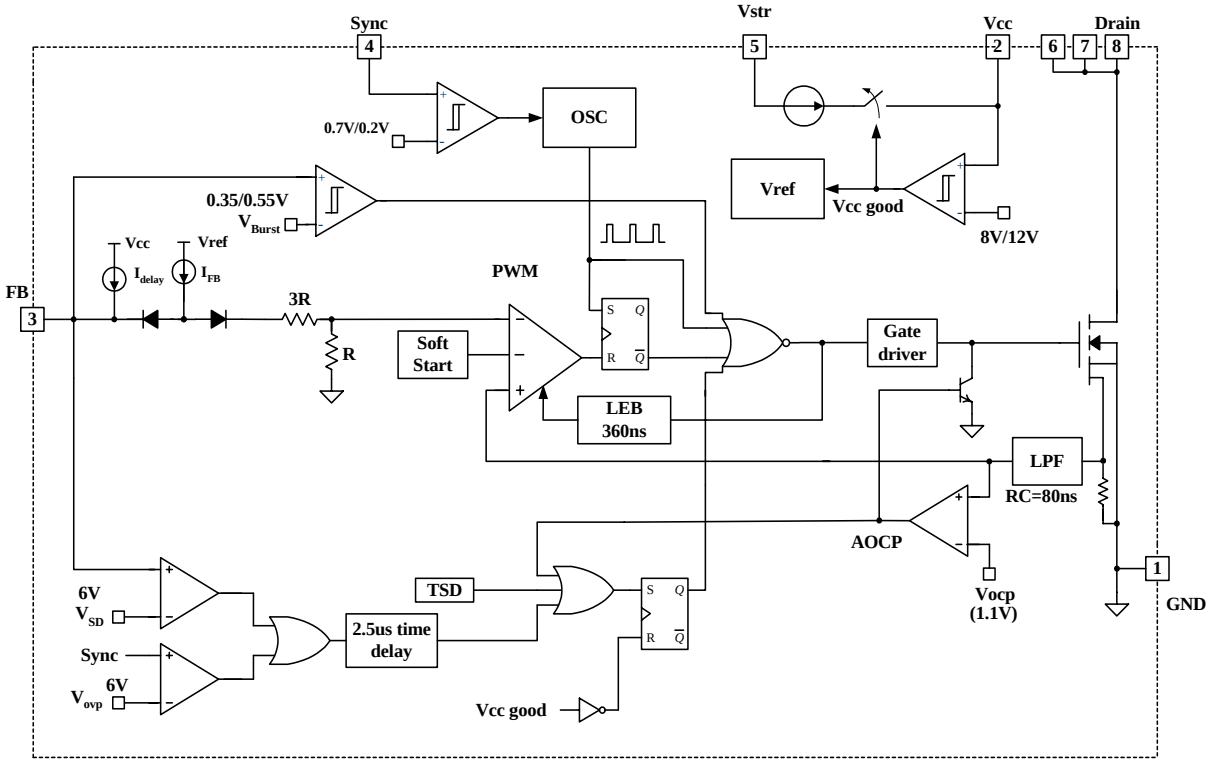

Figure 2. Internal Block Diagram

Pin Assignments

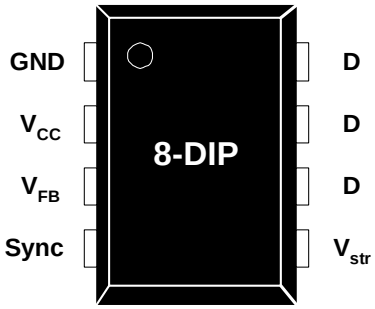

Figure 3. Package diagram

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	GND	This pin is the control ground and the SenseFET source.
2	Vcc	This pin is the positive supply input. This pin provides internal operating current for both start-up and steady-state operation.
3	VFB	This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 6V, the over load protection triggers, which results in the FPS shutting down.
4	Sync	This pin is internally connected to the sync detect comparator for quasi-resonant switching. In normal quasi-resonant operation, the threshold of the sync comparator is 0.7V/0.2V.
5	Vstr	This pin is connected directly or through a resistor to the high voltage DC link. At startup, the internal high voltage current source supplies internal bias and charges the external capacitor that is connected to the Vcc pin. Once Vcc reaches 12V, the internal current source is disabled.
6	D	High voltage power SenseFET drain connection.
7	D	High voltage power SenseFET drain connection.
8	D	High voltage power SenseFET drain connection.

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{STR}	Vstr Pin Voltage	650		V
V_{DS}	Drain Pin Voltage	650		V
V_{CC}	Supply Voltage		20	V
V_{FB}	Feedback Voltage Range	-0.3	9	V
V_{Sync}	Sync Pin Voltage	-0.3	9	V
I_{DM}	Drain Current Pulsed (1)			A
I_D	Continuous Drain Current (Tc=25°C)			A
I_D	Continuous Drain Current (Tc=100°C)			A
E_{AS}	Single Pulsed Avalanche Energy (2)			mJ
P_D	Total Power Dissipation			W
T_J	Operating Junction Temperature		150	°C
T_A	Operating Ambient Temperature	-25	+85	°C
T_{STG}	Storage Temperature	-55	+150	°C

Notes:

1. Repetitive rating: Pulse width limited by maximum junction temperature
2. L=24mH, starting T_J=25°C.

Electrical Characteristics

Parameter	Symbol	Test Condition & Comment	Min.	Typ.	Max.	Unit
SenseFET SECTION						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{CC} = 0V, I_D = 100μA	650	-	-	V
Zero-Gate-Voltage Drain Current	I_{DSS}	V_{DS} = 560V	-	-	100	μA
Drain-Source On-State Resistance	$R_{DS(ON)}$	T_J = 25°C, I_D = 25mA	-	3.6	4.5	Ω
		T_J= 100°C, I_D = 25mA	-			
Input Capacitance	C_{ISS}			315		pF
Output Capacitance	C_{OSS}			47		pF
Reverse Transfer Capacitance	C_{RSS}			9		pF
Turn-on Delay Time	$t_{d(on)}$			11.2		ns
Rise Time	t_r	V_{DS} = 350V, I_D = 25mA	-	34	-	ns
Turn-off Delay Time	$t_{d(off)}$			28.2		ns
Fall Time	t_f	V_{DS} = 350V, I_D = 25mA	-	32	-	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g					nC
Gate-Source Charge	Q_{gs}					nC
Gate-Drain (Miller) Charge	Q_{gd}					nC
CONTROL SECTION						
Maximum ON time	$T_{ON.MAX}$	T_J = 25°C	10.5	12	13.5	us
Blanking time	T_B		13.5	15	16.5	us
Detection time window	T_W	T_J = 25°C, Vsync=0V	2.7	3	3.3	us
Switching Frequency Variation	Δf_S	- 25°C < T_J < 85°C	-	±5	±10	%
Feedback Source Current	I_{FB}	V_{FB} = 0V	700	900	1100	μA
Minimum Duty Cycle	D_{MIN}	V_{FB} = 0V	-	-	0	%
UVLO Threshold Voltage	V_{START}		11	12	13	V
	V_{STOP}	After Turn-on	7	8	9	V
Internal Soft Start Time	$t_{S/S}$	With free-running frequency		15		ms
BURST MODE SECTION						
Burst Mode Voltage	V_{BURH}	T_J = 25°C, t_{PD} = 200ns[1]	0.45	0.55	0.65	V
	V_{BURL}		0.25	0.35	0.45	V
	Hysteresis		-	200	-	mV
PROTECTION SECTION						
Peak Current Limit		T_J = 25°C, di/dt = 300mA/us,	1.32	1.5	1.68	A
Shutdown Feedback Voltage	V_{SD}	V_{CC} = 15V	5.5	6.0	6.5	V
Shutdown Delay Current	I_{DELAY}	V_{FB} = 5V	4	5	6	μA
Leading Edge Blanking Time	t_{LEB}		-	360	-	ns
Over Voltage Protection	V_{OVP}	V_{CC} = 15V, V_{FB} = 2V	5.5	6.0	6.5	V
Over Voltage Protection Blanking Time	t_{OVP}		2.0	2.5	3.0	μs

Over Current Latch Voltage	V_{OCP}		0.95	1.1	1.25	V
Over voltage protection Blanking Time	T_{OVP}		2.0	2.5	3.0	μs
Thermal Shutdown Temperature	T_{SD}		125	140	155	°C
Sync SECTION						
Sync Threshold Voltage	V_{SH}		0.55	0.7	0.85	V
	V_{SL}		0.14	0.2	0.26	V
Sync Delay Time	t_{Sync}		270	200	230	ns
TOTAL DEVICE SECTION						
Operating Supply Current (Control Part Only)	I_{OP}	V_{CC} = 5.8V	1	3	5	mA
Start Current	I_{START}	Vcc=10V (before Vcc reaches Vstart)	300	400	500	mA
Start-up Charging Current	I_{CH}	V_{CC} = 0V, V_{str} = min 40V	0.7	0.85	1.0	mA
V_{str} Supply Voltage	V_{STR}		35	-	650	V

Notes:
1. Propagation delay in the control IC

Functional Description

1. Startup : At startup, an internal high voltage current source supplies the internal bias and charges the external capacitor (Ca) that is connected to the V_{CC} pin as illustrated in Figure 4. When V_{CC} reaches 12V, the FPS begins switching and the internal high voltage current source is disabled. Then, the FPS continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 8V.

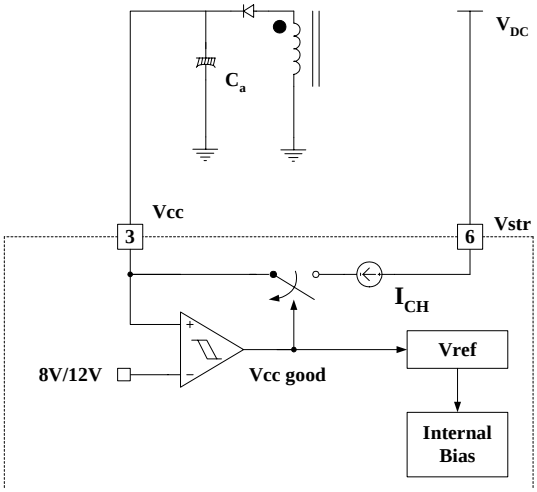

Figure 4. Startup Block

2. Feedback Control: FPS employs current mode control, as shown in Figure 5. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the Rsense resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the KA431 exceeds the internal reference voltage of 2.5V, the H11A817A LED current increases, thus pulling down the feedback voltage and reducing the duty cycle. This event typically happens when the input voltage is increased or the output load is decreased.

2.1 Pulse-by-pulse current limit: Because current mode control is employed, the peak current through the Sense FET is limited by the inverting input of PWM comparator (Vfb*) as shown in Figure 5. Assuming that the 0.9mA current source flows only through the internal resistor (2.5R +R= 2.8 kΩ), the cathode voltage of diode D2 is about 2.5V. Since D1 is blocked when the feedback voltage (Vfb) exceeds 2.5V, the maximum voltage of the cathode of D2 is clamped at this voltage, thus clamping Vfb*. Therefore, the peak value of the current through the Sense FET is limited.

2.2 Leading edge blanking (LEB): At the instant the internal Sense FET is turned on, there usually exists a high current spike through the Sense FET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the Rsense resistor would lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (T_{LEB}) after the Sense FET is turned on.

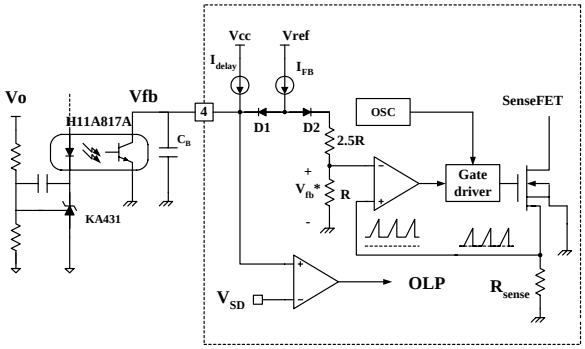

Figure 5. Pulse width modulation (PWM) circuit

3. Synchronization: The FSQ-Series employs a quasi-resonant switching technique to minimize the switching noise and loss. The basic waveforms of the quasi-resonant converter are shown in Figure 6. In order to minimize the MOSFET's switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value as shown in Figure 6. The minimum drain voltage is indirectly detected by monitoring the V_{CC} winding voltage as shown in Figure 6.

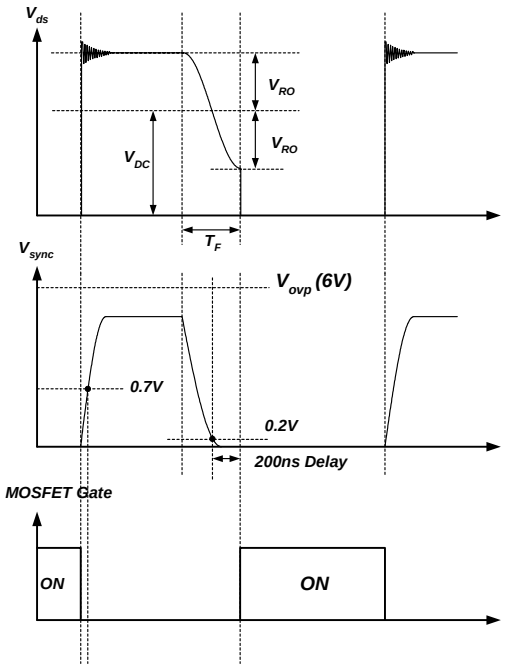

Figure 6. Quasi-resonant switching waveforms

4. Protection Circuits: The FSQ-Series has several self-protective functions such as over load protection (OLP), abnormal over current protection (AOCP), over voltage protection (OVP) and thermal shutdown (TSD). All the protections are implemented as auto-restart mode. Once the fault condition is detected, switching is terminated and the Sense FET remains off. This causes V_{CC} to fall. When V_{CC} falls down to the under voltage lockout (UVLO) stop voltage of 8V, the protection is reset and startup circuit charges V_{CC} capacitor. When V_{CC} reaches the start voltage of 12V, the FSQ-Series resumes its normal operation. If the fault condition is not removed, the Sense FET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated.

Because these protection circuits are fully integrated into the IC without external components, the reliability can be improved without increasing cost.

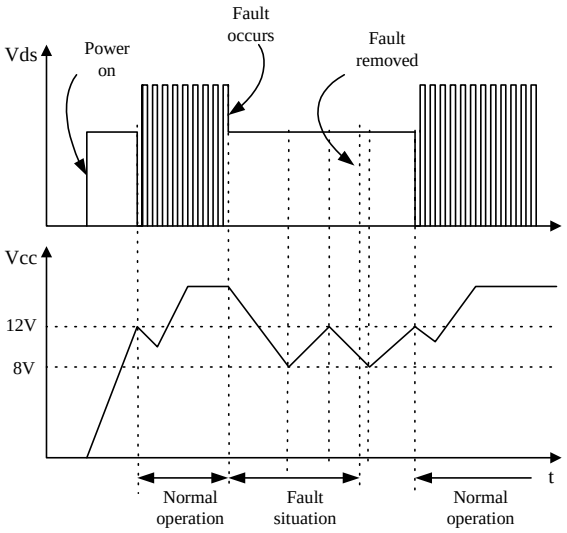

Figure 7. Auto restart protection waveforms

4.1 Over Load Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger in order to protect the SMPS. However, even when the SMPS is in the normal operation, the over load protection circuit can be triggered during the load transition. In order to avoid this undesired operation, the over load protection circuit is designed to trigger after a specified time to determine whether it is a transient situation or an overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the Sense FET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (Vo) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (Vfb).

If Vfb exceeds 2.8V, D1 is blocked and the 5uA current source starts to charge C_B slowly up to V_{CC}. In this condition, Vfb continues increasing until it reaches 6V, when the switching operation is terminated as shown in Figure 8. The delay time for shutdown is the time required to charge C_B from 2.8V to 6V with 5uA. In general, a 20 ~ 50 ms delay time is typical for most applications.

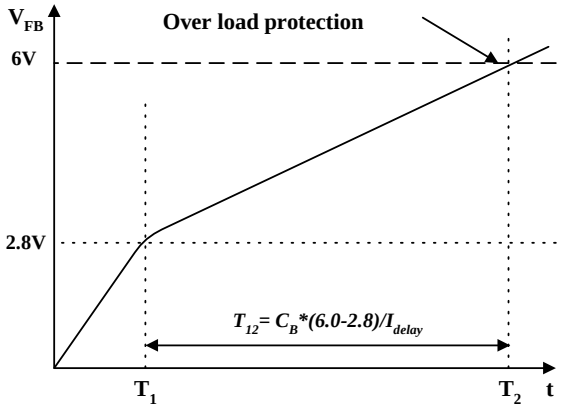

Figure 8. Over load protection

4.2 Abnormal Over Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the Sense FET during the LEB time. Even though the FSQ-Series has OLP (Over Load Protection), it is not enough to protect the FSQ-Series in that abnormal case, since severe current stress will be imposed on the Sense FET until OLP triggers. The FSQ-Series has an internal AOCP (Abnormal Over Current Protection) circuit as shown in Figure 9. When the gate turn-on signal is applied to the power Sense FET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is then compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the latch, resulting in the shutdown of SMPS.

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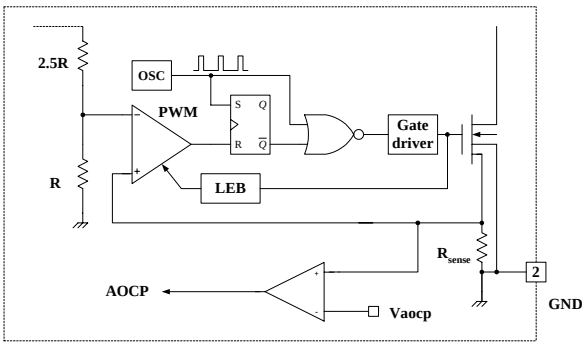


Figure 9. Abnormal over current protection

4.3 Over Voltage Protection (OVP): If the secondary side feedback circuit malfunctions or a solder defect causes an open in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then, Vfb climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection triggers. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the over load protection triggers, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, the peak voltage of the sync signal is proportional to the output voltage and the FSQ-Series uses a sync signal instead of directly monitoring the output voltage. If the sync signal exceeds 6V, an OVP is triggered resulting in a shutdown of SMPS. In order to avoid undesired triggering of OVP during normal operation, the peak voltage of the sync signal should be designed to be below 6V.

4.4 Thermal Shutdown (TSD): The Sense FET and the control IC are built in one package. This makes it easy for the control IC to detect the abnormal over temperature of the Sense FET. When the temperature exceeds approximately 150°C, the thermal shutdown triggers.

5. Soft Start : The FPS has an internal soft start circuit that increases PWM comparator inverting input voltage together with the Sense FET current slowly after it starts up. The typical soft start time is 15msec, The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode during startup.

6. Burst operation: In order to minimize power dissipation in standby mode, the FPS enters burst mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 10, the device automatically enters burst mode when the feedback voltage drops below V_{BURL} (350mV). At this point switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (550mV) switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the power Sense FET thereby reducing switching loss in standby mode.

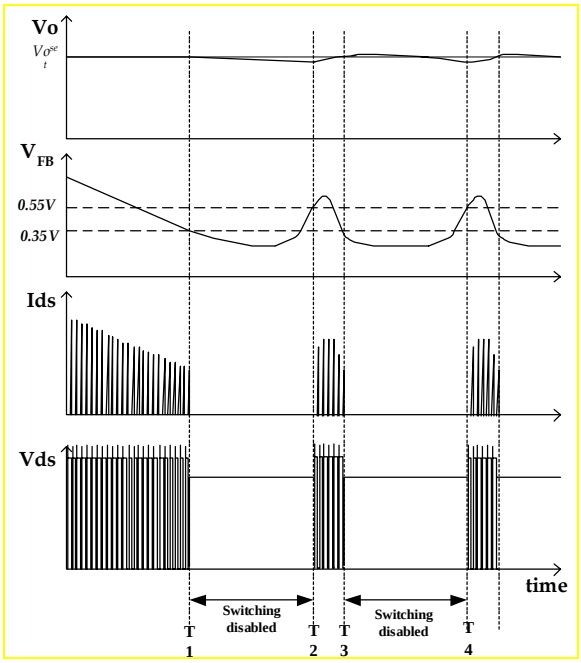
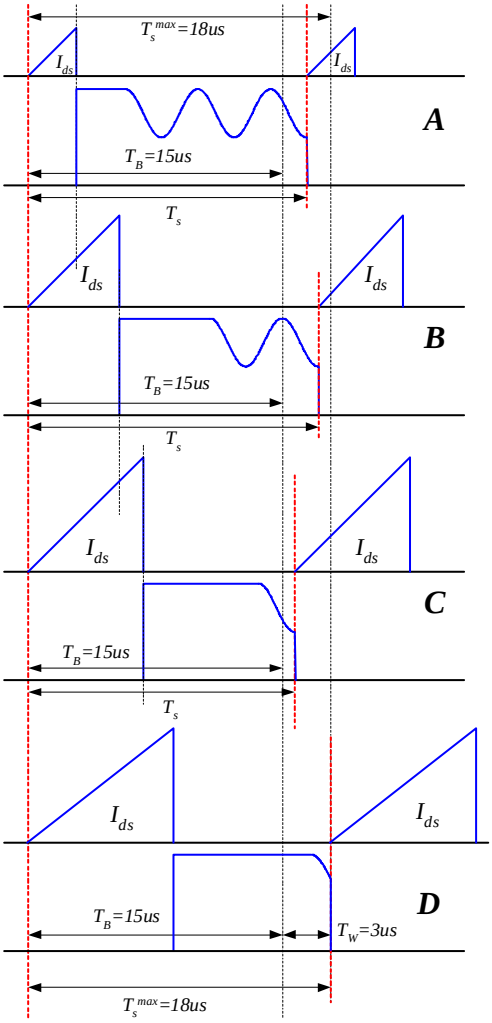


Figure 10. Burst mode operation

7. Switching Frequency Limit: To minimize switching loss and EMI (Electromagnetic Interference), MOSFET turns on when the drain voltage reaches its minimum value in Quasi-resonant operation. However, this causes switching frequency to increases at light load conditions. As the load decreases, the peak drain current diminishes and, therefore, the switching frequency increases. This results in severe switching losses at light load condition, as well as intermittent switching and audible noise. Because of these problems, the quasi-resonant converter topology has limitations in a wide range of applications.

In order to overcome this problem, FSQ-series employs frequency limit function as shown in Figure 11 and 12. Once Sense FET is turned on, the next turn-on is prohibited during the blanking time (T_{BLK}). After the blanking time, the controller finds the valley within detection time window (T_{DW}) and turns on the MOSFET as shown in Figure 11 and 12 (Case A, B, and C). If no valley is found during T_{DW}, the internal Sense FET is forced to turn on at the end of t_{DW} (Case D). Therefore, FSQ0365RN has its minimum switching frequency 55kHz and maximum switching frequency 67kHz as shown in Figure 12.

Figure 11. QRC Operation with Limited Frequency



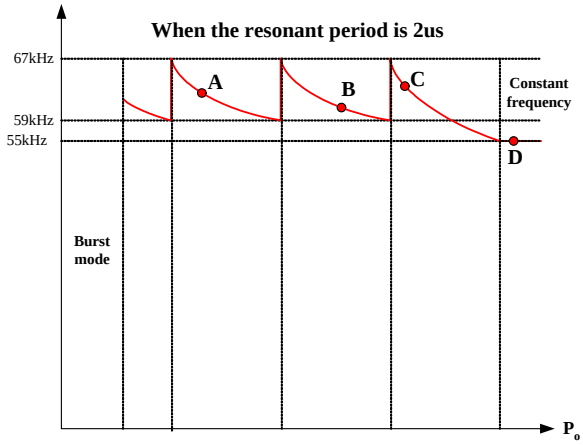


Figure 12. Switching Frequency Range

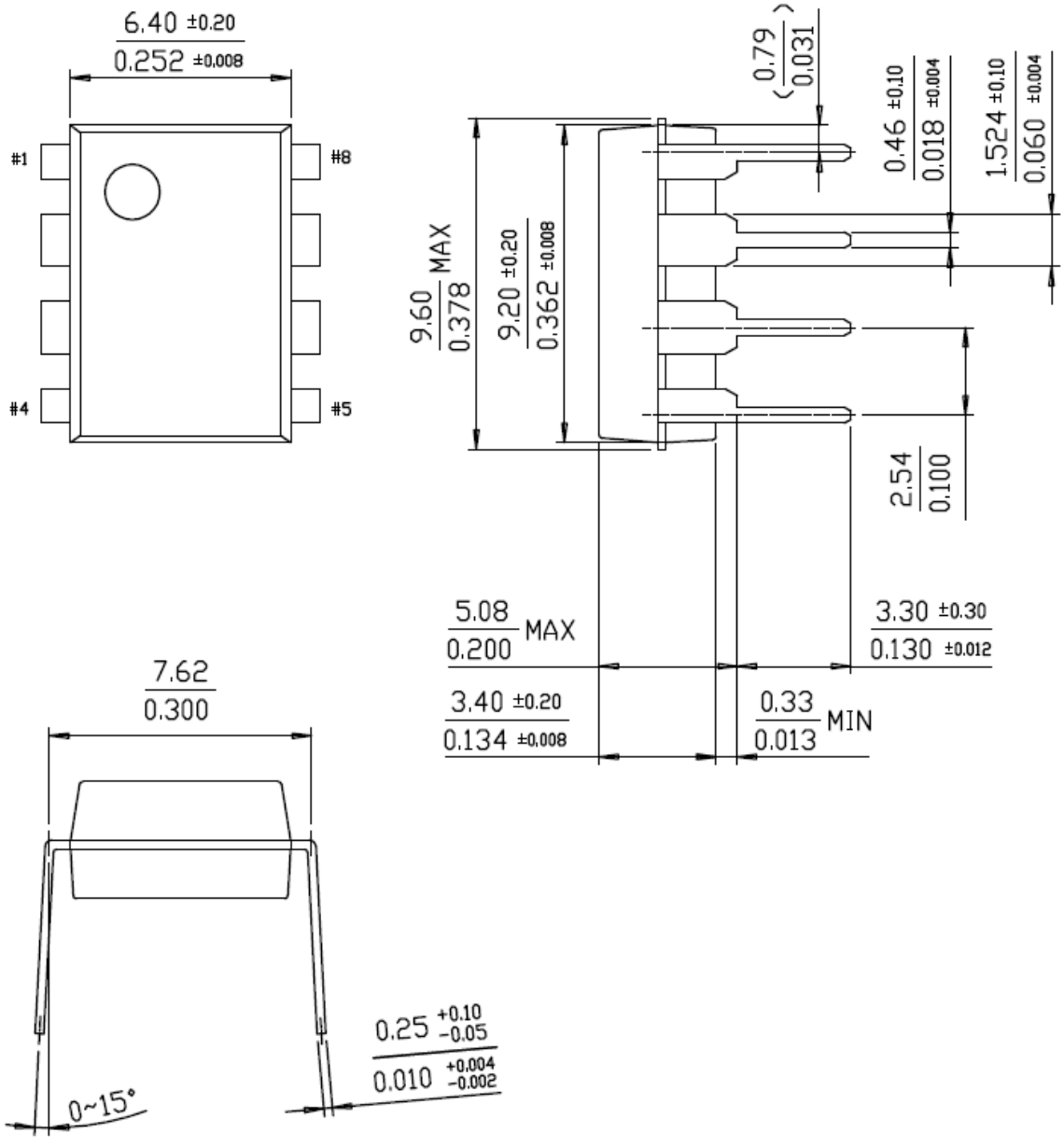
Typical Performance Characteristics

Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packing Method
FSQ321	8-Dip	Yes	-25 to +85	
FSQ0165RN	8-Dip	Yes	-25 to +85	
FSQ0265RN	8-Dip	Yes	-25 to +85	
FSQ0365RN	8-Dip	Yes	-25 to +85	

Physical Dimensions

8-DIP



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DOME™	IntelliMAX™	PowerEdge™	SuperSOT™-3	UHC™
EcoSPARK™	ISOPLANAR™	PowerSaver™	SuperSOT™-6	UltraFET®
E^2CMOS™	LittleFET™	PowerTrench®	SuperSOT™-8	UniFET™
EnSigna™	MICROCOUPLER™	QFET®	SyncFET™	VCX™
FACT™	MicroFET™	QS™	TCM™	Wire™
FACT Quiet Series™	MicroPak™	QT Optoelectronics™	TinyBoost™	
FAST®	MICROWIRE™	Quiet Series™		
FASTr™	MSX™	RapidConfigure™	Across the board. Around the world.™	
FPS™	MSXPro™	RapidConnect™	Programmable Active Droop™	
FRFET™	OCX™	ScalarPump™	The Power Franchise®	

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PRODUCT STATUS DEFINITIONS

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